Measurements and Modelling of Delay Lines on Printed Circuit Boards

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Abstract:

Traces on printed circuit boards (PCBs) are often turned into meandering lines to introduce an additional delay. This technical report explores the electrical parasitics involved in that practice by reporting measurements of traces fabricated on a test board. Traces that meander have shorter propagation delays than expected due to coupling between segments. Calculations of the time delay reduction are presented and a model is proposed.

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1.0 Introduction

Designers of printed circuit boards often face the problem illustrated by the example in Figure 1. It is desired to transmit signals 1, 2 and 3 from one chip to the other with precisely the same transmission delay. However, with the routing pattern in Figure 1a, signal 3 has a longer path and will arrive later. The conventional solution, shown in Figure 1b, artificially extends the paths of signals 1 and 2 to match the lengths of all wires.

An example where meander lines might be used is as a bus between a processor and memory. Another example is a clock distribution tree between a clock synthesizer and target clocked circuits.

Traces such as those for signals 1 and 2 are called serpentine lines or meander lines. In the past, meander lines have been used with the assumption that the extra wire length is electrically identical to a straight section, and no parasitics were introduced. As trace dimensions become smaller and signal frequencies increase, that assumption may no longer be valid.

In this report, we present measurements of the time delay through, and characteristic impedance of meander lines as compared to an equivalent length of straight line.

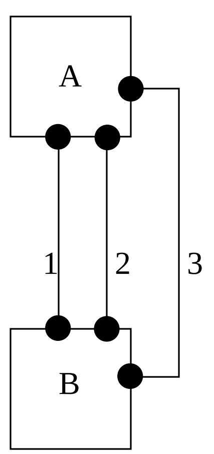

Figure 1a: Unequal Wire Lengths

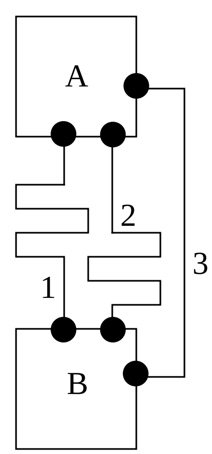

Figure 1b: Equal Wire Lengths

It is seen that the delay through a meander line is shorter than the delay through an equivalent length of straight trace. This is because coupling between the segments of the meander lines shortens the electrical path.

The remainder of this report is organized as follows. Section 2 gives the physical background of transmission lines and meander lines, and defines terms used in the rest of the report. Section 3 discusses our measurement methods and reports experimental results. In Section 4, we discuss the results, and Section 5 gives a model for the observed effects. Finally, Section 6 gives conclusions.

2.0 Background

2.1 Meander Line Parameters

A meandering section of a PCB trace might look like the wire of Figure 2. The straight path between points A and D is interrupted by several zigzagging segments. We define N as the number of segments in the meander section, l as the length of each section, and d as the pitch (center-to-center spacing of adjacent traces).

In practice, meandering sections are not always rectangular as shown, in order to fit into the odd shapes found on a PCB.

2.2 Transmission Line Circuit Theory

Digital signals are electromagnetic waves that propagate along guiding structures at a finite speed. Because their speed is finite, the waves have a non-zero physical extent—a wavelength. At any given time, the values of the electric and magnetic fields for a particular wave vary with respect to position. Therefore, the voltage and current are different at different points along a wavelength.

In this report, we are concerned with wavelengths as small as 1.5 cm, while we are trying to describe wires that are several centimeters long. Clearly, we cannot consider such a wire as a circuit lumped at a single point. One approach is to model the wires as a succession of sections, which are individually small compared to a wavelength, and therefore can be modelled as lumped elements. Using calculus it is possible to extend this method to sections of infinitesimal length, and describe wires as *distributed* circuit elements called transmission lines.

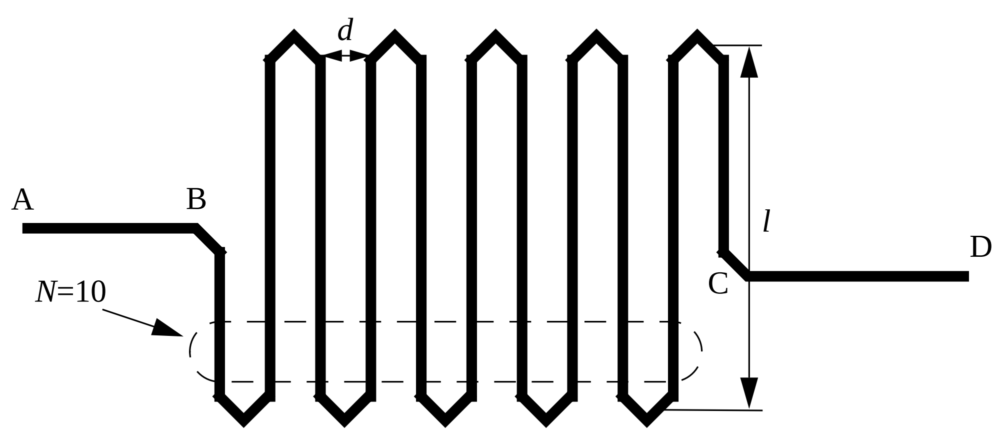

Figure 2: Meander Line Example

A transmission line consists of at least two conductors extending parallel to one another for some length, separated by a non-conducting dielectric. Electromagnetic waves propagate in the dielectric along the length of the line. There are many excellent references for transmission lines and distributed circuit elements [1-5]. In the remainder of this section, we will present some equations and concepts useful in dealing with transmission lines.

<u>Capacitance Per Unit Length</u> Symbol: *C* Units: pF/m

The capacitance between two conductors of a transmission line, divided by the length of the line. It depends on the geometry of the transmission line cross-section and the permittivity (ε) of the dielectric. See Figure 3 for a circuit model of an infinitesimally small section of transmission line.

<u>Inductance Per Unit Length</u> Symbol: *L* Units: nH/m

The inductance of the current loop formed by the two conductors of a transmission line, divided by the length of the line. It depends on the geometry of the transmission line cross-section. See Figure 3.

<u>Resistance Per Unit Length</u> Symbol: *R* Units: Ω/m

The resistance of the transmission line conductors, per unit length of line. It depends on the geometry of the transmission line cross-section, the conductivity of the conductor material, and the frequency of the signal. Because of the skin effect [1], resistance increases with frequency. See Figure 3.

<u>Conductance Per Unit Length</u> Symbol: *G* Units: S/m

High-frequency electromagnetic fields in a dielectric cause oscillations in the local polarization of the dielectric. These oscillations dissipate power from the transmitted signal. This effect is usually negligible. See Figure 3.

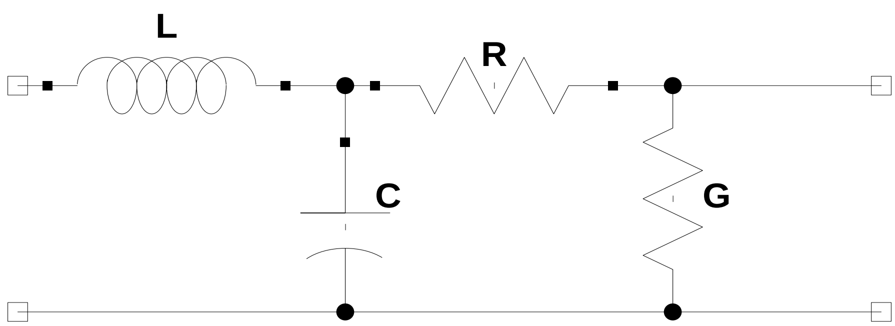

Figure 3: *RLGC* Model of Transmission Line Section

<u>Permittivity and Relative Permittivity</u> Symbol: ε and ε_r Units: F/m and dimensionless

Permittivity is the ratio between electric field strength and electric flux density. It is a property of a material. The permittivity of free space is a universal constant with the value $\varepsilon_0 = 8.854$ pF/m. The total permittivity of a material is found by multiplying ε_0 and ε_r.

$$\varepsilon = \varepsilon_r \cdot \varepsilon_0 \tag{2-1}$$

We will use 4.3 as the relative permittivity of FR-4, a material commonly used as a dielectric in PCBs.

Wave Velocity Symbol: v Units: m/s

The velocity at which the signal propagates. It depends on the relative permittivity of the dielectric and is given by Equation 2-2:

$$v = \frac{c}{\sqrt{\varepsilon_r}} \tag{2-2}$$

c is the speed of light in a vacuum, which is 3×10^8 m/s.

Characteristic Impedance Symbol: Z_0 Units: Ω

Defined by Equation 2-3, the characteristic impedance is a property of the line. It is the input impedance of the line, but no power is dissipated by this impedance.

$$Z_0 = \sqrt{\frac{L}{C}} \tag{2-3}$$

Reflection Coefficient Symbol: ρ or Γ Units: Dimensionless

When a wave hits an impedance discontinuity, either at the boundary between two transmission lines of different Z_0 or when entering or leaving a transmission line, part of the wave is reflected and part is transmitted. The reflection coefficient, as shown in the first part of Equation 2-4, gives the fraction of the incident wave amplitude that is reflected. The value of ρ is bounded by -1 and 1. The second part of Equation 2-4 shows how ρ may be calculated; Z_1 refers to the input impedance of the network on which the wave is incident.

$$\rho = \frac{V_{reflected}}{V_{incident}} = \frac{Z_1 - Z_0}{Z_1 + Z_0} \tag{2-4}$$

Scattering Parameters (S-parameters) Symbol: S_{11}, S_{12}, S_{21}, and S_{22} Units: Dimensionless

S-parameters are a generalization of the reflection coefficient. They include transmission information and are complex quantities. In the two-port network of Figure 4 for example, S_{11} gives the fraction of the wave input at port 1 that returns out of port 1, and S_{21} is the fraction of the wave input at port 1 that transmits to port 2. S-parameters can be displayed in magnitude-phase form as a function of frequency, or in a polar plot known as a Smith chart, parameterized by frequency.

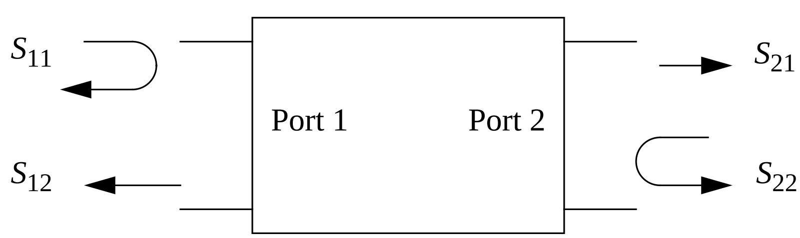

Figure 4: Two-Port Network

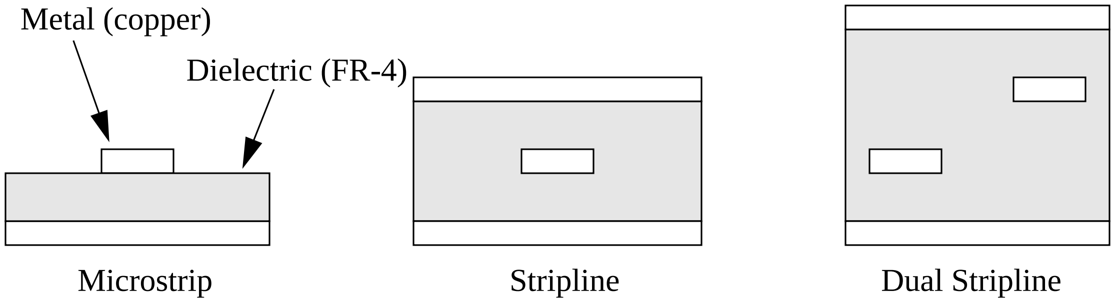

Figure 5: Common PCB Trace Geometries

2.3 Printed Circuit Boards and Traces

A quick review of PCB trace terminology is in order. Figure 5 (not to scale) shows cross-sections of typical wire geometries. A **microstrip** is a trace that runs on the surface of a board and has a nearby reference plane. **Striplines** are signals enclosed in adjacent reference planes. The final geometry is the most common--a **dual stripline** where two signal layers are routed between two reference planes, usually power and ground. Usually the routing directions of the two layers are perpendicular (**orthogonal dual striplines**), though this is not shown here. The dual stripline geometry is also called **asymmetric stripline**.

2.4 Characterization Methods

2.4.1 Time-Domain Transmission (TDT)

In TDT, a fast step function in voltage is put into the input of a network under test and the output is watched. TDT is useful in measuring delay through a network and looking for distortion. TDT is not very useful for extracting a circuit model since the effects of all the components in the network under test are superimposed at one point in time.

2.4.2 Time-Domain Reflectometry (TDR)

TDR is a measurement method which probes a network by exciting it with a step and watching the reflections. Background on the principles of TDR can be found in [1]. A TDR graph shows reflection coefficient (as observed at the source) as a function of time. A series inductance shows up as a peak, a shunt capacitance shows up as a dip, and a transmission line is a horizontal line where height corresponds to its characteristic impedance. A lossy transmission line has an upward slope.

Normalized characteristic impedance at any point can be calculated by Equation 2-5:

$$Z_1 = \frac{1+\rho}{1-\rho} \cdot Z_0 \qquad (2\text{-}5)$$

where Z_0 is the characteristic impedance of the test equipment (usually 50 Ω).

2.4.3 Network Analysis

A network analyzer characterizes a two-port system in the frequency domain. At each of several frequencies, the network analyzer injects a sine wave into each port of the network in turn, then measures the transmitted and reflected waves to compute the S-parameters.

3.0 Measurements of Meander Lines

3.1 Test Setup

In this section, we present time-domain and network analyzer measurements for three actual asymmetric stripline traces. Figure 6 shows the three traces as they appear on the board (not to scale). One of the traces (trace (c) of Figure 6) is straight; the other two contain one inch of straight trace, two inches of meandering, then three inches of straightaway (traces (a) and (b) in Figure 6). The actual board has three sets of the traces shown in Figure 6.

Figure 7 shows a cross-section of the geometry used in the meandering sections of trace (a) and trace (b). Trace (a) used a 15-mil[1] pitch (d=15 mils in Figure 7) and trace (b) used a 10-mil pitch (d=10 mils in Figure 7). The traces were 1/2-ounce copper, about 0.7 mils thick.

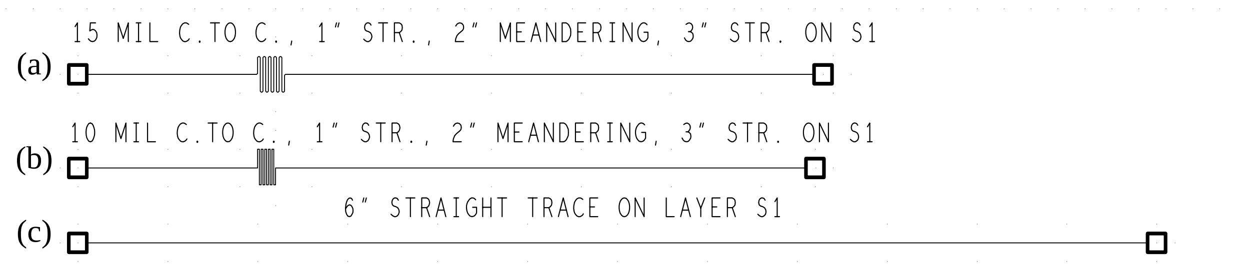

Figure 6: Test Traces (One Set)

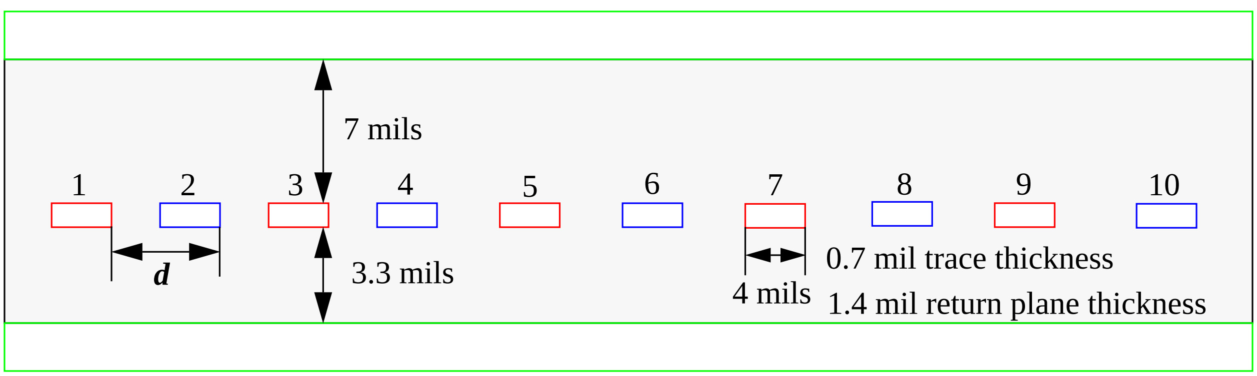

Figure 7: Cross-section of Meander Line Model

1. 1 mil = 0.001 inch = 0.0254 mm

The time-domain measurements were done with a Tektronix 11801 digital sampling oscilloscope. The input to the network was a voltage step of amplitude 250 mV and risetime 38 ps. The network analyzer used was an Agilent 8722ES. The test port power was -10dBm.

3.2 Time-Domain Transmission (TDT)

Figure 8 shows the time-domain transmission results from the three sets of three test traces, superimposed. These are the waveforms seen at the output of each trace. The first group of curves is for the 10-mil-pitch lines, the second for the 15-mil-pitch lines, and the third for the straight lines. The amplitude has been normalized with respect to the 250-mV step. The incident step happens at time 0. The delays are clearly different for the three line types (meandering with 10-mil pitches, meandering with 15-mil pitches, and straight).

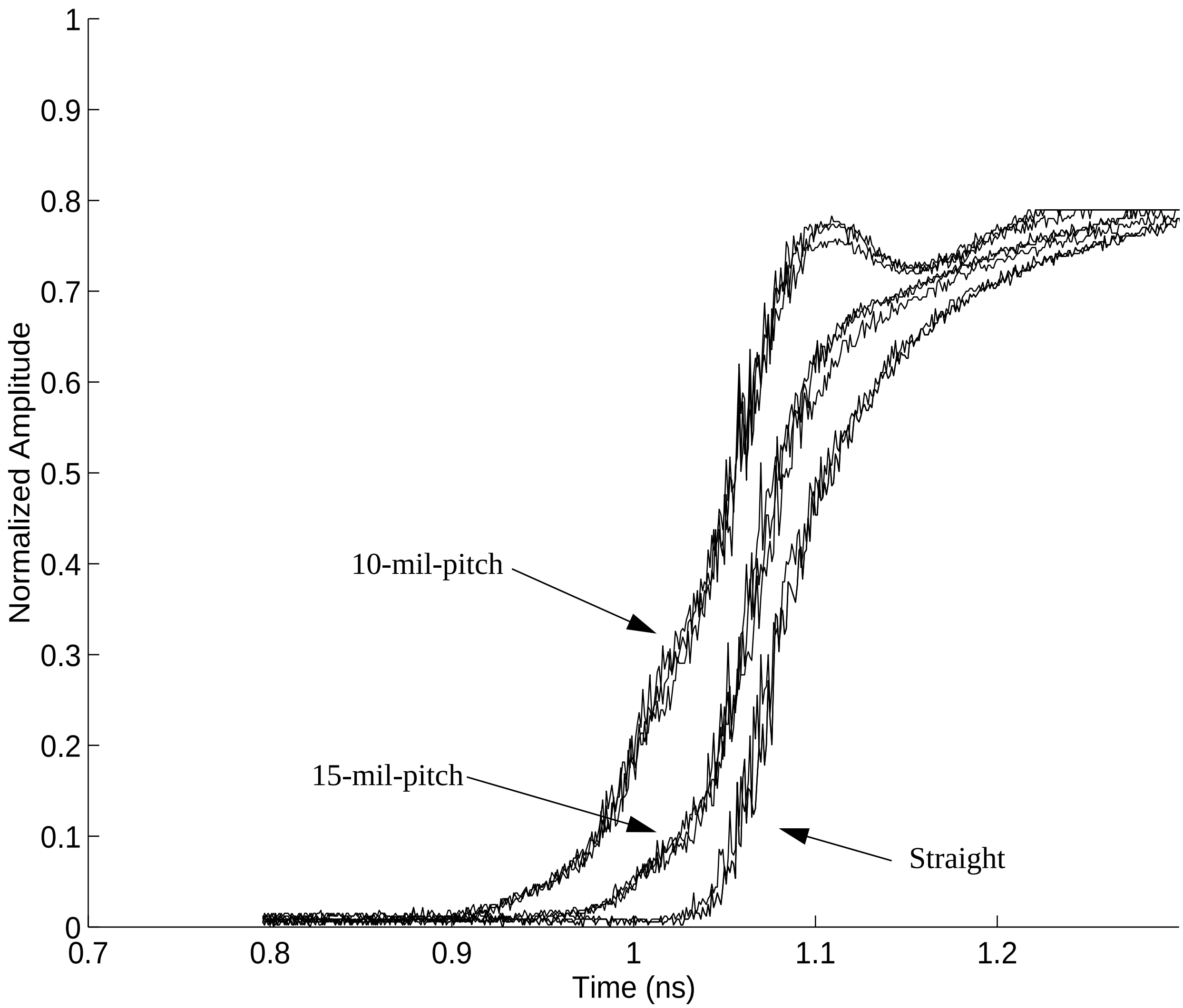

Figure 8: Time-Domain Transmission Results for Three Trace Types

3.3 Time-Domain Reflectometry (TDR)

Figure 9 shows a similar plot for the TDR results, where reflection coefficient has been converted into characteristic impedance. The incident step happens at time 0. The three sets of three traces are superimposed, but cannot be easily distinguished. There are no apparent correlations between line type and characteristic impedance. Each trace seems to have a characteristic impedance between about 55 Ω and 65 Ω, with no apparent pattern as to how impedance varies along the line.

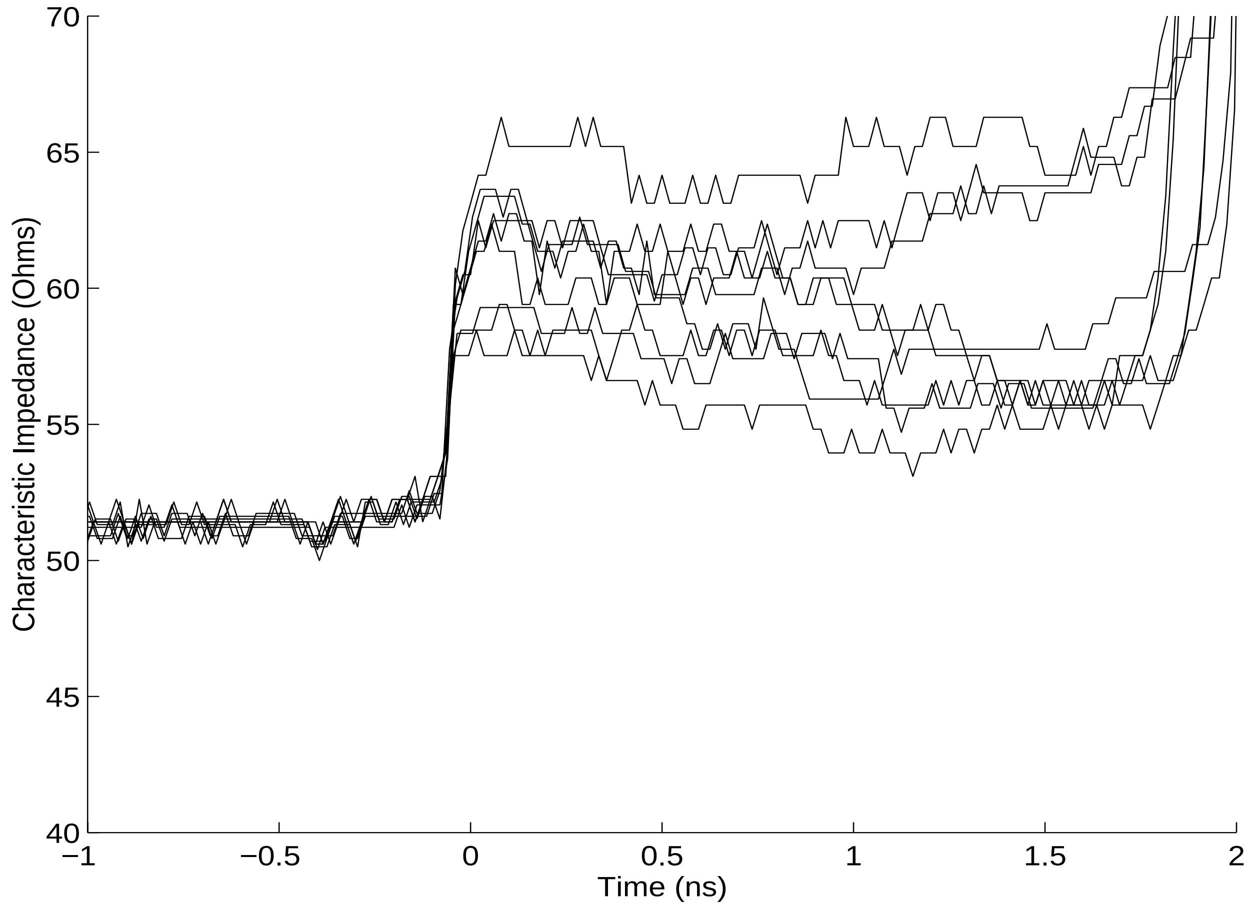

Figure 9: Reflections Measured for Three Trace Types

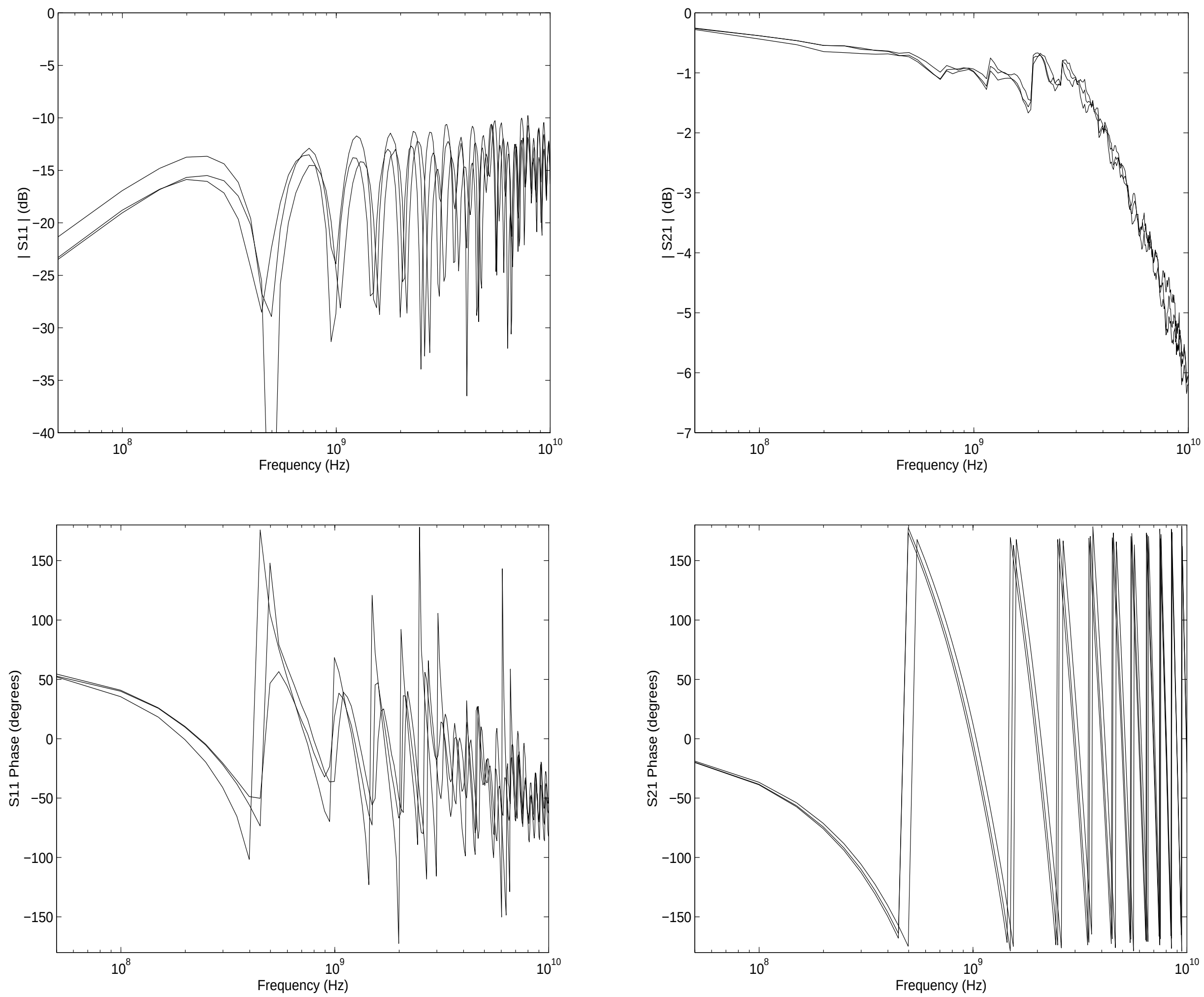

Figure 10: S_{11} and S_{21} for Three Trace Types

3.4 Network Analysis

Figure 10 presents S_{11} and S_{21} in magnitude and phase form for a straight trace, a 15-mil-pitch trace, and a 10-mil-pitch trace plotted together. Only one sample of each trace type is plotted in each chart.

4.0 Discussion of Results

The TDT picture of Figure 8 allows calculation of the time delays through each type of line. Clearly, the meandering lines are faster than a straight line of equivalent length. The trend is plotted in Figure 11. The horizontal axis of Figure 11 corresponds to the vertical axis of Figure 8: the fraction of full-scale voltage, or amplitude. For each amplitude level we have plotted the range of the differences in delay between each meander line and the straight line. For example, the 15-mil-pitch lines led the straight line by 21-38 ps.

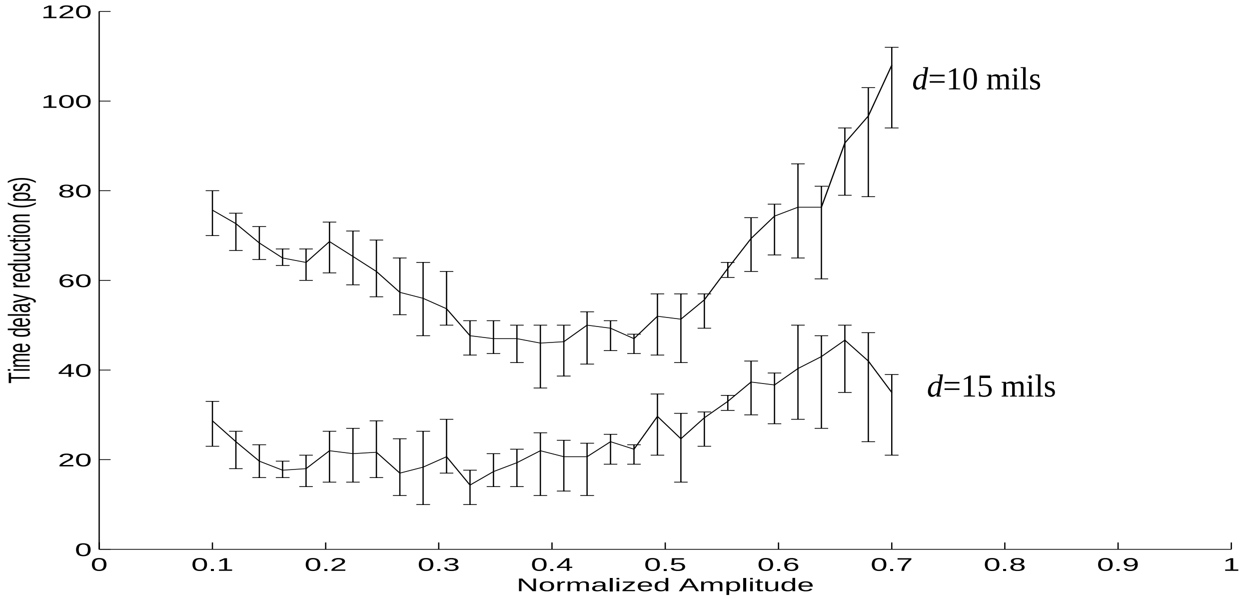

Figure 11: Time Delay Reduction

Delay differs with the receiver's threshold. Figure 11 shows how much time delay reduction, and variance in time delay, can be expected for a given logic threshold. For example, a receiver with a threshold of one-half the full-scale voltage will detect the delay for the 15-mil-pitch line as 30 ps shorter than the delay for the straight line, and the delay for the 10-mil-pitch line is 50 ps shorter than the delay for the straight line.

Therefore designers may think they have matched delays, but have actually created 50 ps of skew.

The time delay reduction measurements are summarized in Table 1.

Table 1: Time Delay Reduction

d (mils)	Nominal Meander Delay (ps)	Reduction (ps)	Error
Straight	340	0	0
15	340	30	9%
10	340	50	15%

The nominal meander delay was calculated by Equation 4-1, where Equation 2-2 has been used for velocity, and *L* refers to the intended length of the meandering section:

$$T_{nom} = \frac{L}{v} = \frac{L}{c/\sqrt{\varepsilon}} = \frac{2in}{3 \times 10^8 \frac{m}{s} / \sqrt{4.3}} = 340ps \qquad (4\text{-}1)$$

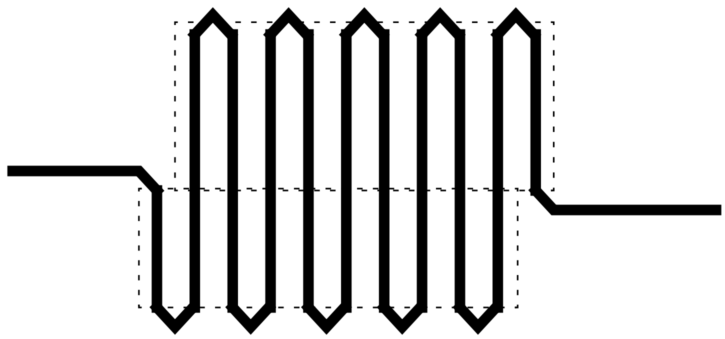

Figure 12: Meander Line Partitioned into Two Sets of Coupled Transmission Lines

The TDR measurements of Figure 9 do not indicate a trend for the characteristic impedance that relates to the presence of a meander line. The variations from trace to trace caused by measurement or manufacturing errors dominate any meander-line effects.

Also, the S-parameter graphs of Figure 10 do not show significant differences. All three lines graphed have similar attenuation and reflection characteristics.

5.0 Linked-W Element Circuit Model

A circuit model suitable for simulation in HSPICE has been developed which predicts the time delay reduction effect. This model is based on the observation that the center of Figure 12 looks like an array of wires running vertically. That array can be modelled as *N* coupled transmission lines with the HSPICE W element. In this section, we discuss how the model is constructed, present time-domain simulation results, and compare those results to the measured values.

5.1 Construction of Linked-W Model

Each of the dashed rectangles contains a set of *N* parallel, lossy, coupled lines. Each rectangle can be replaced with a W element for simulation in HSPICE. Each W element will have 2*N*+1 terminals (two for each signal conductor segment and one for a ground reference). These terminals can be stitched together with ideal wires, and lumped capacitance can optionally be added at the turns.

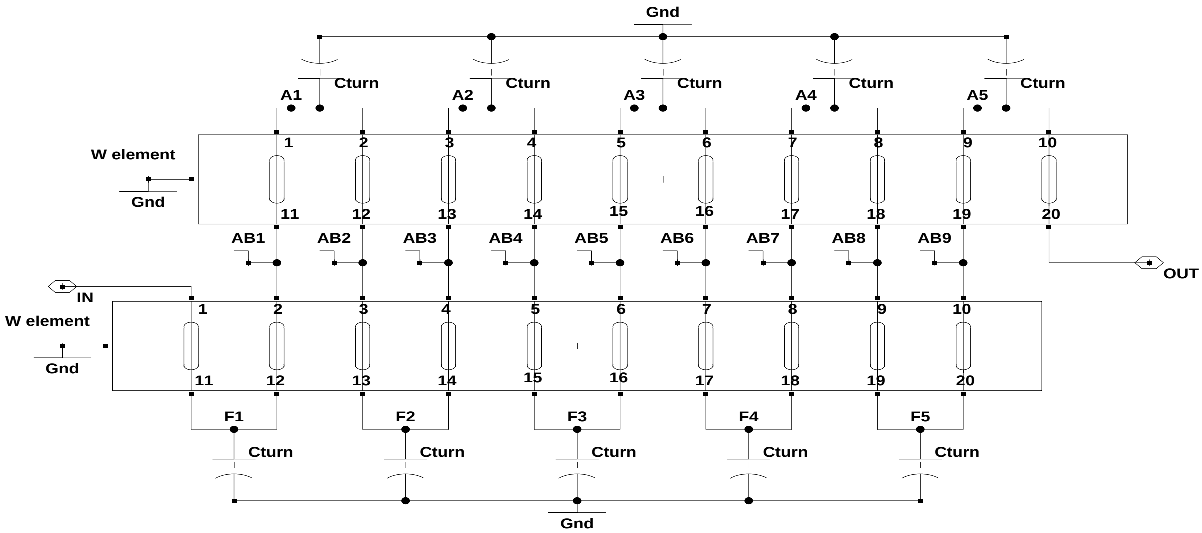

Figure 13: Linked-W Circuit Model for Meander Section

Figure 13 shows the circuit schematic used for this geometry. Each box is a 10-signal-conductor W element. A signal enters at terminal “IN,” crosses the lower W element on one of the signal conductors, then is fed into the neighboring signal conductor.

Table 2 lists the parameters which must be specified to construct the model [6]. In the rest of this section we will show how the value of each parameter was found or estimated.

Table 2: Linked-W Model Parameters

Parameter	Description	Value	Units
N	Number of parallel conductors	10	Dimensionless
L	Length of wire represented by each section	0.00254	m
L matrix	Inductance matrix[8]	See Appendix A	H/m
C matrix	Capacitance matrix	See Appendix A	F/m
R matrix	DC Resistance matrix	See Appendix A	Ω/m
G matrix	Dielectric Conductance matrix	See Appendix A	S/m
R_S matrix	Skin effect coefficient matrix	See Appendix A	$\frac{\Omega}{m\sqrt{Hz}}$
C_{turn}	Lumped capacitance at wire turns	$29x10^{-15}$	F

Looking at Figure 12, it is clear that each dashed rectangle contains ten signal conductors, so N=10.

The total length of our meander line is 50.8 mm, and each W element accounts for half of that length, so L=(50.8 mm)/2N, or 2.54 mm.

C_{turn} was estimated to be 17fF from a three-dimensional field solution, and estimated to be 40fF using formulas in [7]. We used the average value, 29fF. Of course, no lumped turn capacitance was used in the straight-line model.

The R, L, G, and C matrices are generalizations of the *R*, *L*, *G*, and *C* terms introduced in Section 2.2 for lines with multiple conductors. The matrices can be obtained by a two-dimensional field solution. MAXWELL/HFSS version 7.0 [8] was used to generate RLGC matrices based on our board geometry, shown in Figure 7.

The difficulty in constructing one of these models is in how much coupling to allow. MAXWELL generates an RLGC file suitable to be imported to HSPICE. The simulator, however, does not have any concept of the time it takes a field to propagate between lines, so it does not consider the fact that lines 1 and 10 (referring to Figure 7) are 9*d* apart. Light takes over 20 ps (for *d*=15 mils) to travel that far. Yet an HSPICE simulation may be done with a timestep of 2 ps, which will show a voltage on line 10 induced by the current on line 1 with no time delay.

To solve this problem, we hand-edited the matrices produced by MAXWELL and removed the terms which cause faraway coupling by setting them to zero. We decided to allow instantaneous coupling between conductors only up to a distance of 2*d*. This means keeping the diagonal matrix terms and the closest two off-diagonals.

The RLGC files used for the 15-mil, 10-mil, and straight line models are included in Appendix A. We have made the following modifications to the matrices produced by MAXWELL:
1. Deletion of matrix terms outside the diagonal and closest two off-diagonal terms. This was done to limit faster-than-light coupling.
2. Deletion of all off-diagonal resistance terms.
3. Setting diagonal skin effect terms to a common value. MAXWELL produced a different value for R_s for the meander lines and the straight line. To our knowledge, there is no physical reason for a difference in skin effect here, so we set all the terms to the same value.

5.2 Time-Domain Transmission in Linked-W Model

Figure 14 shows the simulated time-domain transmission results that correspond to those shown in Figure 8. Likewise, Figure 15 corresponds to Figure 11. For reference, Figures 8 and 11 are reprinted.

The simulations were done with a 50-ps-risetime step.[1]

5.3 Discussion of Linked-W Model

Our model predicts the time delay reduction effect and the approximate magnitudes of the reductions. However, there is not perfect agreement between simulation and measurement. It

1. A 50-ps step was used rather than the 38-ps step of the real test equipment to account for risetime degradation due to connector losses.

should also be noted that all model parameters only consider geometry. We did not use any empirical adjustments.

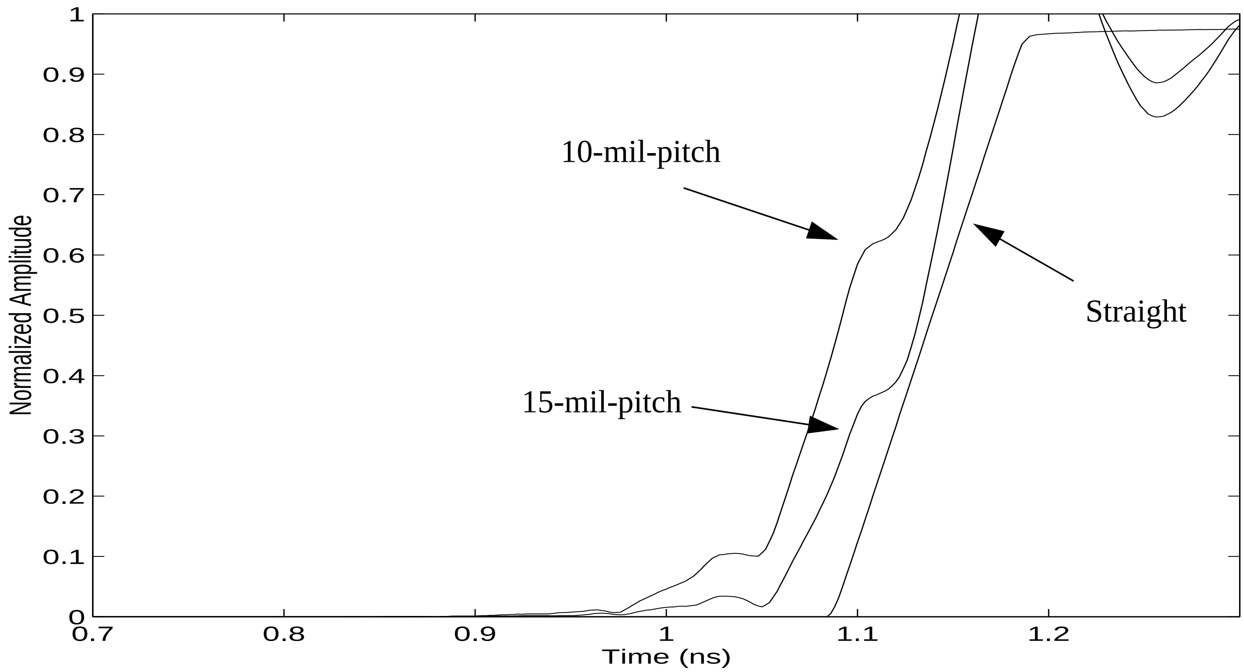

Figure 14: Simulated Time-Domain Transmission

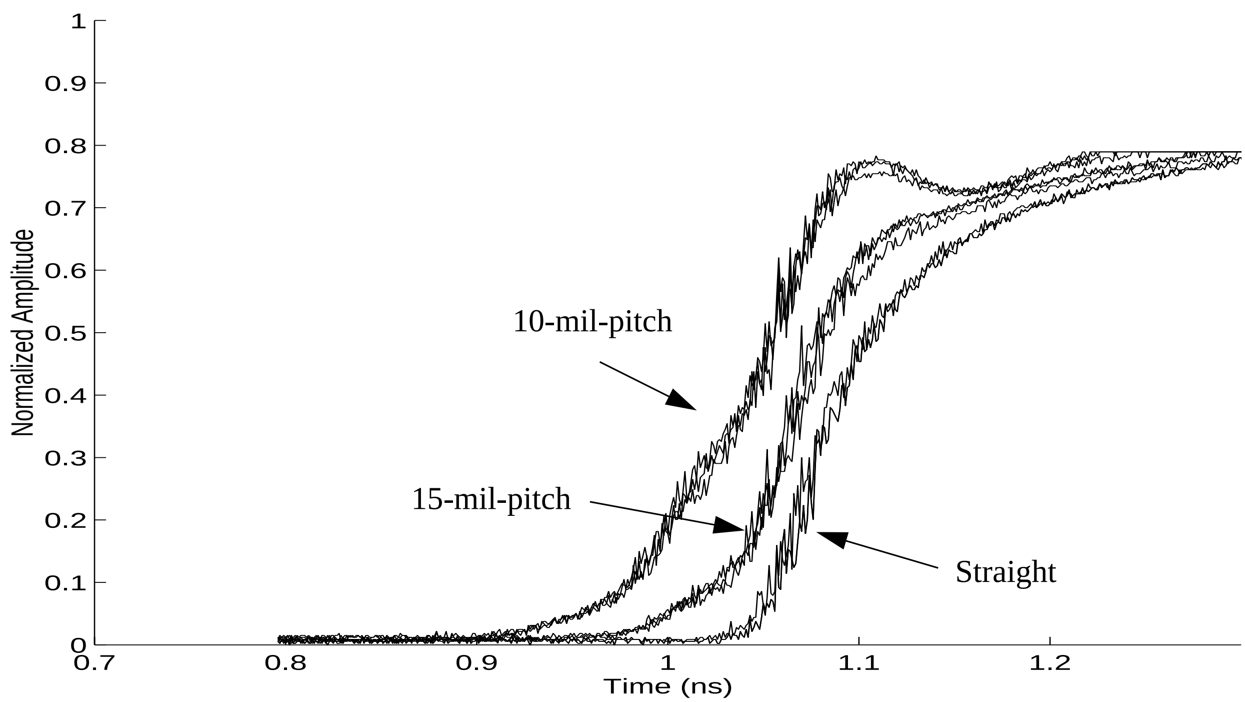

Figure 8 (repeat): Measured Time-Domain Transmission

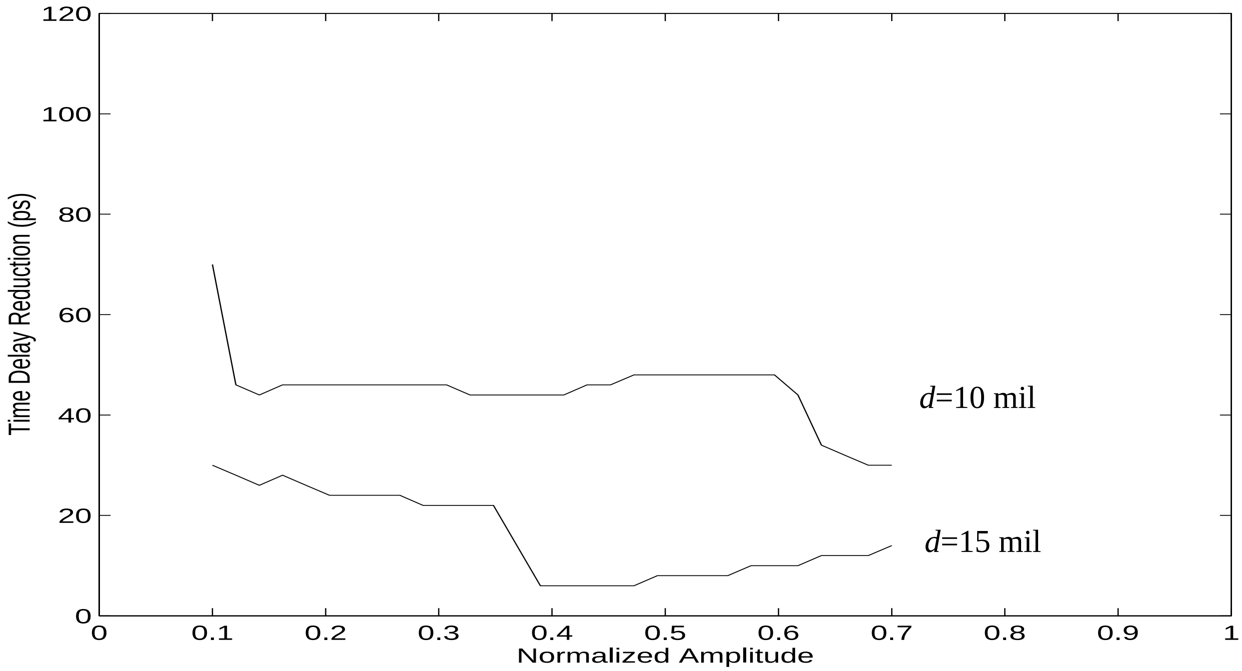

Figure 15: Simulated Reduction Chart

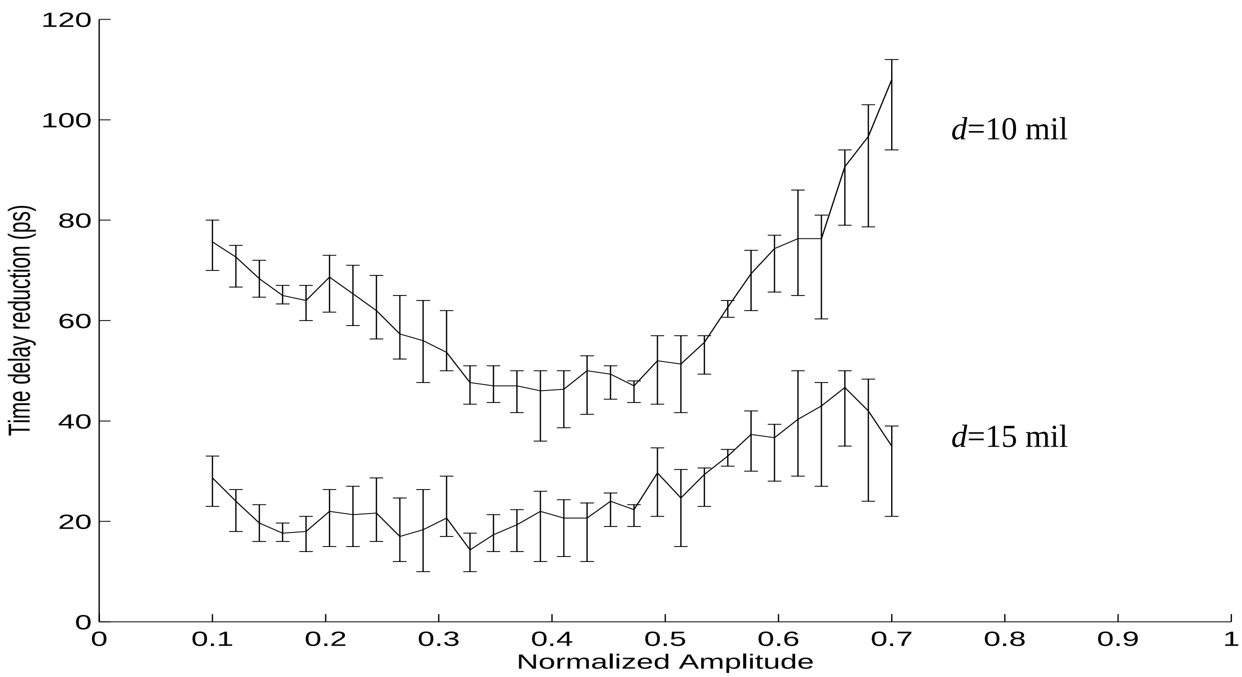

Figure 11 (repeat): Measured Time Delay Reduction

6.0 Conclusions

Measurements have been presented in time and frequency domains for meandering lines on a printed circuit board. Coupling between segments of the meander line causes a significantly smaller time delay through that section than if it had been straight. The difference in delays can be on the order of tens of picoseconds and could be important in circuits with small timing margins. In fact, time delay reduction due to meander lines is always critical, since meander lines are only used on traces with matched delays.

Meandering does not have any apparent effect on the characteristic impedance and attenuation of the line.

We have presented a method of modelling the time delay reduction effect by linking together W elements in HSPICE, based on parameters from a 2-dimensional field solution.

7.0 Acknowledgements

The authors would like to thank Hans Eberle and Russell Kao for reviewing the report and providing many helpful comments. The authors would also like to thank Cameron Barfield for technical assistance.

8.0 References

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[8] Ansoft Corporation, *Maxwell 2D Extractor Manual*, 1999.

Appendix A: Modified RLGC Files

A.1 Straight line (1 conductor)

```
* BEGIN ANSOFT HEADER
* node 1 sig5_A
* node 2 Ground_A
* node 3 sig5_B
* node 4 Ground_B
*   Format: HSPICE W Element
*   Length: 5.08E-08 meters
*   T_Rise: 1E-10 seconds
*    Model: Distributed Lossy Transmission Line
* Project: str_st
*      Cap: /home/sdpowers/Maxwell/default/getstart/str_st.pjt/es.pjt/es.cap
*      Imp: /home/sdpowers/Maxwell/default/getstart/str_st.pjt/ed.pjt/ed.prz
* END ANSOFT HEADER

* N (number of signal conductors)
********************************
1

* Lo
********************************
   3.465089513201419e-07

* Co
********************************
   1.462881467579594e-10

* Ro
********************************
       9.639797604641265

* Go
********************************
                       0

* Rs
********************************
    0.000268

* end of file
```

A.2 15-mil-pitch line (10 conductors)

```
* 30 August 2000 SDP

* N (number of signal conductors)
********************************
10

* Lo
********************************
   3.978000188843106e-07
   3.459751814200422e-08   3.974867357202248e-07
   2.839707726076615e-08   3.453878165311019e-08    3.97664314599814e-07
   0   2.850152755743982e-08   3.454455462013588e-08    3.97349030656235e-07
   0   0   2.848237095558171e-08   3.457529655995407e-08   3.976189963940695e-07
   0   0   0   2.847260444356216e-08   3.459393871320488e-08   3.972074355881755e-07
   0   0   0   0   2.840893558432792e-08   3.456508927964784e-08   3.977146625088864e-07
   0   0   0   0   0   2.844605521816457e-08   3.457634528927084e-08   3.973688445811604e-07
   0   0   0   0   0   0   2.841228903817922e-08   3.455425206233288e-08     3.9778506799773e-07
   0   0   0   0   0   0   0   2.829566683836047e-08   3.455304887816948e-08   3.981240525700018e-07

* Co
********************************
   1.513356708521982e-10
 -9.826693708693645e-12   1.536525963616726e-10
 -7.180554575146058e-12 -9.739205099561922e-12   1.520393658761986e-10
```

```
   0   -7.27972061075645e-12 -9.779520638663971e-12   1.540406957082853e-10
   0   0 -7.099511963761053e-12 -9.787045265776113e-12   1.523321850652039e-10
   0   0   0 -7.304304581486275e-12   -9.80795524075891e-12   1.543120509113623e-10
   0   0   0   0 -7.087437837999916e-12 -9.723075591269848e-12   1.517133955572949e-10
   0   0   0   0   0 -7.339544008271266e-12 -9.801837140012699e-12   1.546393173053052e-10
   0   0   0   0   0   0 -7.064805780910984e-12 -9.763067320436035e-12   1.518389732756162e-10
   0   0   0   0   0   0   0 -7.471251697816697e-12 -9.874478457298695e-12   1.542690755224136e-10

* Ro
********************************
       9.639797604641792
0       9.639797604642132
0 0       9.639797604642581
0 0 0       9.639797604641217
0 0 0 0       9.639797604641432
0 0 0 0 0       9.63979760464151
0 0 0 0 0 0       9.639797604641194
0 0 0 0 0 0 0       9.639797604641632
0 0 0 0 0 0 0 0       9.639797604641794
0 0 0 0 0 0 0 0 0       9.639797604642347

* Go
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* Rs
********************************
```

```
   0.000268
0   0.000268
0 0   0.000268
0 0 0   0.0002683
0 0 0 0   0.0002683
0 0 0 0 0   0.000268
0 0 0 0 0 0   0.000268
0 0 0 0 0 0 0   0.0002681
0 0 0 0 0 0 0 0   0.000268
0 0 0 0 0 0 0 0 0   0.000268

* end of file
```

A.3 10-mil-pitch line (10 conductors)

```
* section10_10.rlgc
* 30 August 2000 SDP

* N (number of signal conductors)
********************************
10

* Lo
********************************
   3.975032886313612e-07
   5.300890036796857e-08   3.974891780778403e-07
   3.022502612572039e-08   5.301347732932887e-08   3.972818349088896e-07
   0   3.022988166983593e-08   5.299895087440138e-08   3.975929303521778e-07
   0   0   3.031466361275415e-08   5.301399359509427e-08   3.973483769216797e-07
   0   0   0   3.022142790285396e-08   5.299978957209532e-08   3.975784279014101e-07
   0   0   0   0   3.018427540255959e-08   5.296679259825262e-08    3.97401329438346e-07
   0   0   0   0   0   3.022174917830365e-08   5.299701305489592e-08   3.973863289117837e-07
   0   0   0   0   0   0   3.026787489958043e-08   5.299930688579718e-08   3.976700843000904e-07
   0   0   0   0   0   0   0   3.022509167278706e-08   5.300689317596155e-08   3.980838751849757e-07

* Co
********************************
    1.52964401425452e-10
 -1.796896028774361e-11   1.575985578499609e-10
 -6.507841630944313e-12 -1.733865876121427e-11   1.543727869704399e-10
   0   -6.24243511617727e-12 -1.708643613870431e-11   1.549883830262787e-10
   0   0   -6.05719602092117e-12 -1.699838039651984e-11   1.542721070797919e-10
   0   0   0 -6.194211469986304e-12 -1.731095841322729e-11   1.564139968234101e-10
   0   0   0   0 -6.069109642869945e-12 -1.716398112328102e-11   1.545560844790896e-10
   0   0   0   0   0 -6.203286383554278e-12 -1.718412403061199e-11     1.5546478956334e-10
   0   0   0   0   0   0 -6.073353856536537e-12 -1.704742678159788e-11   1.542331506185294e-10
   0   0   0   0   0   0   0 -6.750337266382617e-12   -1.77640963841799e-11    1.57006434576901e-10

* Ro
********************************
      9.639797604641998
     0       9.639797604641977
     0 0       9.639797604642631
     0 0 0       9.639797604641402
     0 0 0 0       9.639797604641119
     0 0 0 0 0       9.639797604641419
     0 0 0 0 0 0       9.639797604641409
     0 0 0   0 0 0 0       9.639797604641807
     0 0 0 0 0 0 0 0       9.639797604642393
     0 0 0 0 0 0 0 0 0       9.639797604642123

* Go
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* Rs
********************************
   0.000268
   0   0.000268
   0   0   0.000268
   0   0   0   0.000268
   0   0   0   0   0.000268
   0   0   0   0   0   0.000268
   0   0   0   0   0   0    0.000268
   0   0   0   0   0   0    0    0.000268
   0   0   0   0   0   0    0    0   0.000268
   0   0   0   0   0   0    0    0   0   0.000268

* end of file
```

About the Authors

Scott D. Powers was an Intern at Sun Microsystems Laboratories during the summer of 2000. He received the Bachelor of Science degree (summa cum laude) in electrical engineering from Washington University in St. Louis in 1999. He is currently a Ph.D. candidate in electrical engineering at Stanford University. Mr. Powers is a student member of IEEE and a member of Tau Beta Pi.

Jose M. Cruz is a Member of the Technical Staff at Sun Microsystems Laboratories, where he is doing research in radio-frequency circuits and networking. He received the Master of Engineering degree, with high distinction, from the University of Leuven, Belgium, and the M.S. and Ph.D. degrees in Electrical Engineering and Computer Sciences from the University of California at Berkeley. He has worked in the fields of Circuit Theory and Integrated Circuit Design. He has co-authored several journal papers, book articles, patents, and conference papers. He has been a member of the Technical Program Committee for the Custom Integrated Circuits Conference for the years 1999 and 2000.