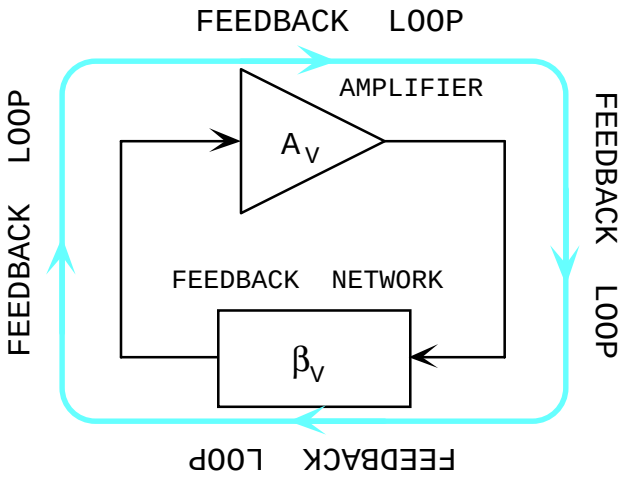
SINEWAVE OSCILLATORS

1. OSCILLATION MECHANISM



An amplifier with feedback is shown above. A_V and β_V are normally frequency dependant gains which have complex values - magnitude and phase or real and imaginary parts. At some frequency feedback can become re-generative (an initial train of oscillations will be regenerated by the feedback loop) if phaseshift introduced by A_V and β_V becomes 360° and the loop may produce sustained sinewave oscillations.

BARKHAUSEN OSCILLATION CRITERION

1. Transient starting condition

Upon application of power to the oscillator circuit, the output amplitude is 0V, therefore one must initiate the oscillations by injecting some energy at some point in the circuit - this is usually done by inputing a single pulse at the appropriate point. Once the oscillations have started, their amplitude must grow until it reaches the desired level and then stay constant. For this to happen, the loop gain must be greater than $1\angle 0°$ initially.

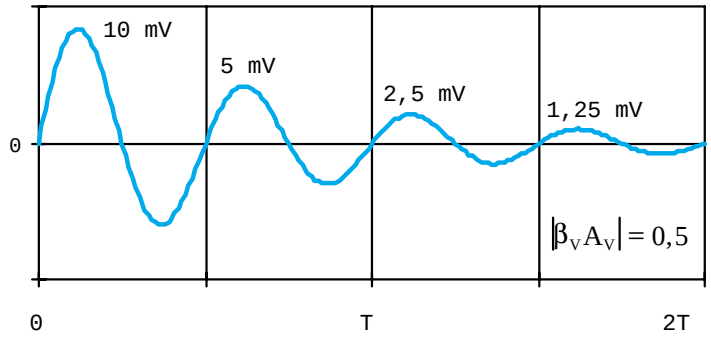
Loop gain $L(S) = \beta_V A_V \rangle 1\angle 0°$ for growing oscillations

2. Steady state running condition

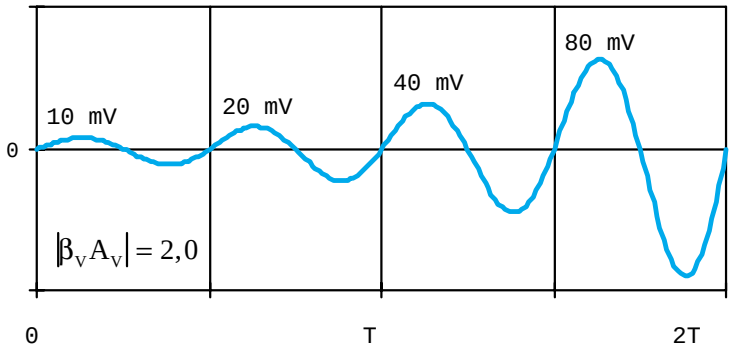
Once the oscillations have reached the desired level, the loop gain must be exactly $1\angle 0°$ to maintain constant amplitude oscillations. The oscillations will occur at the frequency where the phaseshift of the loop gain is exactly 0° or ±N x 360°.

Loop gain $L(S) = \beta_V A_V = 1\angle 0°$ for constant amplitude oscillations

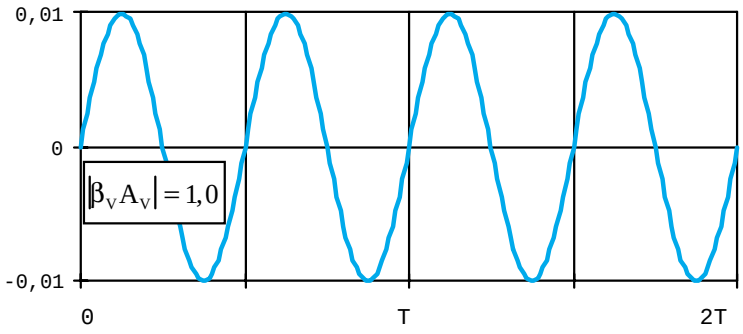
Frequency F_{OSC} where $\hat{L}(S) = \pm N \times 360°$ where N = 0, ±1, ±2, ±3, etc.

LOOP GAIN	OUTPUT WAVEFORM
CASE#1 De-generative feedback $\lvert L(j\omega)\rvert < 1$ $\hat{L}(j\omega) = \pm 360^\circ$ Decreasing amplitude, oscillations are damped. This is the condition desired for a stable amplifier, the faster the oscillations are damped (less loop gain), the more stable the amplifier is.	

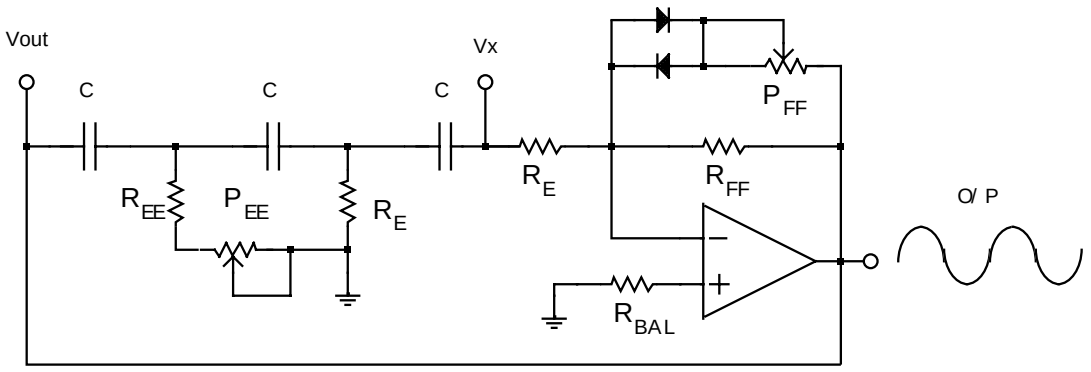
Let's assume $\lvert\beta_V A_V\rvert = 0,5$ and that a 10 mV_P sinewave is initiated at the output. Every time the oscillation goes around the loop it will be amplified by a loop gain of 0.5, or attenuated 2 times (i.e. attenuation = 1 / gain (v/v) or attenuation (dB) = -gain (dB)). Therefore the output sinewave will be damped out and will not be sustained

CASE#2 Re-generative feedback $\lvert L(j\omega)\rvert > 1$ $\hat{L}(j\omega) = \pm 360^\circ$ Increasing amplitude until non-linearity of circuit limits the amplitude or saturation of circuit occurs - sustained oscillations. Oscillator startup - the larger the loop gain is, the faster the oscillations grow.	

Assuming a loop gain of two, the amplitude doubles every time they go around the loop, therefore the amplitude grows exponentially until non-linearity or saturation limits the amplitude.

CASE#3 Re-generative feedback $\lvert L(j\omega)\rvert \equiv 1$ $\hat{L}(j\omega) = \pm 360^\circ$ Constant amplitude, sustained oscillations. Oscillator has reached a steady state operation. The oscillations are amplified by a gain of 1 every time they go around the loop, therefore their amplitude stays perfectly constant.	

2. PHASESHIFT OSCILLATOR



Description

This circuit provides a low-frequency sinewave with a THD around 0,2% for large amplitudes and a THD around 2% for small amplitudes. The frequency can be trimmed within a narrow range but this will also vary the output amplitude which can be re-adjusted with P_{FF}. Amplitude is adjustable.

Diodes: form a non-linear resistor that will stabilise the loop gain to one when the amplitude of the oscillations has reached the proper level.

P_{FF} : adjustment of the output amplitude.

P_{EE}: trimming of the frequency of oscillation - narrow range.

R_E and C: determine the frequency of oscillation

R_F and R_E: determine the gain of the inverting amplifier, that is $A_V = -R_F/R_E$.

Loop gain and frequency of oscillation

$$L(S) = \beta_V A_V = \left(\frac{(SRC)^3}{(SRC)^3 + 6(SRC)^2 + 5(SRC) + 1} \right) \times \left(-\frac{R_F}{R_E} \right) \qquad \text{where} \quad R_F = R_{FF} \| (P_{FF} + r_d)$$

If we replace S with jω and simplify, we obtain:

$$L(j\omega) = \left[\left(1 - \frac{5}{(\omega RC)^2} \right) - j \left(\frac{6}{(\omega RC)} - \frac{1}{(\omega RC)^3} \right) \right]^{-1} \times \left(-\frac{R_F}{R_E} \right) = 1 \angle 360^\circ$$

real imaginary $\angle 180^\circ$

The first term must have an angle of 180° for a total of 360° and this will occur only if its imaginary part is zero and its real part is negative.

$$\left(\frac{6}{(\omega RC)} - \frac{1}{(\omega RC)^3} \right) = 0 \quad \Rightarrow \quad \omega_n = \left(\sqrt{6} \times R_E C \right)^{-1} \quad \Rightarrow \quad L(j\omega_n) = \left[-\frac{1}{29} \right] \times \left(-\frac{R_F}{R_E} \right)$$

Practical considerations

Starting conditions:

V_{out} low amplitude, diodes are OFF.
$R_F = R_{FF} \parallel \infty$, therefore make $R_F > 29\ R_E$ for a loop gain > 1. Use a loop gain of at least 1,5 to ensure proper start of oscillations.

$$L(j\omega_n) = \left[-\frac{1}{29}\right] \times \left(-\frac{R_{FF}}{R_E}\right) \rangle 1{,}5$$

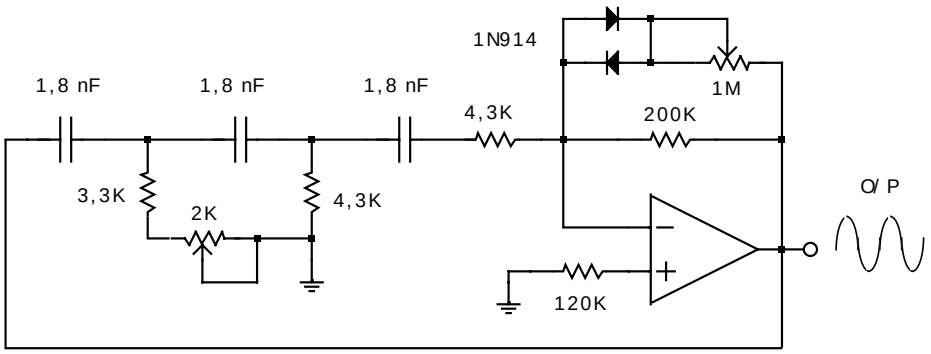
V_{out} large amplitude, diodes are ON.
$R_F = R_{FF} \parallel (P_{FF} + r_d)$ therefore make $R_F = 29\ R_E$ for a loop gain = 1. Assuming that the diodes resistance is negligible, aim for an approximate pot setting of $P_{FF} / 3$.

$$R_F = 29R_E = R_{FF} \parallel (P_{FF} / 3)$$

Design example

Design a phaseshift oscillator with a frequency of 10 kHz. Frequency should be trimmable because frequency determining components have % tolerances.

Final circuit

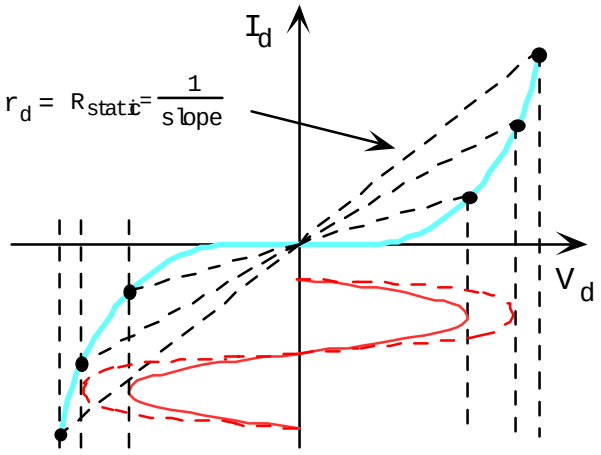


Loop Gain Stabilisation

The diodes are non-linear and can be represented as a non-linear resistor. As the amplitude of the output sinewave increases, the diodes will conduct more current and their static resistance will decrease as shown beside. The final amplitude of the signal will stabilise when the diode resistance makes the loop gain exactly equal to one,

that is $$R_{FF} \parallel (P_{FF} + r_d) = 29R_E$$

$$\beta_V A_V = \beta_V \left(-\frac{R_{FF} \parallel (P_{FF} + r_d)}{R_E}\right)$$



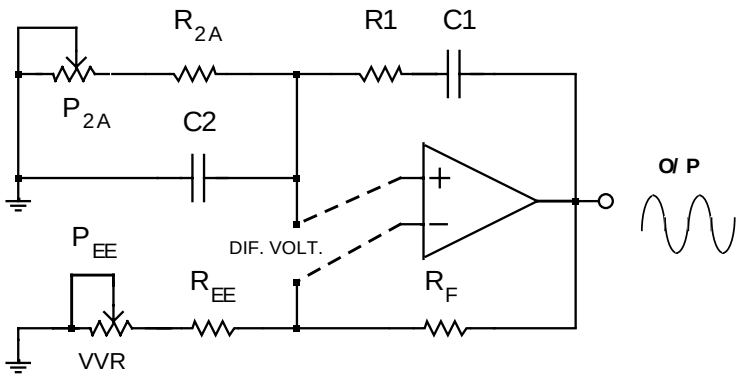
Back to back diodes characteristics

3. BASIC WIEN BRIDGE OSCILLATOR

Basic circuit

$R_2 = R_{2A}+P_{2A}$ $R_E = R_{EE}+P_{EE}$

R_1C_1 and R_2C_2 form a frequency dependant voltage divider that feeds the output back to V^+ of the op amp which amplifies V^+ by the non-inverting gain of $1+R_F/R_E$. Since the non-inverting gain has a phaseshift of 0°, the circuit will oscillate when V^+ is in phase with the output.



The VVR is a voltage variable resistor that is used to adjust the loop gain automatically to one when it is used in an AGC loop (Automatic Gain Control). The AGC loop will generate the proper DC voltage that will set the VVR resistance to its desired value.

Loop gain

$$L(S)=\beta_V A_V=\left(\frac{\frac{S}{R_1C_2}}{S^2+\left(\frac{1}{R_1C_1}+\frac{1}{R_2C_2}+\frac{1}{R_1C_2}\right)S+\frac{1}{R_1C_1R_2C_2}}\right)\times\left(1+\frac{R_E}{R_E}\right)$$

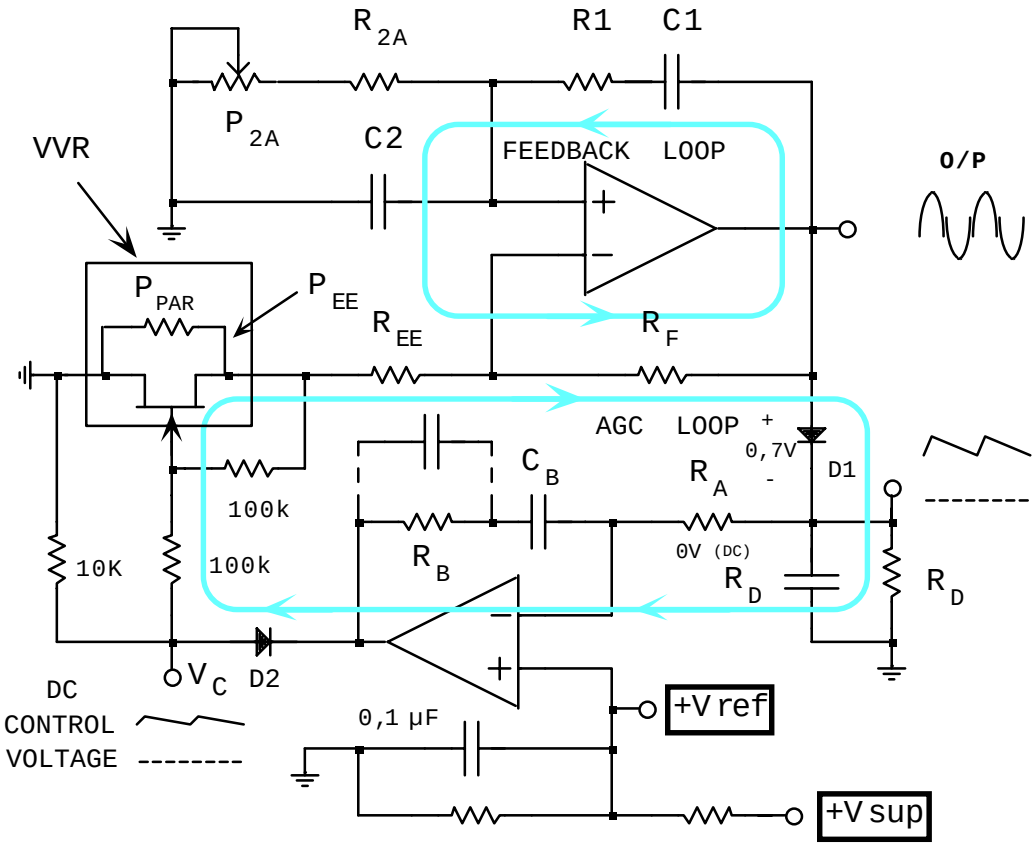
$\beta_V = V^+/V_{OUT}$

Replacing S with jω we obtain the loop gain L(jω) as a function of frequency. One can show that the loop gain will have a phase angle of 0° at the following frequency:

$$\omega_n=\frac{1}{\sqrt{R_1C_1R_2C_2}} \quad where \quad \beta_V A_V=\left(1+\frac{R_1}{R_2}+\frac{C_2}{C_1}\right)^{-1}\times\left(1+\frac{R_F}{R_E}\right)$$

The circuit will oscillate at ω_n if the loop gain is appropriate and the starting conditions are respected.

Actual circuit



Description of AGC loop

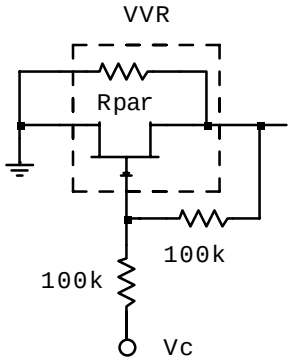
The envelope detector produces a DC voltage that is approximately equal to the peak O/P voltage minus the 0,7V lost across the diode - this assumes negligible ripple voltage across C_D.

$$\Delta V_D \approx \frac{V_{O(peak)} - 0,7}{R_D C_D F}$$

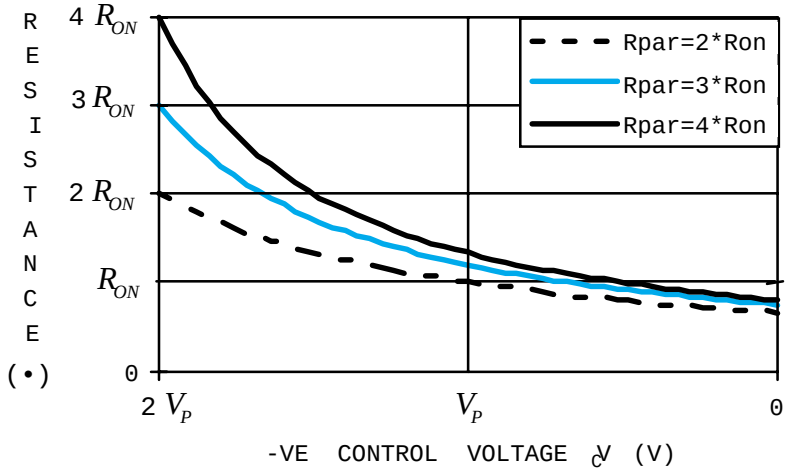
The reference op amp is actually an error amplifier which generates the proper V_C to correct the output amplitude. $V_C = A_d \times V_d = A_d (V_{REF} - (V_{oP} - 0,7))$. V_d is very small since A_d of op amp is very large. *If* $V_{OP}\downarrow$, *then* $V_d\uparrow, V_C\uparrow, R_{EQ}\downarrow$ *and* $A_V\uparrow$, *which increases* V_{OP} that will stabilise at V_{REF} -0,7.

The error amp will force the two inputs equal, that is $V_D(DC) = V_{REF}$. Notice that there is no DC current through R_A , therefore 0V DC across it. R_A, R_B and C_B stabilise the AGC feedback loop and determine the speed of this loop - that is $\tau = R_A C_B$. For a stable AGC loop, make $R_A C_B < R_D C_D/25$ and do not choose $R_D C_D$ too large. Also make $(2\pi R_B C_B)^{-1} < F_{osc}$ to make $A_V(AC) = -R_B/R_A$ at ripple frequency.

The diode at the O/P of the error amp prevents positive voltages to appear on the gate of the JFET because forward biasing of the gate-channel junction is a NO NO. At start up V_{OP} is 0V, $V_2^- = 0V$, $V_2^+ = V_{REF}$ which will saturate the error amp O/P positively, D2 will be OFF and V_C = 0V and $R_{EQ} = R_{ON} \| R_{PAR}$ which will cause maximum loop gain to build up O/P amplitude until V_{OP} - 0,7 surpasses V_{REF} , then V_d becomes negative and D2 will turn ON and V_C will go negative to increase R_{EQ} and reduce the loop gain to stabilise the O/P amplitude.



JFET-VVR characteristics



$$r_{ds} \approx \frac{R_{ON}}{1-\frac{V_C}{2V_P}} \Rightarrow R_{EQ} = R_{PAR} \| r_{ds}$$

R_{ON}: JFET channel ON resistance V_P: channel pinchoff voltage
For an N channel JFET both V_C and V_P must be negative (for P-JFET, both positive)

R_{EQ} in the above expression assumes that the two 100K resistors are much larger than $R_{PAR} \| r_{ds}$.
The two 100K resistors provide 50% feedback (optimum %) from the drain to the gate in order to reduce the distortion introduced by the non-linear resistance of the JFET channel. It can also be shown that minimum distortion is obtained if we bias the JFET at $V_{GS} = V_P/2$ or $V_C = V_P$. The lower the AC signal across drain and source, the less distortion is encountered. JFETs with larger V_P values will produce less distortion with same amplitude AC signals.

DESIGN EXAMPLE: Design a Wien bridge oscillator that produces a 5 kHz/4V_P sinewave with a THD less than 0,1%. Frequency must be trimmable. Use a 2N5459 as the VVR : V_P = -5.8V, I_{DSS} = 9 mA, $r_{ds(ON)}$=500Ω (typical values)

1. Calculation of R_E and R_F for low THD and loop gain variation

   For $C_1 = C_2$, we have:

$$\beta_V A_V = \frac{\left(1+\frac{R_F}{R_E}\right)}{\left(1+\frac{R_1}{R_2}+\frac{C_2}{C_1}\right)} = \frac{\left(1+\frac{R_F}{R_{E(VAR)}}\right)}{\left(2+\frac{R_1}{R_{2(VAR)}}\right)} = 1\angle 0^o$$

$R_E = r_{ds} \| R_{PAR}$ is controlled by V_C where r_{ds} ranges from R_{ON} to ∞. Let us pick a 4 to 1 variation in R_E to accommodate tolerances of the components and trimming of R_2 and still keep the loop gain at 1.

R_E ranges from $R_{ON} \| R_{PAR}$ to R_{PAR} that is $\frac{R_{E\,max}}{R_{E\,min}} = \frac{R_{PAR}}{R_{PAR} \| R_{ON}} = 1+\frac{R_{PAR}}{R_{ON}} = 4 \Rightarrow R_{PAR} = 3R_{ON}$

R_{PAR} = 3 x 500 = 1,5K therefore $R_{E\,min}$ = 500||1500 = 375 and $R_{E\,max}$= ∞||1500 = 1500

For a good range of L(s) values above and below 1, make $R_E = \sqrt{R_{E_{max}} \times R_{E_{min}}} = \sqrt{375 \times 1500} = 750$ at (L(s)=1, which corresponds to r_{ds} = 1500Ω and

$$V_C = 2V_P\left(1-\left(R_{ON}/r_{ds}\right)\right) = 2\times(-5{,}8)\times\left(1-\left(500/1500\right)\right) = -7{,}73V$$

Let R_F = 10 x R_E = 10 x 750 = 7,5K to keep V^+ and the JFET operating at low v_{ds} =V^+ to keep the distortion down. We sould use v_{ds}< 0,5V if possible to maintain a low THD.

$$V^+ = v_{ds} = V_{out} \times R_E / \left(R_E + R_F\right) = 4\times 750 / \left(750+7500\right) = 0{,}364V_P$$

2. Calculation of R_1, C_1, R_2 and C_2 for frequency and loop gain.

$$\left(1+\frac{R_F}{R_{E(VAR)}}\right)=\left(1+\frac{C_2}{C_1}+\frac{R_1}{R_{2(VAR)}}\right)=\left(2+\frac{R_1}{R_{2(VAR)}}\right) \quad for \quad C_1=C_2 \quad therefore \quad \frac{R_1}{R_{2(VAR)}}=\frac{R_F}{R_{E(VAR)}}-1$$

$$\frac{R_1}{R_{2(VAR)}}=\frac{7500}{750}-1=9 \quad \Rightarrow \quad R_1=9R_2 \quad \omega_n^2=\frac{1}{R_1R_2C_1C_2}=\frac{1}{9C^2R_2^2} \quad \Rightarrow \quad CR_2=\frac{1}{3\omega_n}$$

$$CR_2=\frac{1}{3\omega_n}=\frac{1}{3\times 2\pi\times 5000}=10{,}61\,\mu s$$ R_2 = 3K, C = 10,61µ/3K = 3,54 nF (3,6 nF std)

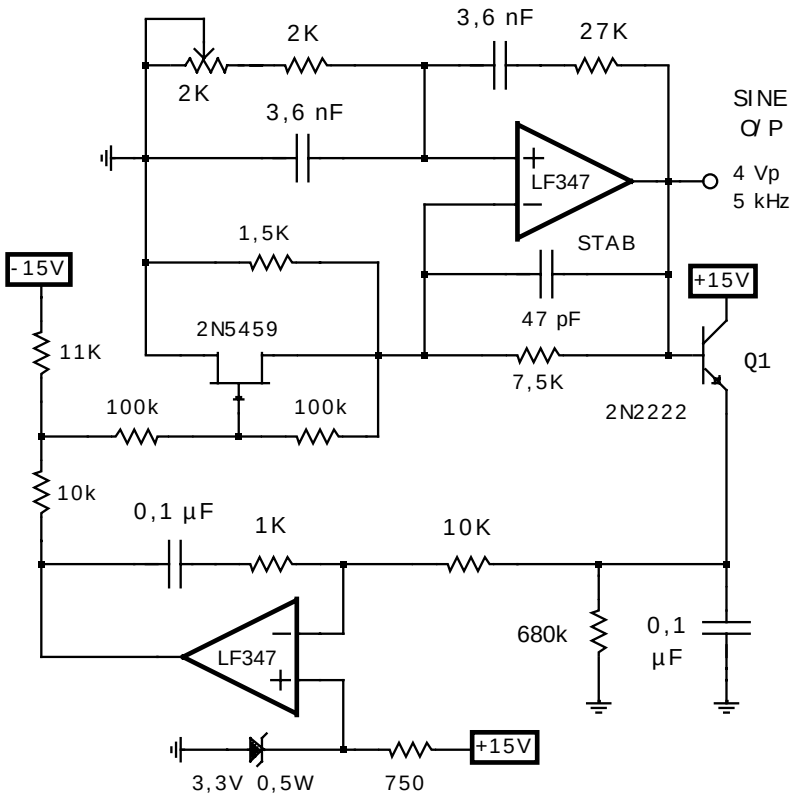
R_1 = 9 * 3K = 27K (std) R_2 = 2K fixed + 2K pot for trimming of frequency.

3. Calculation of R_D, C_D, R_A, R_B and C_B for ripple voltage, time constant and stability

Let the ripple ΔV_d = 10 mV_{pp} for low THD of O/P sinewave:

$$R_DC_D=\frac{V_{REF}}{F\Delta V_{RIP}}=\frac{3{,}3}{5000\times 10m}=66\,ms$$ C_D = 0,1 µF, R_D = 660K (680K std)

$R_AC_B < R_DC_D/25$ = 2,72 ms for a "stable" AGC loop and $(2\pi R_B C_B)^{-1} < F_{osc}$ or $R_B C_B$ > 31,8 µs
Let C_B = 0,1 µF, R_B > 31,8µ/0,1µ = 318 and R_A < 2,72m/0,1µ = 27,2K
Let R_A = 10K and R_B = 1K which will attenuate the ripple 10X going through the error amplifier.



4. Zener Reference

Bias Zener at 10% of $I_z$max, that is I_z= 0,1*0,5W/3,3V =15,15mA to operate past the "knee" of the I-V curve. R_1 = (15-3,3)/15,15m = 772
R_1 = 750std

5. The 10K-11K voltage divider limits V_{GS} to a range of -7,25V to +0,1V typical-assume V_{sat}=±14V

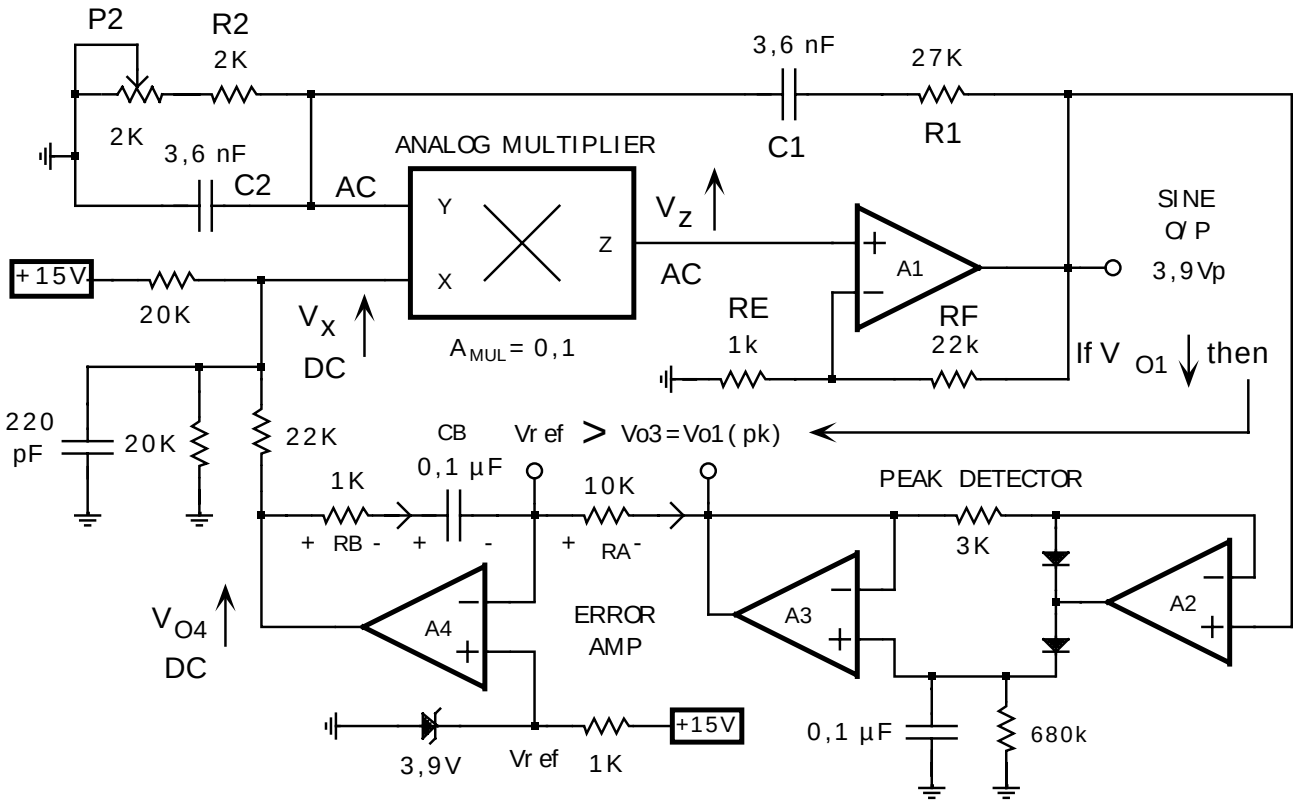
Final Circuit

The AGC loop may not be stable, if this occurs, change time constants R_dC_d and/or R_AC_B for a stable loop.

The design has not been optimised for lowest THD, this can be done by biasing the JFET at $V_{GS} = V_p/2$ where r_{ds} = 2 R_{on} - modify R_{par} or R_F to do so.

The 47 pF cap stabilises the upper op amp when Q1 is ON because the 0,1 µF load seen by the op amp de-stabilises -ve feedback . Q1 lessens the capacitive load seen by the op amp O/P by (h_{fe} +1) times which makes it easier to stabilise with a smaller cap (47 pF).

AGC LOOP WITH ANALOG MULTIPLIER



Loop gain

$$L(S)=\beta_V A_V=\left(\frac{\frac{S}{R_1C_2}}{S^2+\left(\frac{1}{R_1C_1}+\frac{1}{R_2C_2}+\frac{1}{R_1C_2}\right)S+\frac{1}{R_1C_1R_2C_2}}\right)\times\left(A_{MUL}V_Y\right)\times\left(1+\frac{R_F}{R_E}\right)$$

$\beta_V = V_X/V_{O1}$

Replacing S with jω we obtain the loop gain L(jω) as a function of frequency. One can show that the loop gain will have a phase angle of 0° at the following frequency:

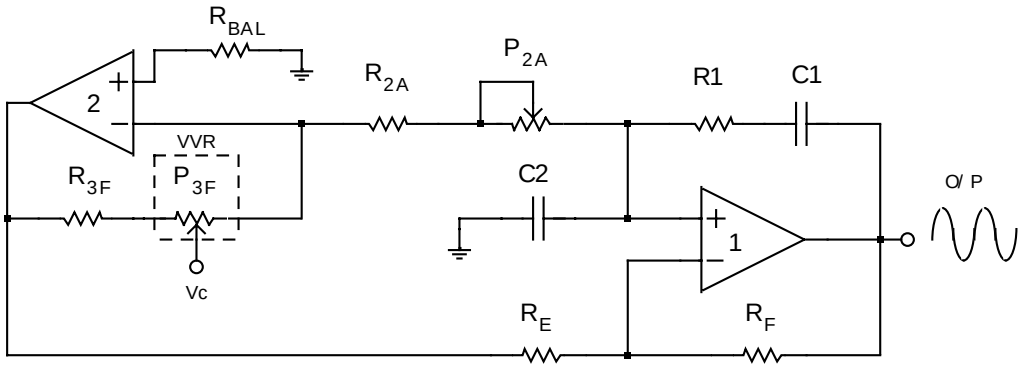
$$\omega_n=\frac{1}{\sqrt{R_1C_1R_2C_2}}\quad where\quad \beta_V A_V=\left(1+\frac{R_1}{R_2}+\frac{C_2}{C_1}\right)^{-1}\times\left(A_{MUL}V_X\right)\times\left(1+\frac{R_F}{R_E}\right)$$

The circuit will oscillate at ω_n if the loop gain is appropriate and the starting conditions are respected. The AGC loop gain is regulated by adjusting V_X which is a DC voltage that sets the AC gain of the analog multipler, that is $V_Z = (A_{MUL}\ V_{X(DC)}) * V_{Y(AC)}$. Now V_x is adjusted automatically such as to force $V^- = V^+$ in op amp A4. $V^- = V_{o1}(pk)$ and $V^+ = V_{ref}$ of the zener diode. If V_{o1} goes down for some reason or another, then $V_{ref} > V_{o1}$ and $I_{RA} = (V_{ref} - V_{o1})/R_A$ will charge C_B up and automatically increase V_{o4} which in turn will increase V_X(DC) and the loop gain will rise above 1V/V thereby increasing V_{o1} until V_{o3} (which equals V_{o1}) reaches the V_{ref} level and knock I_{RA} back to 0A and V_{o1} has stabilised at $V_{o1} = Vref = V_{zener}$. V_X(DC) should be chosen as the midrange value of the V_x range. V_x min should not be too close to 0V because one risks V_x going -ve which would add an extra 180° to the oscillator loop and kill the oscillations right away. The

two 20K and the 22K resistors at the O/P of A4 set the range of V_x to +0,78V to +9,5V assuming V_{sat} = ±14V for A4. The maximum of +9,5V was picked not to go too close to V_x(max) specified for the analog multiplier. Therefore V_x mid = (0,78+9,5)/2 = 5,14V should be used to set the AGC loop gain to 1V/V which results in a loop gain ranging from 0,15 to 1,85 V/V. When V_{o1} is too large one wants a loop gain less than one to lower V_{o1} and when V_{o1} is too small one wants a loop gain greater than one to increase V_{o1}.

4. WIDE RANGE WIEN BRIDGE OSCILLATOR

Basic circuit



P_{2A} allows wide range frequency tuning which cannot be obtained with the basic Wien bridge oscillator because of the loop gain variation occuring when P_{2A} is varied - loop gain variation causes amplitude variation of output and stops the oscillations when loop gain falls below unity.

The above circuit compensates for loop gasin variations encountered in the basic Wien oscillator. As P_{2A} decreases, β_V goes down but op amp #2 amplifies the feedback voltage ($V_1^- = \beta_V V_{o1}$) by a gain of $A_{V2} = -R_3/R_2$ which increases as $R_2 = R_{2A} + P_{2A}$ goes down thus keeping the loop gain constant in spite of R_2 variations.

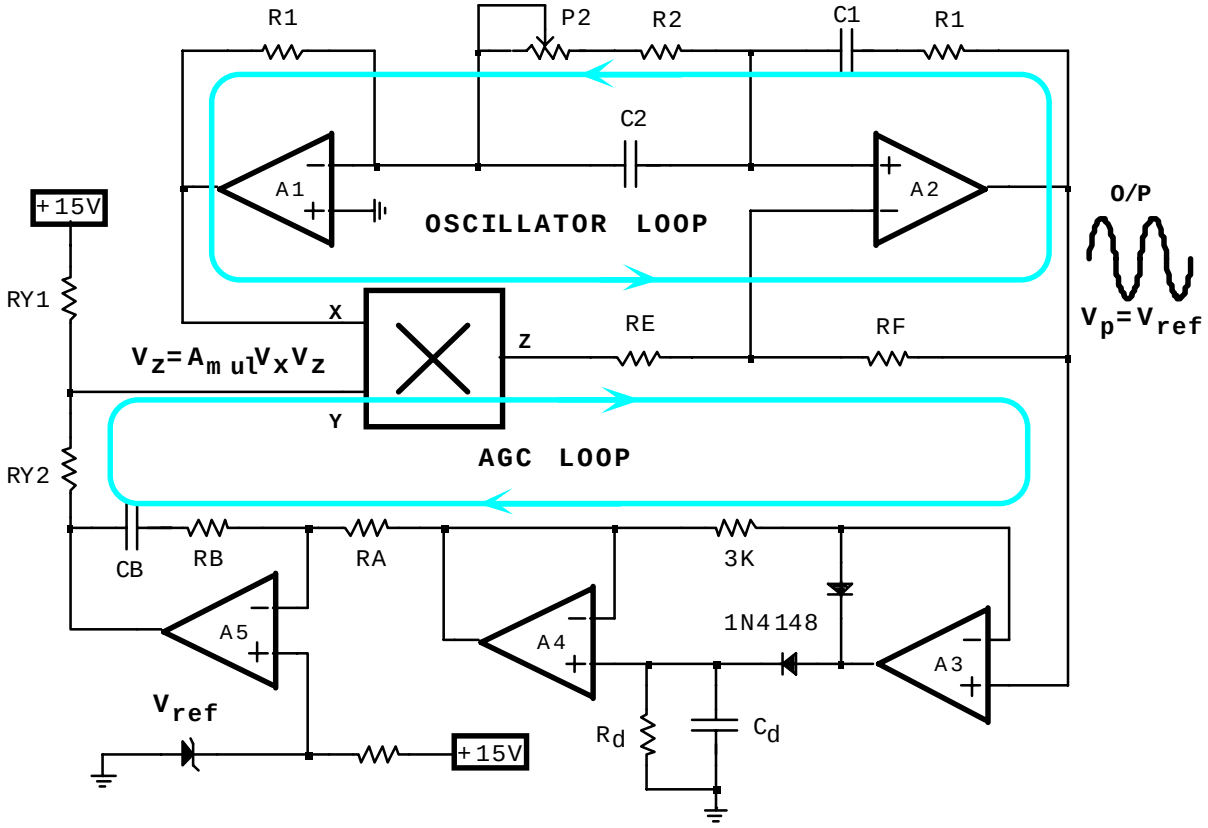
$$L(S) = \beta_V A_V = \left(\frac{\frac{S}{R_1 C_2}}{S^2 + \left(\frac{1}{R_1 C_1} + \frac{1}{R_2 C_2} + \frac{1}{R_1 C_2} \right) S + \frac{1}{R_1 C_1 R_2 C_2}} \right) \times \left[1 + \left(\frac{R_F}{R_E} \times \left(1 + \frac{R_3}{R_2} \right) \right) \right] \qquad \beta_V = V_1^+ / V_{O1}$$

Replacing S with jω we obtain the loop gain L(jω) as a function of frequency. One can show that the loop gain will have a phase angle of 0° at the following frequency:

$$\omega_n = \frac{1}{\sqrt{R_1 C_1 R_2 C_2}} \quad where \quad \beta_V A_V = \left(1 + \frac{R_1}{R_2} + \frac{C_2}{C_1} \right)^{-1} \times \left[1 + \left(\frac{R_F}{R_E} \times \left(1 + \frac{R_3}{R_2} \right) \right) \right]$$

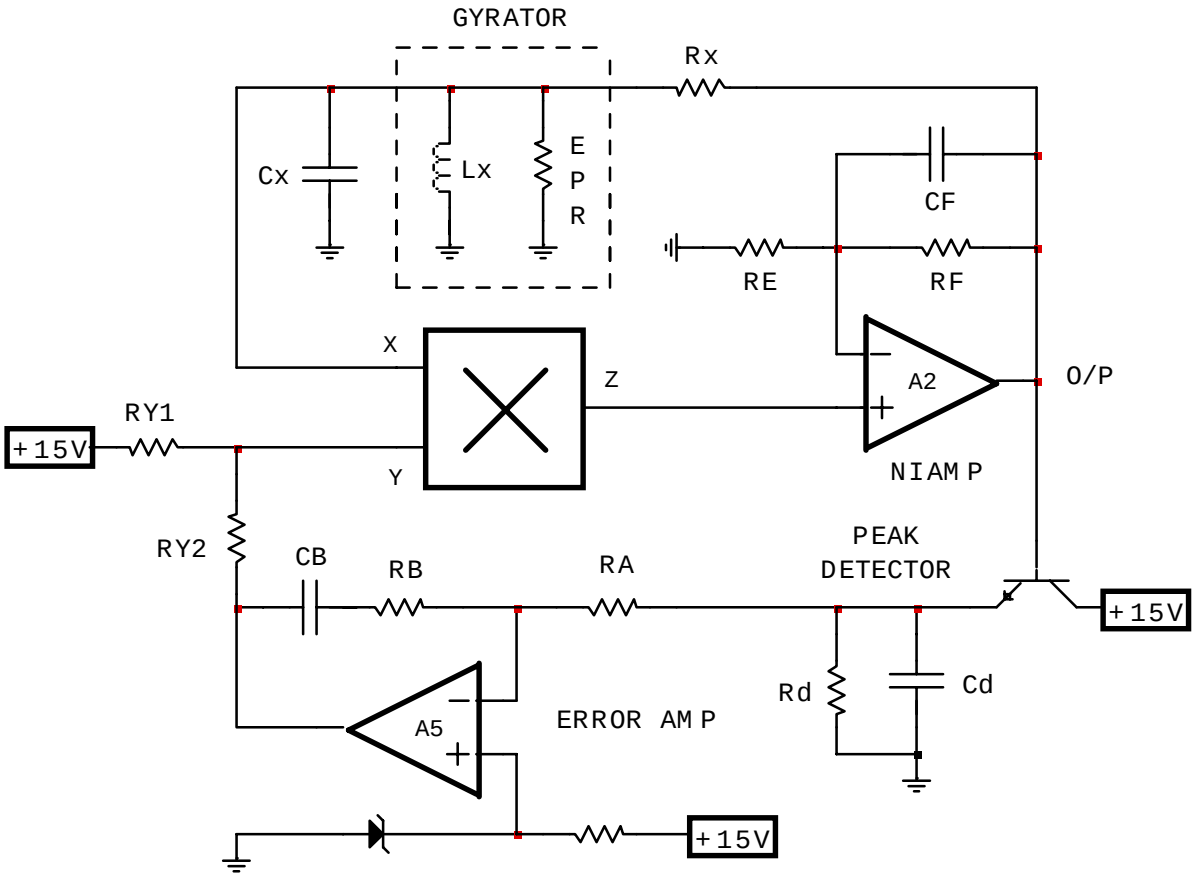
To simplify the design, make $C_1 = C_2$ and $R_E = R_F$, then you find that for a loop gain of one, one must have $R_3 = R_1$.

Practical Wien bridge circuit with AGC loop



NOTE: The output sinewave has a very low THD (< 0,05%) that depends mainly on the linearity of the analog multiplier which usually exhibits better linearity with smaller signals. The second factor affecting THD is the ripple voltage at the O/P of the peak detector which feeds back into the Y input of the multiplier thereby distorting the sine wave.

5. LC OSCILLATOR WITH AGC LOOP



The loop gain at resonance of L_x and C_x is given by the following:

$$L(j\omega_n) = \frac{EPR}{EPR + R_X} \times \left(1 + \frac{R_F}{R_E}\right) \times A_{MUL} V_Y = 1 \angle 0^o \quad and \quad \omega_n = \frac{1}{L_X C_X}$$

The Equivalent Parallel Resistance (EPR) of the gyrator that simulates the inductor L_x using the op amp circuit shown on the next page has to be determined by simulation as shown on the next page.
If the op amps were ideal, the EPR would be infinite and the inductor would be ideal - no losses.

Note: The EB junction reverse breakdown voltage is normally low, between 5V and 10V, for most transistors, thereforeif there is a risk that the EB junction goes into avalanche breakdown, add a diode in series with the emitter or simply replace the transistor for one that has a high breakdown voltage.

Simulation of inductor with gyrator

Gyrator equations

Assuming ideal op amps, we can derive the following equation for the gyrator:

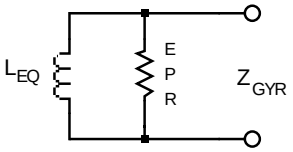
$$Z_{GYR(ideal)} = \frac{Z_1 Z_3 Z_5}{Z_2 Z_4} = \frac{R_1 R_3 R_5}{R_2\left(\frac{1}{j\omega C_4}\right)}$$

$$Z_{GYR(actual)} = j\omega\left(\frac{R_1 R_3 R_5 C_4}{R_2}\right) \| EPR$$

$$Z_{GYR(actual)} = \left(j\omega\ L_{EQ}\right) \| EPR$$

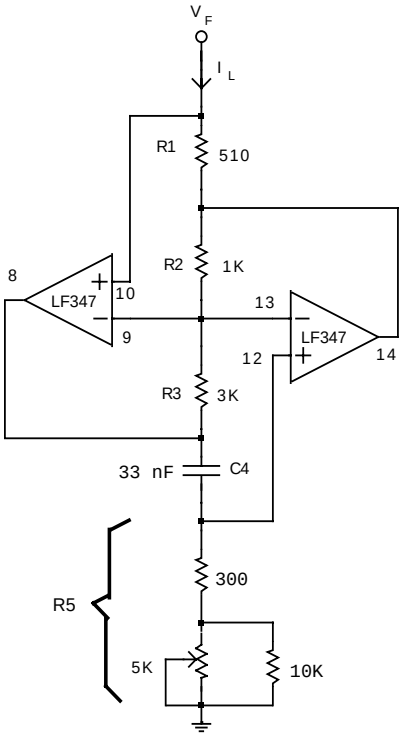
$$where \quad L_{EQ} = \frac{R_1 R_3 R_5 C_4}{R_2}$$

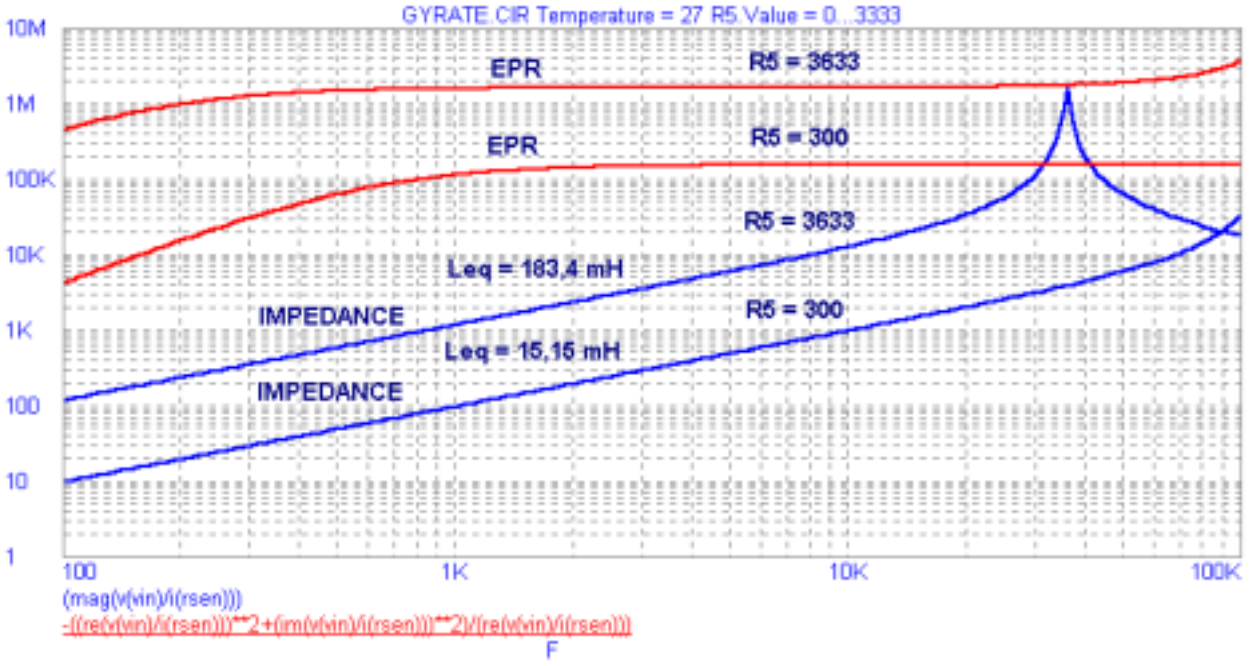
Unideal Gyrator



Theoretically, the gyrator simulates a pure inductor in the present application. However, in practice, as frequency increases, the op amps' voltage gain decreases and is no longer ideal and this implies that Z_{GYR} is not purely inductive but has some Equivalent Parallel Resistance (EPR) at high frequency.

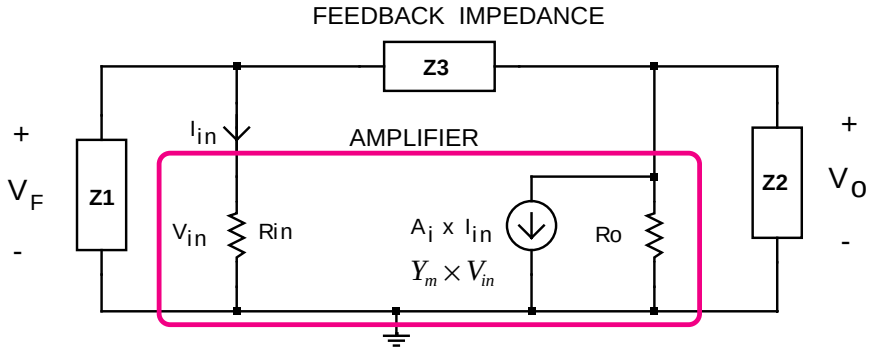
Gyrator





6. L-C REACTANCE COUPLED OSCILLATORS

Basic equations



Z_1, Z_2 and Z_3 will be reactive components, that is capacitors, inductors, combination of both or a crystal. The above amplifier model is used to derive a single formula that will apply to both inverting and non-inverting amplifiers. Z_3 is the feedback impedance and Z_2 will be assumed much smaller than R_O of the amplifier.

$$V_o = -A_i \times i_{in} \times \left[R_o \| Z_2 \| \left(Z_3 + Z_1 \| R_{in}\right)\right] \approx -A_i \times \frac{V_{in}}{R_{in}} \times \left[Z_2 \| \left(Z_3 + Z_1 \| R_{in}\right)\right]$$

$$A_V = \frac{V_o}{V_{in}} = -\frac{A_i}{R_{in}} \times \left[Z_2 \| \left(Z_3 + Z_1 \| R_{in}\right)\right] \quad or \quad A_V = \frac{V_o}{V_{in}} = -Y_m \times \left[Z_2 \| \left(Z_3 + Z_1 \| R_{in}\right)\right]$$

$$\beta_V = \frac{V_E}{V_o} = \frac{Z_1 \| R_{in}}{\left(Z_3 + Z_1 \| R_{in}\right)} \quad \Rightarrow \quad L(S) = \beta_V A_V = -\frac{A_i}{R_{in}} \times \frac{Z_2 \left(Z_1 \| R_{in}\right)}{\left(Z_1 \| R_{in}\right) + Z_2 + Z_3}$$

Simplifying we obtain the following expression:

$$L(S) = \beta_V A_V = -\frac{A_i Z_1 Z_2}{R_{in}\left(Z_1 + Z_2 + Z_3\right) + Z_1\left(Z_2 + Z_3\right)}$$

The circuit will oscillate very near the series resonant frequency of Z_1, Z_2 and Z_3.

$$L(S) = \beta_V A_V = -\frac{Y_m R_{in} Z_1 Z_2}{R_{in}\left(Z_1 + Z_2 + Z_3\right) + Z_1\left(Z_2 + Z_3\right)}$$

For lossless components, we have $Z_1 + Z_2 + Z_3 = 0 \Rightarrow Z_2 + Z_3 = -Z_1$

For lossy components, we have $Z_1 + Z_2 + Z_3 = ESR_{tot} \Rightarrow Z_2 + Z_3 = ESR_{tot} - Z_1$

For BJT transistors

With lossless components: $L(S) = \dfrac{A_i Z_2}{Z_1}$

With lossy components:

$$L(S) = \frac{-A_i Z_1 Z_2}{R_{in} ESR_{tot} + Z_1\left(ESR_{tot} - Z_1\right)}$$

For FET transistors

With lossless components: $L(S) = \dfrac{Y_m R_{in} Z_2}{Z_1}$

With lossy components: (and R_{in} very large)

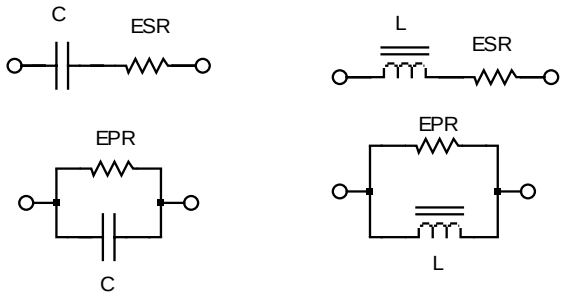
$$Z_1 + Z_2 + Z_3 = ESR_{tot} \Rightarrow Z_2 + Z_3 = ESR_{tot} - Z_1$$

$$L(S) = \frac{-Y_m Z_1 Z_2}{ESR_{tot} + Z_1\left(ESR_{tot} - Z_1\right)/\, R_{in}} \approx \frac{-Y_m Z_1 Z_2}{ESR_{tot}}$$

Lossy reactances

Actual capacitors and inductors have losses which are often defined with a Q factor. Losses can be represented either by an equivalent series resistor (ESR) or an equivalent parrallel resistor (EPR).

$$Q_{SER} = \frac{X_{SER}}{ESR} \Leftrightarrow Q_{PAR} = \frac{EPR}{X_{PAR}}$$



Types of oscillators

1st case A_i or Y_m is +ve Z_1 and Z_2 must be the same type of reactance (both capacitive or both inductive) in order to obtain 0° phaseshift in the loop gain. This also means that Z_3 must be the opposite type of reactance in order to have series resonance $Z_1+Z_2+Z_3 = 0$

2nd case A_i or Y_m is -ve Z_1 and Z_2 must be opposite types of reactance (one capacitive and the other inductive) in order to obtain 0° phaseshift in the loop gain. Z_3 can be either type of inductance to series resonate

$Z_1+Z_2+Z_3 = 0$

Impedance configuration for +ve A_i or Y_m

Type	Z1 (input)	Z2 (output)	Z3 (feedback)
Colpitts	C1	C2	L3
Hartley	L1	L2	C3
Clapp	C1	C2	Series L3-C3
Ultra-Audion	C1	C2	Parallel L3-C3
Pierce	C1	C2	Crystal

Impedance configuration for -ve A_i or Y_m

Type	Z1 (input)	Z2 (output)	Z3 (feedback)
Colpitts	C1	L2	C3
Hartley	L1	C2	L3
Clapp	C1	L2	Series L3-C3
Ultra-Audion	C1	L2	Parallel L3-C3
Pierce	C1	Crystal	C3

Example: Common emitter Colpitts oscillator

Design a Colpitts oscillator for a frequency of 1MHz. Bias transistor at I_C = 2 mA, V_{CE} =10,6V

Transistor data: h_{ib} at 1 mA = 28Ω, h_{fe} > 75
C_{in} = 10 pF, C_{out} = 5 pF

Solution: R_{B1} = 20K, R_{B2} = 10K, R_E = 2,2K

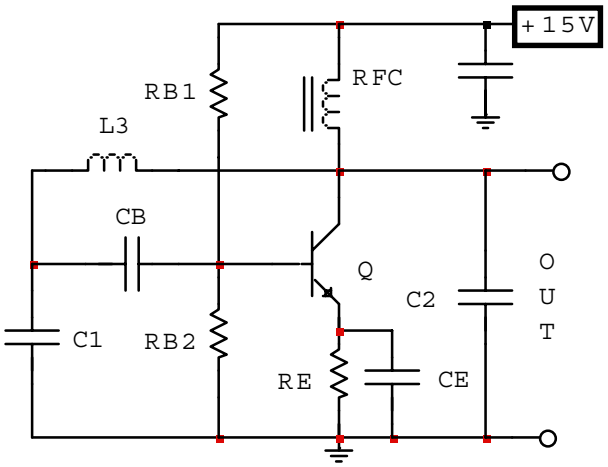
Assuming lossless reactances, we have:

$$L(S) = A_i \frac{Z_2}{Z_1} = A_i \frac{C_1}{C_2} = \frac{C_1}{C_2} \times \frac{h_{fe}}{1 + \frac{h_{ie}}{R_{B1} \| R_{B2}}}$$

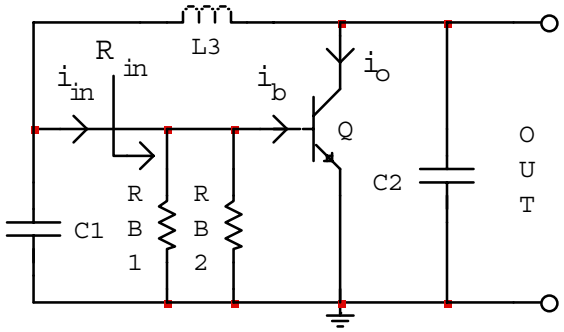
$$A_i = \frac{i_o}{i_{in}} = \frac{\frac{i_c}{V_F}}{\frac{R_{in}}{}} = \frac{\frac{i_c}{v_{be}}}{\frac{R_{in}}{}} = \frac{\frac{i_c}{i_b h_{ie}}}{\frac{R_{in}}{}} = \frac{i_c R_{in}}{i_b h_{ie}}$$

$$A_i = h_{fe} \times \frac{R_{B1} \| R_{B2} \| h_{ie}}{h_{ie}} = \frac{h_{fe}}{1 + \frac{h_{ie}}{R_{B1} \| R_{B2}}}$$

$$h_{ie} = (h_{fe} + 1) h_{ib} = 76 \times 28 / 2 = 1024 \text{ min}$$



AC equivalent circuit



The circuit will oscillate at the series resonant frequency where $Z_1+Z_2+Z_3 = 0$. Stray capacitance C_{in} of transistor must be lumped with Z_1 and C_o with Z_2.

$$\frac{1}{j\omega(C_1 + C_{in})} + \frac{1}{j\omega(C_2 + C_o)} + j\omega L_3 = 0 \Rightarrow j\omega L_3 = \frac{-1}{j\omega}\left(\frac{1}{(C_1 + C_{in})} + \frac{1}{(C_2 + C_o)}\right)$$

$$\omega_n = \sqrt{\frac{1}{L_3}\left(\frac{1}{(C_1 + C_{in})} + \frac{1}{(C_2 + C_o)}\right)}$$

Let us use C_1 and C_2 values that are much higher than the stray capacitances of the transistor in order to desensitise the resonant frequency with respect to the stray capacitances. We must also consider the Q factor of the resonant circuit in the design. The larger the Q, the less noisy the oscillator will be which results in narrower spectral rays. The Q of C_1, C_2 and L_3 can be selected high (given in data sheets) but if R_{in} of the amplifier is too low, then the circuit Q will be too low. Let $Q_{par} = R_{in} / X_{C1} \rangle 10$ for a good sinewave at v_b:

$$C_1 \rangle (2\pi \times 1M \times 887,7 / 10)^{-1} = 1,79\ nF$$

$$L(S) = \frac{C_1}{C_2} \times \frac{h_{fe(\min)}}{1 + \frac{h_{ie}}{R_{B1} \| R_{B2}}} \rangle 1 \angle 0° \Rightarrow L(S) = \frac{C_1}{C_2} \times \frac{75}{1 + \frac{1064}{20k \| 10k}} = 64,7 \times \frac{C_1}{C_2}$$

Let L(S) =3 to make sure there is enough loop gain - losses not accounted for in above formula.

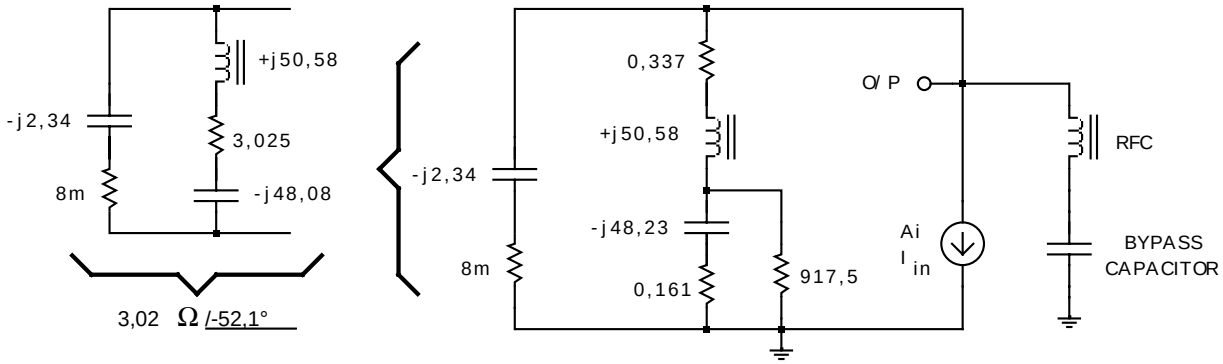
NOTE: The higher L(S) is, the higher v_c is and the higher the distortion is in the v_c waveform.

Let C_1 = 3,3nF $L(S) = 64,7 \times \frac{C_1}{C_2} = 3 \Rightarrow C_2 = \frac{64,7 \times 3,3n}{3} = 71,2\ nF \Rightarrow 68\ nF\ std$

NOTE: Decreasing ratio C_2/C_1 by factor of N will make loop gain N times larger.

$$L_3 = \frac{1}{\omega_n^2}\left(\frac{1}{(C_1 + C_{in})} + \frac{1}{(C_2 + C_o)}\right) = \frac{1}{(2 \times \pi \times 1M)^2}\left(\frac{1}{(3,3n + 10p)} + \frac{1}{(68n + 5p)}\right) = 8,05\ \mu H$$

Let us calculate the output impedance and the circuit Q assuming a Q = 150 for the inductor and Q = 300 for the capacitors. ESR of components is given by X / Q.



Z_{out} = 3,02Ω /-52,1° , $Q_{CIR} = X_L/ESR_{tot} = X_C/ESR_{tot}$ = 50,58/(3,025+0,008) = 16,7 > 10 - OK!

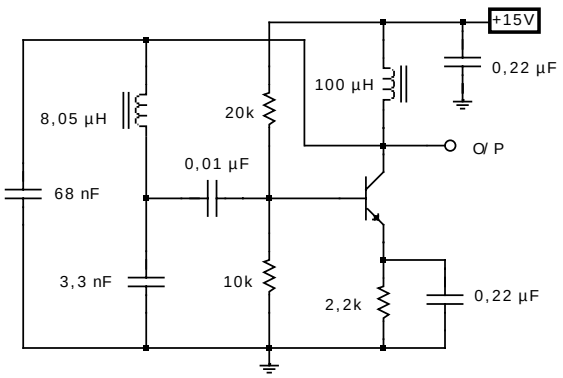
RFC: Make X_L > 100 x Z_{out} so that the resonant circuit is not loaded by the RF choke.
X_L = 100 x 3,02 = 302Ω, L > 302/(2* π * 1M) = 48 μH, let L = 100 μH

Bypass cap: make $X_C < (X_{ch}/100)$= 6,28 to attenuate HF so it does not cause stray feedback on supply rail.
C > 1/(2* π*1M*6,28) = 25.3 nF let C = 0.22μF

Emitter bypass cap: Make $X_C < h_{ib} / 10$ = 1.4Ω, C > 1/(2*π*1M*1.4) = 0.11 μF let C_E = 0.22 μF

Base coupling cap: Make $X_C < R_{in} / 10$ = 88.8, C > 1/(2*π*1M*91.7) = 1.75 nF let C_E = 0.01 μF

Final circuit: 1 MHz Colpitts oscillator



Exact loop gain check

$$L(S) = \frac{-A_i \ Z_1 Z_2}{R_{in} ESR_{tot} + Z_1 (ESR_{tot} - Z_1)} \Rightarrow$$

$$\frac{-64,7 \ (0,161 - j48,23)(7,8m - j2,34)}{917,5 \times 0,506 + (0,161 - j48,23)(0,506 - (0,161 - j48,}$$

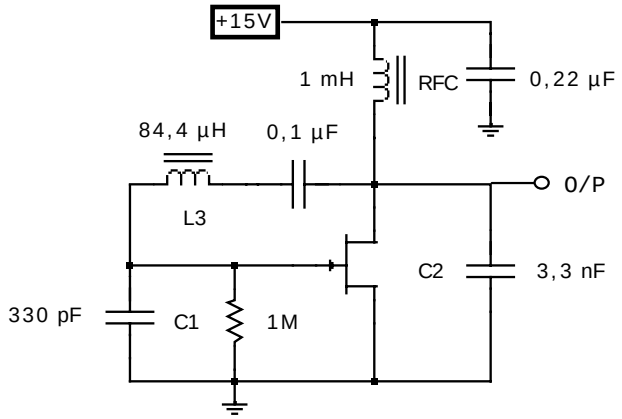
$$L(S) = 2,617\ \underline{/0,564°}$$

This is lower than the design value of 3 because of the losses in the components - we used the approximate loop gain equation for the design. Non-linearity of the EB junction will regulate the loop gain to one.

C_E and the RF choke (100 μH) are critical for stability of the loop gain regulation mechanism and may have to be changed for a stable output amplitude. The amplitude of the output voltage is proportional to the loop gain. If R_E is decreased, L(S) increases and V_o goes up with a higher THD.

Example: Common source Colpitts oscillator

Design a Colpitts oscillator for a frequency of 1MHz. Bias transistor at V_{GS} = 0V for maximum transistor gain (Y_{fs} max).



Transistor 2N5486 data (typical)

I_{DSS} = 10 mA, V_P = -3,5V
Y_{fs} = 5.5 mS at V_{GS} = 0V,
C_{iss} = 3.5 pF, C_{oss}= 1.5 pF

$$L(S)=\beta_V A_V=-Y_m\times\frac{Z_2\left(Z_1\|R_{in}\right)}{\left(Z_1\|R_{in}\right)+Z_2+Z_3}\approx -Y_m\times\frac{Z_1Z_2}{Z_1+Z_2+Z_3}=\frac{-Y_mZ_1Z_2}{ESR_{tot}}$$

Z_1, Z_2 and Z_3 will resonate, total series reactance will be zero and we are left with the total ESR that accounts for losses of the three impedances.

$$\omega_n=\sqrt{\frac{1}{L_3}\left(\frac{1}{(C_1+C_{in})}+\frac{1}{(C_2+C_o)}\right)}$$

$$\frac{1}{j\omega(C_1+C_{in})}+\frac{1}{j\omega(C_2+C_o)}+j\omega L_3=0\Rightarrow j\omega L_3=\frac{-1}{j\omega}\left(\frac{1}{(C_1+C_{in})}+\frac{1}{(C_2+C_o)}\right)$$

$$L(S)=\frac{-Y_mZ_1Z_2}{ESR_{tot}}=\frac{Y_{fs}}{\omega_n{}^2C_1C_2ESR_{tot}}\quad but\quad \omega_n{}^2C_1C_2=\frac{C_1+C_2}{L_3}\quad therefore\quad L(S)=\frac{Y_{fs}L_3}{(C_1+C_2)ESR_{tot}}\times\frac{\omega_n}{\omega_n}$$

$$L(S)=\frac{Y_{fs}}{\omega_n(C_1+C_2)}\times\frac{\omega_nL_3}{ESR_{tot}}=\frac{Y_{fs}Q_{tot}}{\omega_n(C_1+C_2)}\rangle 1\angle\underline{0^o}\Rightarrow(C_1+C_2)\langle\frac{Y_{fs}Q_{tot}}{\omega_n}$$

$$worst\ \ case\ \ (C_1+C_2)\langle\frac{Y_{fs(\min)}Q_{tot(\min)}}{\omega_n}$$

$$(C_1+C_2)\langle\frac{Y_{fs(\min)}Q_{tot(\min)}}{\omega_n}=\frac{1m\times 50}{2\pi\times 1M}=8\ nF\quad let\quad C_1+C_2\approx 4nF\quad and\quad C_2/C_1\approx 10$$

$$C_1+C_2=11\ C_1\approx 4\,nF\quad C_1=364\ pF\ (330pF\ std)\quad and\quad C_2=3{,}3\,nF$$

NOTE: A larger C_2 value entails a low Z_o and less "frequency pulling" by the load.

$$\omega_n^2=\frac{1}{L_3}\left(\frac{1}{(C_1+C_{in})}+\frac{1}{(C_2+C_o)}\right)\approx\frac{1}{L_3}\left(\frac{1}{C_1}+\frac{1}{C_2}\right)$$

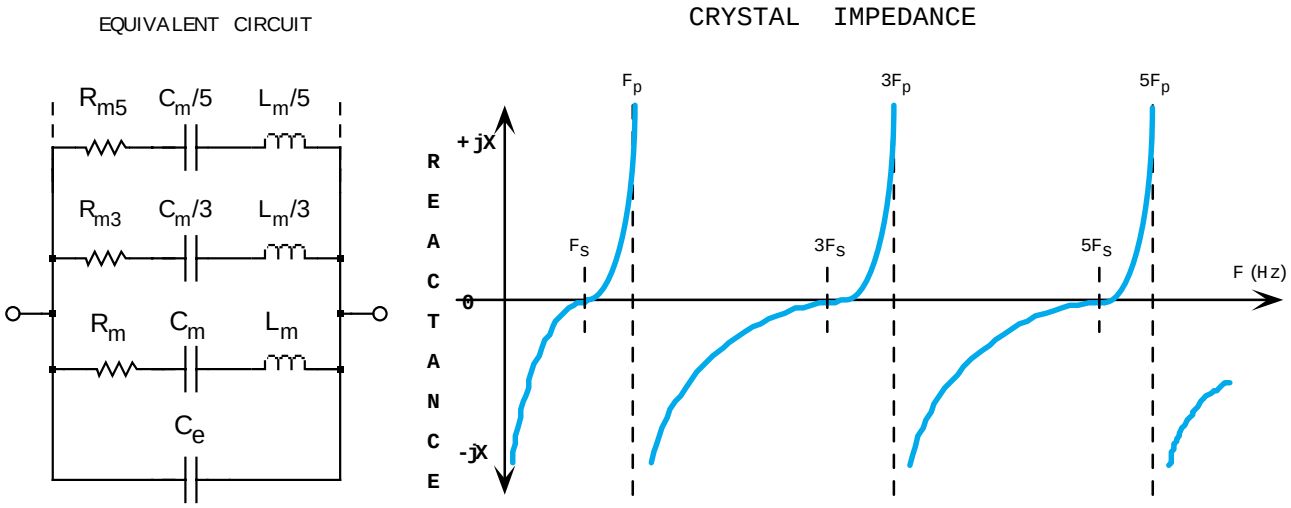
$$L_3=\frac{1}{\omega_n^2}\left(\frac{1}{C_1}+\frac{1}{C_2}\right)=\frac{1}{\left(2\pi\times 10^6\right)^2}\left(\frac{1}{330\,p}+\frac{1}{3{,}3\,n}\right)=84{,}4\ \mu H$$

Again if we assume a Q of 150 for the inductors and 300 for the capacitors, the resonant circuit Q is 95,9 also taking into account the 1M resistor losses. This is a lot higher than the BJT oscillator and yields a less noisy O/P.

RFC: Make X_L > 50 X_{C2} so that the resonant frequency is not affected by the RF choke.
Bypass cap: make $X_C \approx X_{RFC}/50$ to attenuate HF so it does not cause stray feedback on supply rail.
Gate coupling cap: Make X_C << X_{C1} +X_{C2} such that it does not affect the resonant circuit.

7. Crystal Oscillators

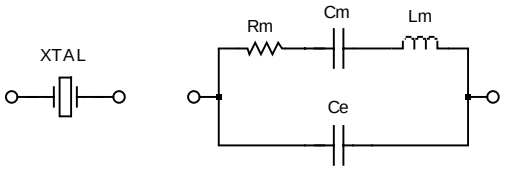
Crystal Characteristics



L_M, C_M and R_M are the electrical equivalents of the crystal mechanical resonator at the fundamental resonant frequency. The values of L_M, C_M amd R_M depend on the mechanical properties of the crystal and the way it has been cut. C_e accounts for the electrical capacitance of the crystal electrodes and its holder parasitic capacitance. R_M represents the energy losses in the crystal. A mechanical resonator can also resonate at odd harmonic frequencies (or overtones) of the fundamental frequency - the equivalent C_M and L_M values are not necessarily divided exactly by a factor of N.

Simplified model for fundamental mode operation

The equivalent circuit of the crystal can be reduced to two branches to study the fundamental mode of operation.

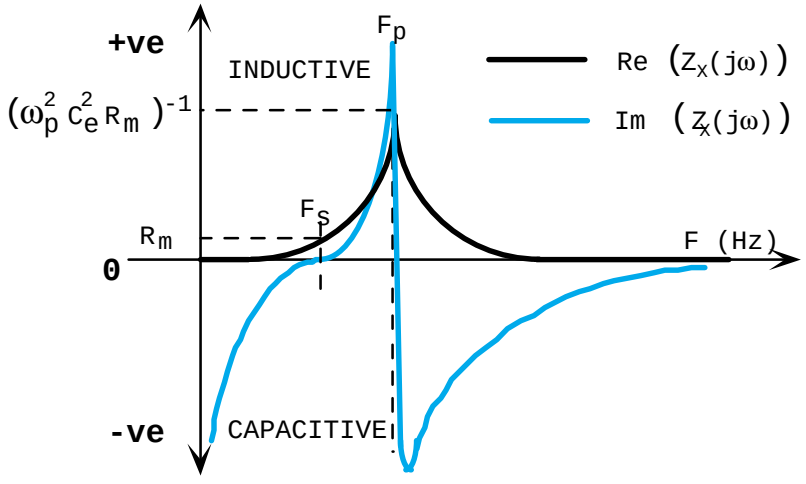


Crystal impedance

$$\frac{1}{SC_e}\left\|\left[R_m + SL_m + \frac{1}{SC_m}\right]\right. \quad simplifies \quad to$$

$$\frac{1}{SC_e} \times \left[\frac{S^2 + \frac{R_m}{L_m}S + \frac{1}{L_m C_m}}{S^2 + \frac{R_m}{L_m}S + \frac{1}{L_m}\left(\frac{1}{C_m} + \frac{1}{C_e}\right)}\right]$$

$$= \frac{1}{SC_e} \times \left[\frac{S^2 + 2\zeta_S\omega_S S + \omega_S^2}{S^2 + 2\zeta_p\omega_p S + \omega_p^2}\right]$$



Series resonance: $\omega_S = 1/\sqrt{L_m C_m}$ implies $X_{Lm} = X_{Cm}$ and

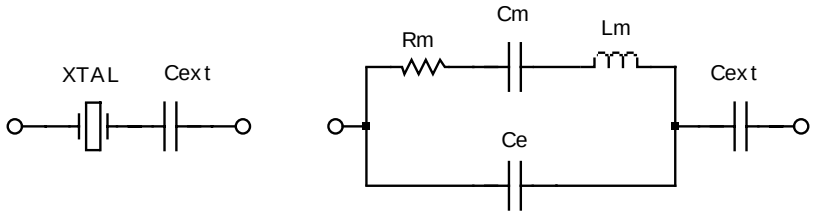
$$Z_X(j\omega_S) = R_m \| (1/\omega_S C_e) = R_m - j\omega_S R_m^2 C_e \approx R_m$$

Parallel resonance: $\omega_P = \sqrt{\frac{1}{L_m}\left(\frac{1}{C_m} + \frac{1}{C_e}\right)}$ implies $X_{Lm} = X_{Cm} + X_{Ce}$ and

$$Z_X(j\omega_p) = \frac{1}{\omega_p^2 C_e^2 R_m} - \frac{1}{j\omega_p C_e} \approx \frac{1}{\omega_p^2 C_e^2 R_m}$$

Notice that the crystal impedance is inductive only between F_S and F_P which is a very narrow range - F_S and F_p are very close to each other because $C_m << C_e$.

Effect of external capacitance - series connection



In practice when the crystal is used in a circuit, it is always in the presence of some external capacitance, whether parasitic or actual capacitor, which will slightly shift either the series or parallel resonant frequency of the crystal. When C_{ext} is in series with the crystal, the series resonant frequency is shifted as shown by the following expression:

$$Z_{XTAL}(S) + \frac{1}{SC_{ext}} = \frac{1}{S}\left(\frac{1}{C_e} + \frac{1}{C_{ext}}\right) \times \left[\frac{S^2 + \frac{R_m}{L_m}S + \frac{1}{L_m}\left(\frac{1}{C_m} + \frac{1}{C_e + C_{ext}}\right)}{S^2 + \frac{R_m}{L_m}S + \frac{1}{L_m}\left(\frac{1}{C_m} + \frac{1}{C_e}\right)}\right]$$

$$\omega_S = \sqrt{\frac{1}{L_m}\left(\frac{1}{C_m} + \frac{1}{C_e + C_{ext}}\right)} \qquad \omega_P = \sqrt{\frac{1}{L_m}\left(\frac{1}{C_m} + \frac{1}{C_e}\right)}$$

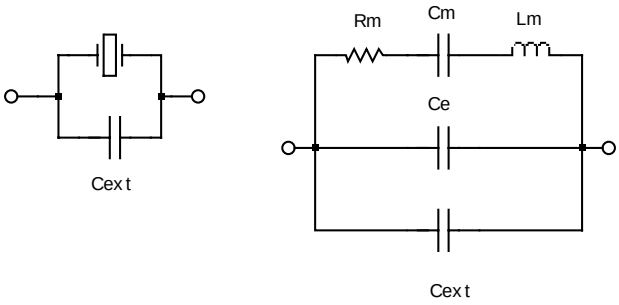
One can see that F_P is not affected by C_{ext} when C_{ext} is connected in series with the crystal.

As C_{ext} varies from ∞ to 0, ω_S is shifted from $\omega_S = \frac{1}{\sqrt{L_m C_m}}$ *to* $\omega_S = \omega_P = \sqrt{\frac{1}{L_m}\left(\frac{1}{C_m} + \frac{1}{C_e}\right)}$

NOTE: Use of a large C_{ext} is not recommended as it increases the amplitude of the mechanical vibrations of the crystal which shifts the crystal frequency and may also break the crystal. Amplitude of voltage across crystal must be low to maintain a low power dissipation (called drive level) which is usually in the XX μW range.

The manufacturer will always specify or calibrate the crystal frequency with a nominal load or external capacitance. If a different external capacitance is used, the accuracy of the crystal is not guaranteed.

Effect of external capacitance - parallel connection



One can see that F_S is not affected by C_{ext} when C_{ext} is connected in parallel with the crystal. As C_{ext} varies from ∞ to 0, ω_P is shifted from

$$\omega_P = \sqrt{\frac{1}{L_m C_m}} \quad to \quad \sqrt{\frac{1}{L_m}\left(\frac{1}{C_m}+\frac{1}{C_e}\right)}$$

Same range as F_S for the series connection.

$$Z_{TOT} = Z_{XTAL}(S) \left\| \frac{1}{SC_{ext}} = \frac{1}{S(C_e + C_{ext})} \times \left[\frac{S^2 + \frac{R_m}{L_m}S + \frac{1}{L_m C_m}}{S^2 + \frac{R_m}{L_m}S + \frac{1}{L_m}\left(\frac{1}{C_m}+\frac{1}{C_e+C_{ext}}\right)} \right] \right.$$

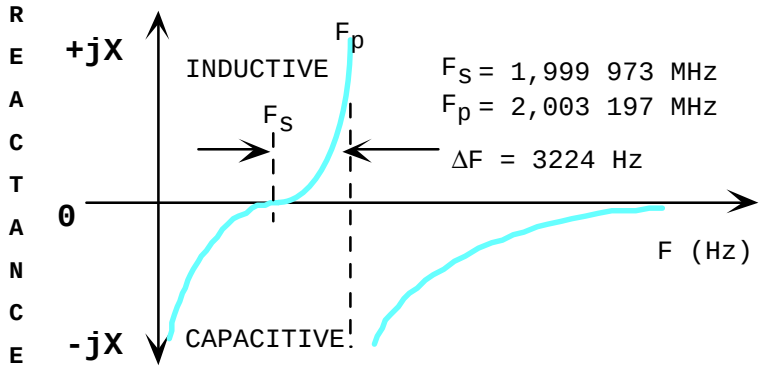
EXAMPLE - 1 **Calculation of crystal parameters**

A crystal has the following parameters: R_m = 500Ω, L_m = 13,084179H, C_m = 0,484 x 10^{-15} F, C_e = 0,15 pF, F=2,000 000 MHz nominal

A) Determine the series and parallel resonant frequencies of the crystal alone to 1 Hz accuracy.

$$F_S = \frac{1}{2\pi\sqrt{L_m C_m}} = 1{,}999\ 973\ \text{MHz} \qquad F_P = \frac{1}{2\pi}\sqrt{\frac{1}{L_m}\left(\frac{1}{C_m}+\frac{1}{C_e}\right)} = 2{,}003\ 197\ \text{MHz}$$

B) Sketch the impedance response assuming the crystal is lossless.
R_m = 0, the impedance is purely reactive.



C) What is the "tuning" range of the crystal if we add external capacitance?

The series or the parallel resonant frequency of the crystal + external capacitor can range from F_S to F_P of the crystal alone, that is from 1,999 973 MHz to 2,003 197 MHz, which is a range of 3224 Hz or 0,161 %.

D) What is the series Q factor of the crystal?

$$Q_S = \frac{X_{L_m}}{R_m} = \frac{X_{C_m}}{R_m} = \frac{2\pi \times 1\,999\,973 \times 13{,}084179}{500} = 328\,837$$

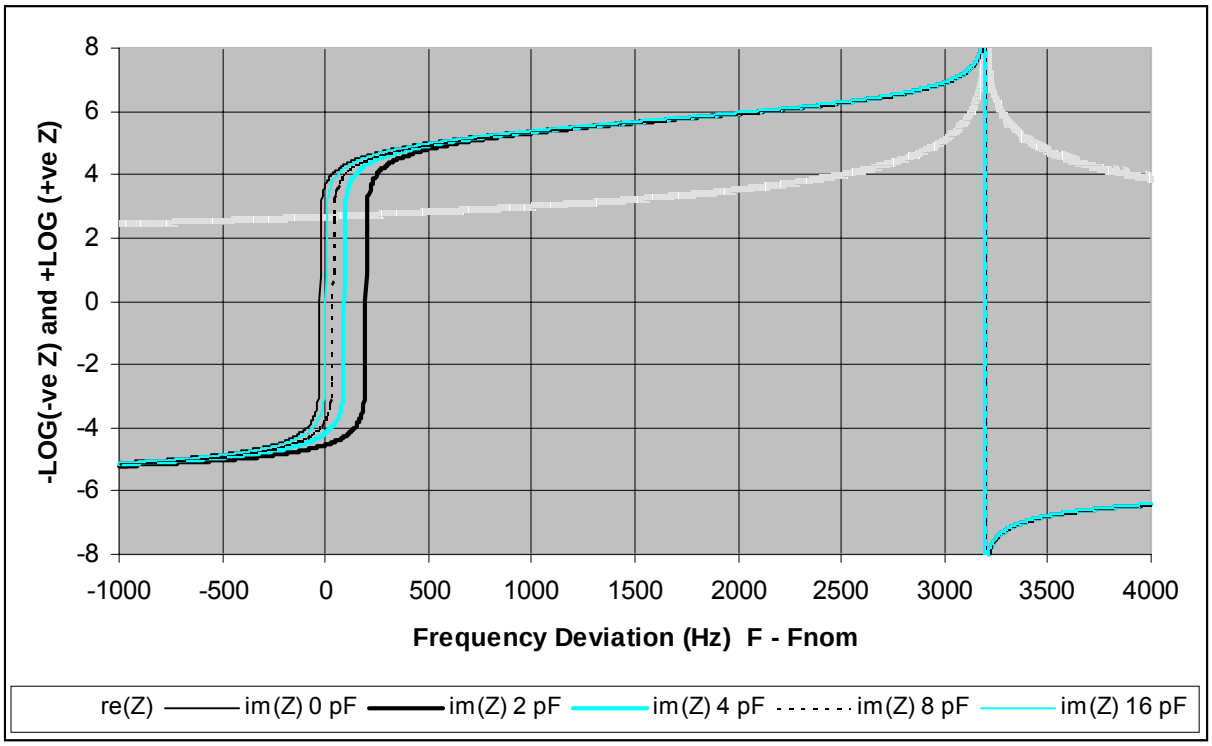
Typical Q values are usually from 10K to 100K but may also be higher.

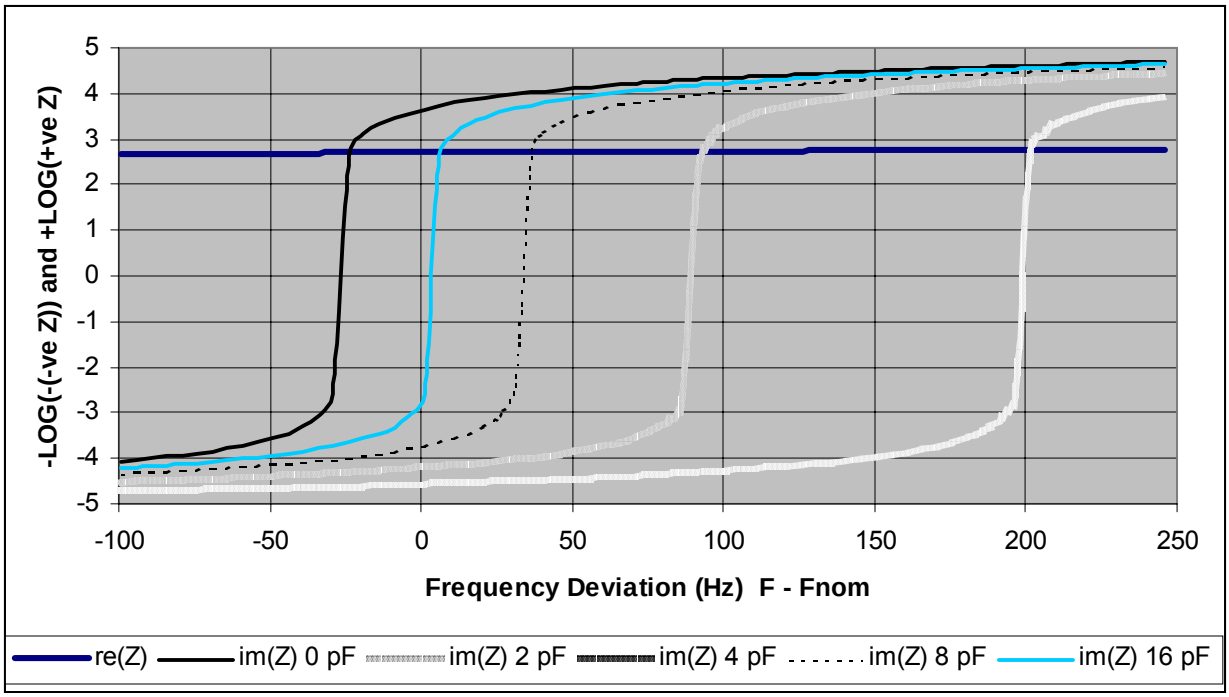
E) What is nominal load capacitance for which the crystal frequency is specified?

$$\omega_{nom} = \sqrt{\frac{1}{L_m}\left(\frac{1}{C_m} + \frac{1}{C_e + C_{ext}}\right)} \Rightarrow \omega_{nom}^2 = \frac{1}{L_m}\left(\frac{1}{C_m} + \frac{1}{C_e + C_{ext}}\right)$$

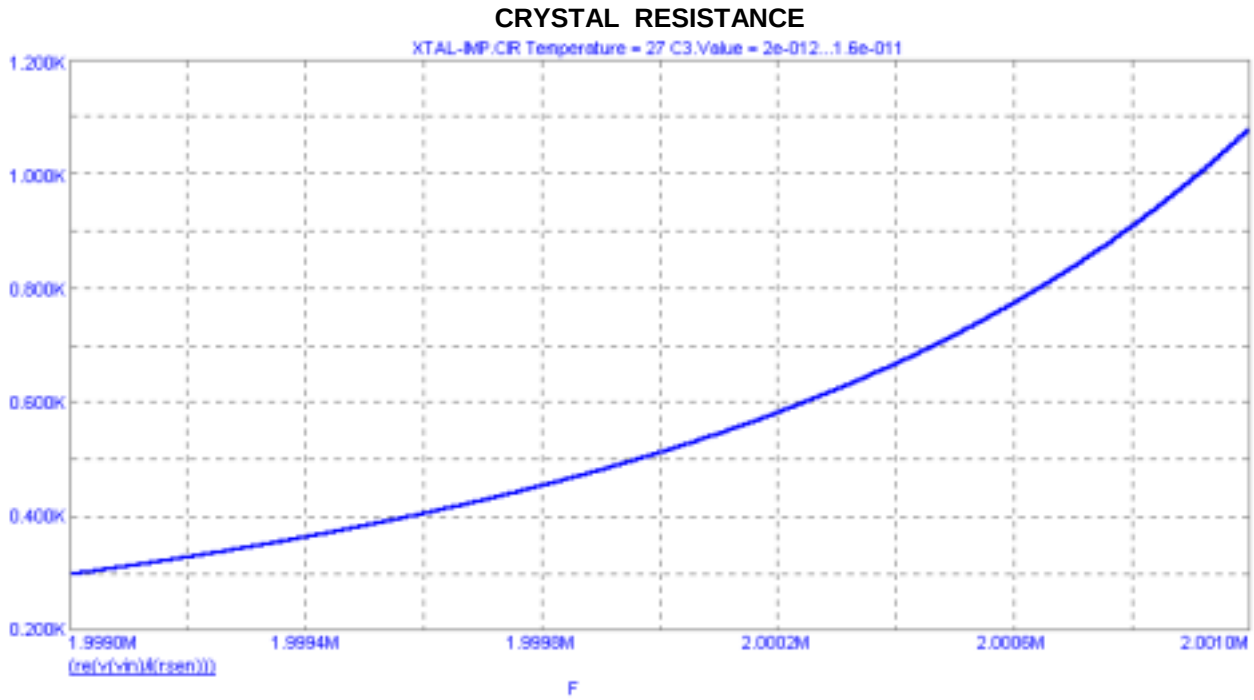
Solving the above equation we have C_{ext} = 18 pF.

F) Determine the effect of a series C_{ext} on the real and imaginary parts of $Z_{tot} = Z_{XTAL} + 1/SC_{ext}$
Do for C_{ext} = 0, 2, 4, 8 and 16 pF - use a spread sheet or mathCAD software.





From the above graph one can see that F_S is very close to 2,000 000 MHz with C_{ext} = 16 pF (less than 10 Hz away). As C_{ext} increases above 16 pF, F_S can only shift by 27 Hz at the most. As C_{ext} goes down, the frequency shift increases exponentially to a max value of $F_p = \frac{1}{2\pi}\sqrt{\frac{1}{L_m}\left(\frac{1}{C_m}+\frac{1}{C_e}\right)}$



One can see that if F_s is shifted too much above F_{nom} , the crystal resistance increases exponentially and this may stop oscillation when the crystal is used in an oscillator.

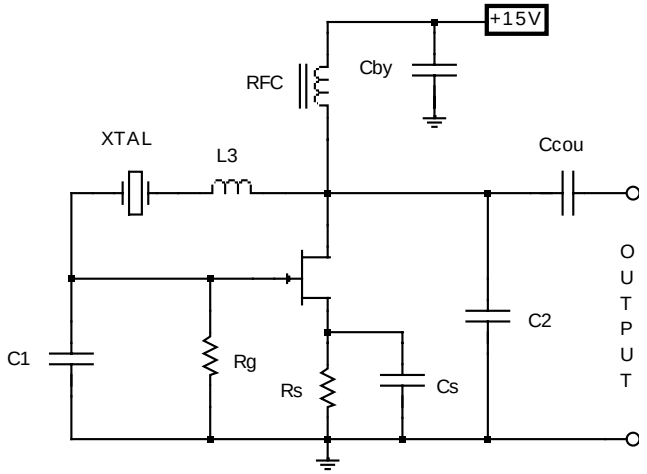
EXAMPLE **Design of a Pierce oscillator**

Design a Pierce oscillator using the following crystal specifications:

39,000 000 MHz 3rd overtone frequency with 20 pF load capacitance. Q_{XTAL} > 10 000

Transistor data (typical) 2N5486

I_{DSS} = 10 mA, V_P = -3,5V
Y_{fs} = 5.5 mS at V_{GS} = 0V,
C_{in}= 5 pF, C_{out}= 2.5 pF at V_{GS} =0V



The Pierce oscillator shown is basically a Colpitts oscillator with a crystal. L3 and C2+C_{out} are tuned at approximately 39 MHz to prevent the crystal from oscillating at the fundamental frequency or at other harmonic frequencies. C1 + C_{in} = C_{LOAD} of the crystal for an accurate crystal frequency. To obtain a loop gain greater than unity (see Colpitts example for derivation), we must have

$$(C_1 + C_2) \langle \frac{Y_{fs(\min)} Q_{tot(\min)}}{\omega_n}$$ where C1 includes C_{in} and C2 includes C_{out}. We are going to

operate the JFET at V_{GS} 0V, this means R_S = 0Ω and C_S is taken out, where Y_{fs} is maximum - this is OK for small AC signals only because we do not want to forward bias the gate-channel junction.

$$(C_1 + C_2) \langle \frac{Y_{fs(\min)} Q_{tot(\min)}}{\omega_n} = \frac{5,5m \times 10\,000}{2\pi \times 39M} = 0,224\,\mu F$$ for $L(j\omega_n) > 1$

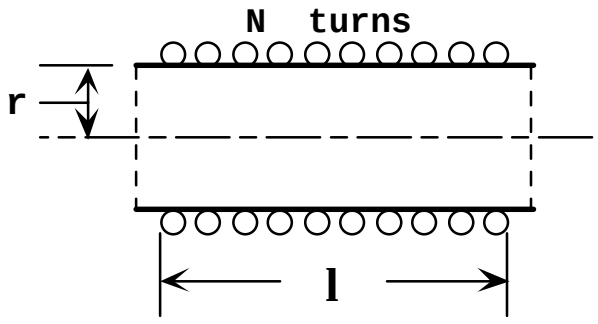
The constraint on C1 +C2 will not pose any problems. C1 = C_{LOAD} - C_{in} = 20 pF - 5 pF = 15 pF. Let us use L_3 = 0,2 µH, a value that can be wired easily on a small plastic form.

Air-Core Inductor Design

$$L = \frac{0,394\, r^2\, N^2}{9\, r + 10\, l} \qquad N = \sqrt{\frac{L \times (9\, r + 10\, l)}{0,394\, r^2}}$$

Formula valid only for l > 0,67 r and a single layer of turns.

L : inductance in µH N: number of turns
l : length in cm r: coil radius in cm



For maximum Q of the inductor, the length l should be equal to the coil diameter but this is not practical for most applications where we need a fair number of turns which require a longer coil. To obtain a better Q one can use a larger diameter wire which is less resistive. Now to increase the frequency range of the inductor one should leave some space between each turn of wire to reduce the stray capacitance of the coil.

Different schemes for L = 0,2 µH with AWG#24 wire diam=0,55 mm (21,6 mils)

r (cm)	0,15	**0,2**	0,25	0,15	0,2	0,25	0,15	0,2	0,25
l (cm)	1	**1**	1	1,5	1,5	1,5	2	2	2
N (turns)	16,0	**12,2**	10,0	19,2	14,6	11,8	21,9	16,6	13,4
SPACE(mm)	0,08	**0,29**	0,50	0,25	0,51	0,78	0,38	0,70	1,01

The possible schemes allow for enough space between each turn for low stray capacitance. The above calculations assume coated (insulated) wire diameter.

One can also use a metal shield around the inductor to prevent mutual inductance coupling with other components and reduce EMI (ElectroMagnetic Interference). The shield will lower the inductance value somewhat from the unshielded value depending on the geometry of the shield. For instance, an inductor with a circular shield will have the following inductance:

$$L = \left(\frac{0,394\ r^2\ N^2}{9\ r + 10\ l}\right) \times \left(1 - \frac{\left(\frac{r}{r_s}\right)^2}{1 + \frac{1,55(r_s - r)}{l}}\right)$$

r_S: shield radius

$$C_2 + C_{out} = \frac{1}{\omega_n^2 L_3} = \frac{1}{(2\pi \times 39M)^2\, 0,2\mu} = 83,2\ pF \Rightarrow C_{out} = 83,2\,p - 2,5p = 80,7\ pF$$ 82 pF std

RFC: Make $X_L > 100\ X_{L3}$ such that $\frac{1}{L_{EQ}} = \frac{1}{L_3} + \frac{1}{L_{RFC}} \approx \frac{1}{L_3} \quad \Rightarrow \quad if \quad L_{RFC} \rangle\rangle L_3$

Bypass cap: make $X_C < X_{RFC}/50$ to attenuate RF so it does not cause stray feedback on supply rail.

O/P coupling cap: Make $X_C << R_{LOAD}$ such that it does not cause any attenuation.

Final circuit

NOTE: Crystal inductive reactance cancels out X_C of 15 pF and C_{in} if value close to C_{LOAD} and 0,2 µH inductor resonates with 82 pF plus C_{out} to ensure crystal resonates on 3 rd overtone of 39 MHz. The non-linearity of the JFET will regulate the loop gain to one but the output amplitude is unpredictable.

The circuit shown below is the same basic oscillator but with an AGC loop to regulate the output voltage to a known value. The AGC voltage basically varies V_{GS} of the first JFET which in turn varies Y_{fs}. and thereby controls its gain for loop gain regulation.