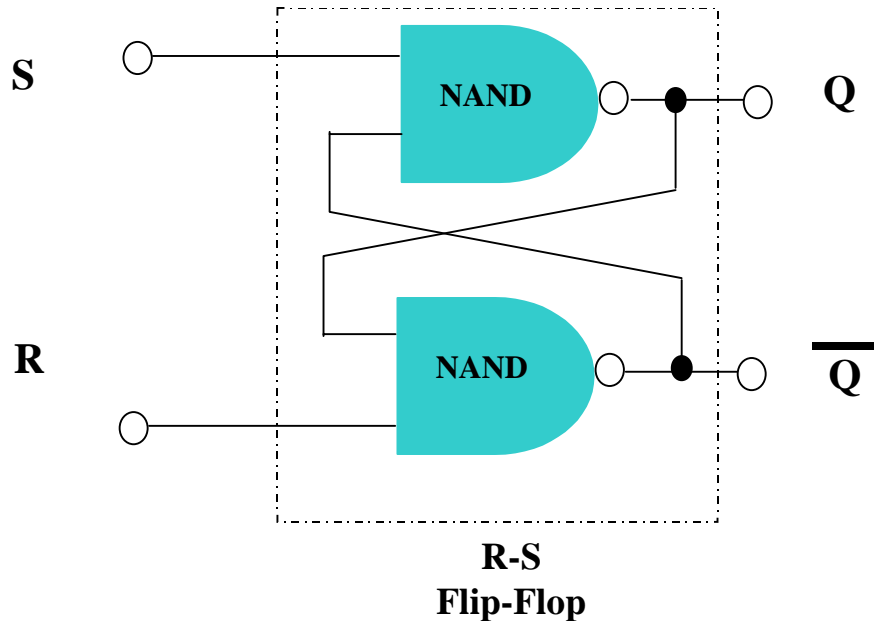


## J-K Flip-Flop

### Basic R-S Flip-Flop

Basic flip-flops are designed to 'store' a logic state. The simplest flip-flop is known as the R-S flip-flop, which consists of two NAND gate wired to give negative feedback and is shown in Figure 1.



**Figure 1 Simple NAND R-S Flip-Flop**

In normal operation the, with the reset (R) set to logic '0' the output Q will follow the logic level applied to the set (S) input.

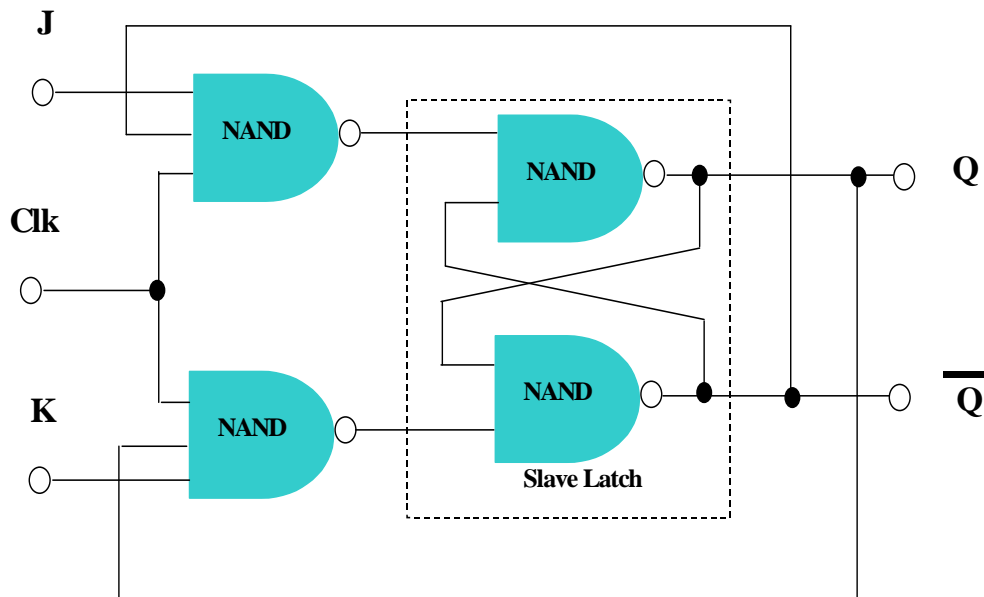
When R is set to logic '1' whatever was set on Q will remain regardless on whether the S input continues to change until the reset input is returned to logic '0'.

The major drawback of this circuit is that it is not possible to predict the output when a logic '1' is simultaneously applied to the S & R inputs.

Therefore, more complex Flip-flops are designed to ensure that these indeterminate states do not exit and the most common circuits are D-type and J-K Flip-flops.

## J-K Flip-Flop

The basic J-K Flip-flop is shown in Figure 2.



**Figure 2 Simple J-K Flip-flop**

Like the R-S flip-flop the outputs follow the inputs when the Clk is logic, but there are two inputs, traditionally labelled J and K.

If J and K are different then the output Q takes the value of J at the next clock edge.

If J and K are both low then no change occurs. If J and K are both high at the clock edge then the output will toggle from one state to the other. It can perform the functions of the R-S Flip-flop and has the advantage that there are no ambiguous states. Due to the extra logic that ensures only one of the R and S inputs is enabled at any time. This prevents possible oscillation, which can occur when both inputs of an RS flip-flop are active at the same time. The truth table of this J-K flip-flop is shown in Table 1.

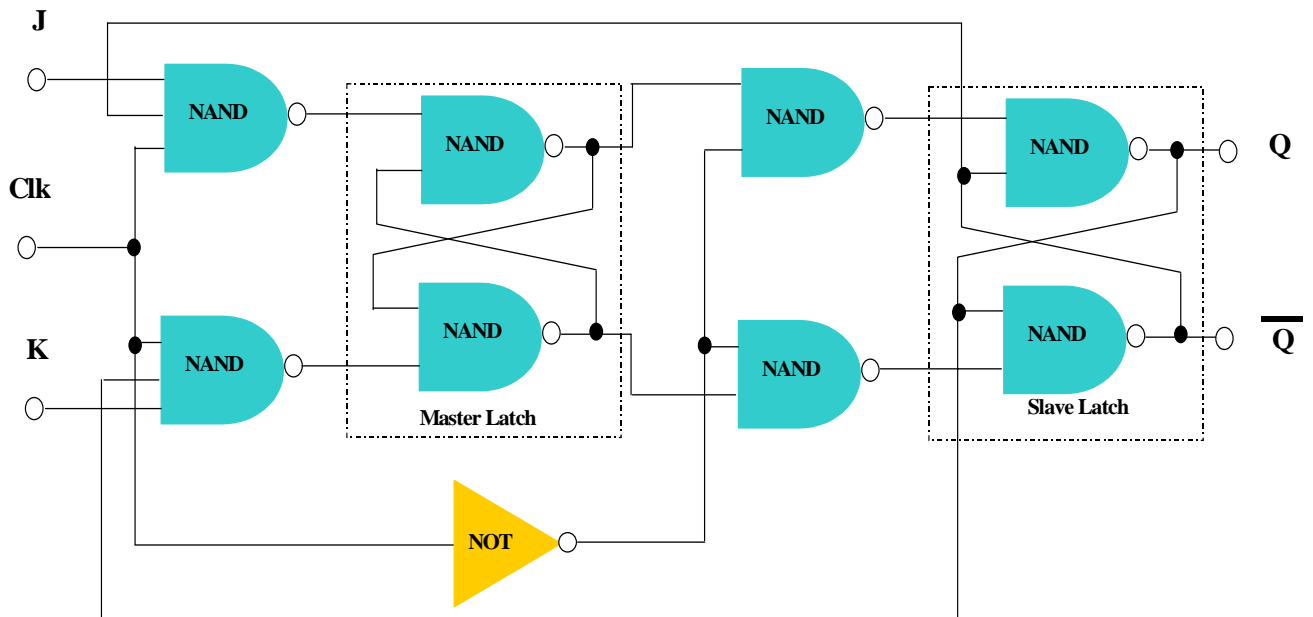
J	K	Clk	Q	Q_bar
0	0	Pos-edge	No change	
0	1	Pos-edge	0	1
1	0	Pos-edge	1	0
1	1	Pos-edge	Toggle	

**Table 1 Truth table for the simple J-K Flip-flop of Figure 2**

One problem with the basic J-K Flip-flop is that spikes can appear on the output and there is an unstable state when both J & K inputs are logic '0'.

This can be eliminated by adding another 'latch' circuit of this flip-flop to isolate the outputs Q and Q\_bar from the inputs J & K as shown in Figure 3.

The inverter connected between the two CLK inputs ensures that the two sections will be enabled during opposite half-cycles of the clock signal.



**Figure 3 Circuit of J-K Flip-flop note 3-input NAND gates are used on the input, the additional latch ensures edge operation and this circuit is known as a JK master-slave flip-flop.**

In normal operation the J-K flip-flop operates as per the R-S flip flop, however there are a couple of exceptions. The outputs only change on the falling edge of an applied clock pulse to the 'Clk' input.

This circuit can also act as a T-type Flip-flop, to accomplish toggling action if J and K are tied together.

This toggle application finds extensive use in binary counters and in frequency division found in prescalars.