Are the outputs from the PIC like Figure 1, 2 or 3?

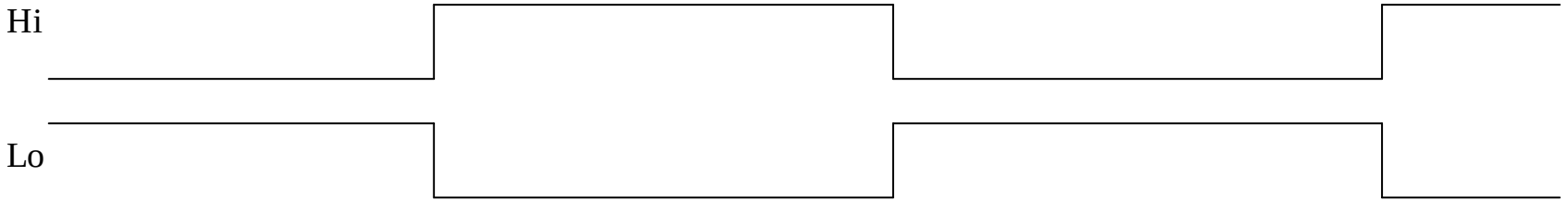


Figure 1

Figure 2 (underlap present but not enough)

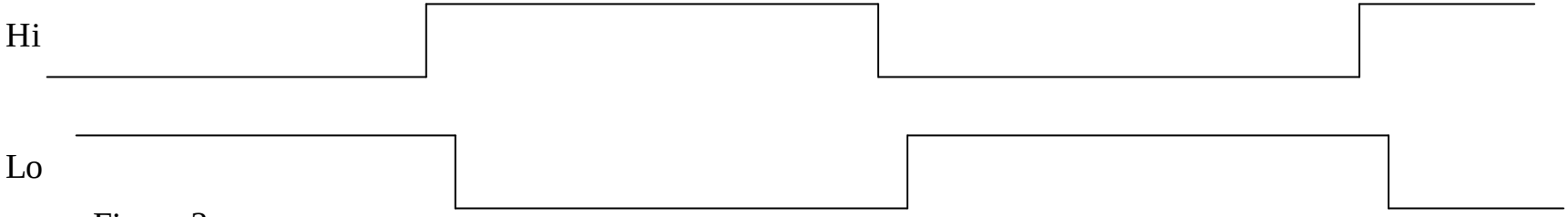
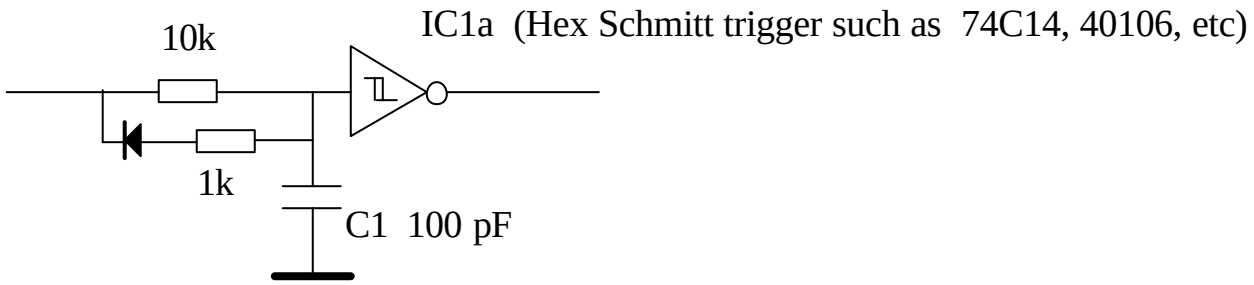


Figure 3

I have exaggerated the overlap/underlap for clarity.

See next page.



If Fig 1 or 2 apply, make 2 of these and insert in the Hi and Lo lines between the PIC and the IR2181 ICs.

If Fig 3 applies, make 1 of these and insert it in the Hi line between the PIC and the IR2181 ICs.
If more underlap is required in the Lo line, insert 1 in this line also.

These will delay the positive edges of the signals by about 1 uS but only delay the negative edges by about 100 nS.

Connect the unused inputs of IC1 to gnd.

If 1 uS is insufficient, increase C1