

August 2008

# Single-Channel: 6N138, 6N139 Dual-Channel: HCPL2730, HCPL2731 Low Input Current High Gain Split Darlington Optocouplers

#### **Features**

- Low current 0.5mA
- Superior CTR-2000%
- Superior CMR-10kV/µs
- CTR guaranteed 0-70°C
- U.L. recognized (File # E90700)
- VDE recognized (File # 120915) Ordering option V, e.g., 6N138V
- Dual Channel HCPL2730, HCPL2731

## **Applications**

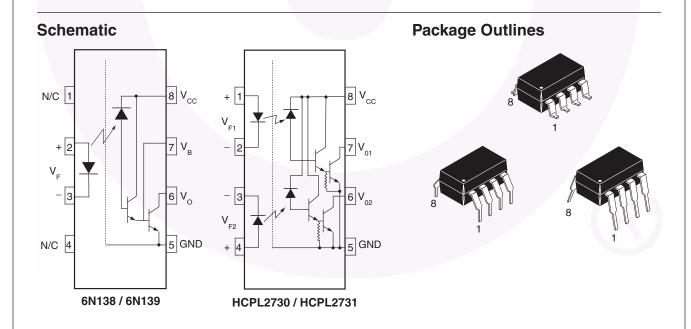
- Digital logic ground isolation
- Telephone ring detector
- EIA-RS-232C line receiver
- High common mode noise line receiver
- µP bus isolation
- Current loop receiver

## **Description**

The 6N138/9 and HCPL2730/HCPL2731 optocouplers consist of an AlGaAs LED optically coupled to a high gain split darlington photodetector.

The split darlington configuration separating the input photodiode and the first stage gain from the output transistor permits lower output saturation voltage and higher speed operation than possible with conventional darlington phototransistor optocoupler. In the dual channel devices, HCPL2730/HCPL2731, an integrated emitter-base resistor provides superior stability over temperature.

The combination of a very low input current of 0.5mA and a high current transfer ratio of 2000% makes this family particularly useful for input interface to MOS, CMOS, LSTTL and EIA RS232C, while output compatibility is ensured to CMOS as well as high fan-out TTL requirements. An internal noise shield provides exceptional common mode rejection of 10 kV/µs.



**Absolute Maximum Ratings** ( $T_A = 25^{\circ}$ C unless otherwise specified) Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Value	Units
T <sub>STG</sub>	Storage Temperature		-55 to +125	°C
T <sub>OPR</sub>	Operating Temperature		-40 to +85	°C
T <sub>SOL</sub>	Lead Solder Temperature (Wave solder only. See recompraph for SMD mounting)	mended reflow profile	260 for 10 sec	°C
EMITTER				
I <sub>F</sub> (avg)	DC/Average Forward Input Current	Each Channel	20	mA
I <sub>F</sub> (pk)	Peak Forward Input Current (50% duty cycle, 1 ms P.W.)	40	mA	
I <sub>F</sub> (trans)	Peak Transient Input Current - (≤1µs P.W., 300 pps)	1.0	Α	
V <sub>R</sub>	Reverse Input Voltage	Each Channel	5	V
P <sub>D</sub>	Input Power Dissipation	Each Channel	35	mW
DETECTO	R			
I <sub>O</sub> (avg)	Average Output Current	Each Channel	60	mA
V <sub>ER</sub>	Emitter-Base Reverse Voltage	6N138 and 6N139	0.5	V
V <sub>CC</sub> , V <sub>O</sub>	Supply Voltage, Output Voltage	6N138, HCPL2730	-0.5 to 7	V
		6N139, HCPL2731	-0.5 to 18	
Po	Output Power Dissipation	Each Channel	100	mW

## **Electrical Characteristics** (T<sub>A</sub> = 0 to 70°C unless otherwise specified)

## **Individual Component Characteristics**

Symbol	Parameter	Test Cond	itions	Device	Min.	Тур.*	Max.	Unit
EMITTER		1		1	Į.		Į.	
V <sub>F</sub>	Input Forward Voltage		T <sub>A</sub> = 25°C	All		1.30	1.7	V
		Each channel (I <sub>F</sub> = 1.6	SmA)				1.75	
BV <sub>R</sub>	Input Reverse Breakdown Voltage	$T_A = 25^{\circ}C, I_R = 10\mu A$		All	5.0	20		V
$\Delta V_F / \Delta T_A$	Temperature Coefficient of Forward Voltage	I <sub>F</sub> = 1.6mA		All		-1.8		mV/°C
DETECTO	R			•	•		•	
I <sub>OH</sub>	Logic HIGH Output	$I_F = 0$ mA, $V_O = V_{CC} =$	18V	6N139		0.01	100	μA
	Current		Each Channel	HCPL2731				
		$I_F = 0mA$ , $V_O = V_{CC} = 7V$		6N138		0.01	250	
			Each Channel	HCPL2730				
I <sub>CCL</sub>	Logic LOW supply	$I_F = 1.6$ mA, $V_O = Open$	n, V <sub>CC</sub> = 18V	6N138, 6N139		0.4	1.5	mA
		I <sub>F1</sub> = I <sub>F2</sub> = 1.6mA, V <sub>CC</sub> = 18V		HCPL2731		1.3	3	
		V <sub>O1</sub> – V <sub>O2</sub> = Open, V <sub>CC</sub> = 7V		HCPL2730				
I <sub>CCH</sub>	Logic HIGH Supply	$I_F = 0$ mA, $V_O = 0$ pen, $V_{CC} = 18V$		6N138, 6N139		0.05	10	μA
		I <sub>F1</sub> = I <sub>F2</sub> = 0mA, V <sub>CC</sub> = 18V		HCPL2731		0.10	20	
		$V_{O1} - V_{O2} = Open, V_{C}$	$V_{O1} - V_{O2} = Open, V_{CC} = 7V$					

### **Transfer Characteristics**

Symbol	Parameter	Test Conditions		Device	Min.	Typ.*	Max.	Unit
COUPLE	D					l	l	
CTR Current Transfer		$I_F = 0.5 \text{mA}, V_O = 0.4$	$I_F = 0.5 \text{mA}, V_O = 0.4 \text{ V}, V_{CC} = 4.5 \text{V}$		400	1100		%
	Ratio <sup>(1)(2)</sup>		Each Channel	HCPL2731		3500		
		$I_F = 1.6 \text{mA}, V_O = 0.4$	V, V <sub>CC</sub> = 4.5V	6N139	500	1300		
		Each Channel	HCPL2731		2500			
		I <sub>F</sub> = 1.6mA, V <sub>O</sub> = 0.4 V, V <sub>CC</sub> = 4.5V		6N138	300	1300		
			Each Channel	HCPL2730	1	2500		
V <sub>OL</sub>	Logic LOW Output	$I_F = 0.5 \text{mA}, I_O = 2 \text{mA}, V_{CC} = 4.5 \text{V}$		6N139		0.08	0.4	V
	Voltage <sup>(2)</sup>	I <sub>F</sub> = 1.6mA, I <sub>O</sub> = 8mA, V <sub>CC</sub> = 4.5V		6N139		0.01	0.4	
			Each Channel	HCPL2731			//	
		$I_F = 0.5 \text{mA}, I_O = 15 \text{m}.$	I <sub>F</sub> = 0.5mA, I <sub>O</sub> = 15mA, V <sub>CC</sub> = 4.5V		0.13	0.4		
			Each Channel	HCPL2731				
		$I_F = 12mA, I_O = 24mA$	I <sub>F</sub> = 12mA, I <sub>O</sub> = 24mA, V <sub>CC</sub> = 4.5V			0.20	0.4	
			Each Channel	HCPL2731	1			
		I <sub>F</sub> = 1.6mA, I <sub>O</sub> = 4.8m	nA, V <sub>CC</sub> = 4.5V	6N138		0.10	0.4	
			Each Channel	HCPL2730	1			

<sup>\*</sup>All Typicals at  $T_A = 25^{\circ}C$ 

## **Electrical Characteristics** (Continued) ( $T_A = 0$ to $70^{\circ}$ C unless otherwise specified)

Switching Characteristics ( $V_{CC} = 5V$ )

Symbol	Parameter	Test Condit	ions	Device	Min.	Тур.*	Max.	Unit
T <sub>PHL</sub>	Propagation Delay	$R_L = 4.7\Omega, I_F = 0.5 \text{mA}$		6N139			30	μs
	Time to Logic LOW <sup>(2)</sup> (Fig. 24)		T <sub>A</sub> = 25°C			4	25	
	LOVV (Fig. 24)	$R_L = 4.7\Omega, I_F = 0.5 \text{mA}$		HCPL2731			120	•
		Each Channel	T <sub>A</sub> = 25°C			3	100	
		$R_L = 270\Omega, I_F = 12mA$	•	6N139			2	•
			T <sub>A</sub> = 25°C			0.2	1	
		$R_L = 270\Omega, I_F = 12mA, E$	ach Channel	HCPL2730			3	
			T <sub>A</sub> = 25°C	HCPL2731		0.3	2	
		$R_L = 2.2\Omega, I_F = 1.6 \text{mA}$		6N138			15	
			T <sub>A</sub> = 25°C			1.5	10	
		$R_L = 2.2\Omega$ , $I_F = 1.6$ mA, Each Channel		HCPL2731			25	
		T <sub>A</sub> = 25°C	HCPL2730		1	20		
T <sub>PLH</sub>	Propagation Delay	$R_L = 4.7\Omega, I_F = 0.5 \text{mA}$		6N139			90	μs
	Time to Logic HIGH <sup>(2)</sup> (Fig. 24)		Each Channel	HCPL2731				
		$R_L = 4.7\Omega, I_F = 0.5 \text{mA}, T_A = 25^{\circ}\text{C}$		6N139		12	60	
			Each Channel	HCPL2731		22		
		$R_L = 270\Omega$ , $I_F = 12mA$		6N139			10	
			T <sub>A</sub> = 25°C			1.3	7	
		$R_L = 270\Omega$ , $I_F = 12mA$ , E	ach Channel	HCPL2730			15	
			T <sub>A</sub> = 25°C	HCPL2731		5	10	
		$R_L = 2.2\Omega, I_F = 1.6 \text{mA}$		6N138			50	
			Each Channel	HCPL2730/1				
		$R_L = 2.2\Omega$ , $I_F = 1.6$ mA, $T_A$	<sub>A</sub> = 25°C	6N138		7	35	
			Each Channel	HCPL2730/1		16		
ICM <sub>H</sub> I Common Mode Transient		$I_F = 0$ mA, $IV_{CM}I = 10V_{P-F}I_{CM}I = 2.2\Omega$	$_{o}$ , $T_{A} = 25^{\circ}C$ ,	6N138 6N139	1,000	10,000		V/µs
Immunity at Logic HIGH <sup>(3)</sup> (Fig. 25)		Each Channel	HCPL2730 HCPL2731					
ICM <sub>L</sub> I Common Mode Transient		$(I_F = 1.6 \text{mA},  V_{CM}  = 10 V_{P-P}, R_L = 2.2 \Omega)$ $T_A = 25 ^{\circ}\text{C}$		6N138 6N139	1,000	10,000		V/µs
Immunity at Logic LOW <sup>(3)</sup> (Fig. 25)		Each Channel	HCPL2730 HCPL2731					

<sup>\*\*</sup> All Typicals at  $T_A = 25^{\circ}C$ 

## Electrical Characteristics (Continued) (T<sub>A</sub> = 0 to 70°C unless otherwise specified)

#### **Isolation Characteristics**

Symbol	Characteristics	Test Conditions		Тур.*	Max.	Unit
I <sub>I-O</sub>	Input-Output Insulation Leakage Current <sup>(4)</sup>	Relative humidity = $45\%$ , $T_A = 25$ °C, $t = 5$ s, $V_{I-O} = 3000$ VDC			1.0	μA
V <sub>ISO</sub>	$ \begin{array}{ll} \mbox{Withstand Insulation Test} & \mbox{RH} \leq 50\%, \mbox{T}_{\mbox{A}} = 25^{\circ}\mbox{C}, \mbox{ I}_{\mbox{I-O}} \leq 2\mu\mbox{A}, \\ \mbox{Voltage}^{(4)} & \mbox{t} = 1 \mbox{ min}. \end{array} $		2500			V <sub>RMS</sub>
R <sub>I-O</sub>	Resistance (Input to Output) <sup>(4)</sup>	V <sub>I-O</sub> = 500VDC		10 <sup>12</sup>		Ω
C <sub>I-O</sub>	Capacitance (Input to Output) <sup>(4)(5)</sup>	f = 1MHz		0.6		pF
l <sub>I-I</sub>	Input-Input Insulation Leakage Current <sup>(6)</sup>	$RH \le 45\%$ , $V_{I-I} = 500VDC$ , $t = 5s$ , $HCPL2730/2731$ only		0.005		μA
R <sub>I-I</sub>	Input-Input Resistance <sup>(6)</sup>	V <sub>I-I</sub> = 500VDC, HCPL2730/2731 only		10 <sup>11</sup>		Ω
C <sub>I-I</sub>	Input-Input Capacitance <sup>(6)</sup>	f = 1MHz, HCPL2730/2731 only		0.03		pF

<sup>\*</sup>All Typicals at  $T_A = 25$ °C

#### Notes:

- Current Transfer Ratio is defined as a ratio of output collector current, I<sub>O</sub>, to the forward LED input current, I<sub>E</sub>, times 100%.
- 2. Pin 7 open. (6N138 and 6N139 only)
- 3. Common mode transient immunity in logic HIGH level is the maximum tolerable (positive) dV<sub>cm</sub>/dt on the leading edge of the common mode pulse signal V<sub>CM</sub>, to assure that the output will remain in a logic HIGH state (i.e., V<sub>O</sub> > 2.0V). Common mode transient immunity in logic LOW level is the maximum tolerable (negative) dV<sub>cm</sub>/dt on the trailing edge of the common mode pulse signal, V<sub>CM</sub>, to assure that the output will remain in a logic LOW state (i.e., V<sub>O</sub> < 0.8V).</p>
- 4. Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.
- 5. For dual channel devices, C<sub>I-O</sub> is measured by shorting pins 1 and 2 or pins 3 and 4 together and pins 5 through 8 shorted together.
- 6. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.

# **Electrical Characteristics** (Continued) $T_A = 25$ °C unless otherwise specified)

**Current Limiting Resistor Calculations** 

$$R_1 \text{ (Non-Invert)} = \underbrace{V_{DD1} - V_{DF} - V_{OL1}}_{I_F}$$

$$R_1 \text{ (Invert)} = V_{DD1} - V_{OH1} - V_{DF}$$

$$\mathsf{R}_2 = \underbrace{\mathsf{V}_{\mathsf{DD2}} = \mathsf{V}_{\mathsf{OLX}} \left( @ \ \mathsf{I}_{\mathsf{L}} - \mathsf{I}_{\mathsf{2}} \right)}_{\mathsf{I}_{\mathsf{L}}}$$

#### Where:

 $V_{DD1}$  = Input Supply Voltage

V<sub>DD2</sub> = Output Supply Voltage

V<sub>DF</sub> = Diode Forward Voltage

V<sub>OL1</sub> = Logic "0" Voltage of Driver

V<sub>OH1</sub> = Logic "1" Voltage of Driver

I<sub>F</sub> = Diode Forward Current

V<sub>OLX</sub> = Saturation Voltage of Output Transistor

I<sub>L</sub> = Load Current Through Resistor R2

I<sub>2</sub> = Input Current of Output Gate

						OUTPU	Т		
IN	INPUT		CMOS @ 5V	CMOS @ 10V	74XX	74LXX	74SXX	74LSXX	74HXX
			R2 (V)	R2 (V)	R2 (V)	R2 (V)	R2 (V)	R2 (V)	R2 (V)
CMOS	NON-INV.	2000	1000	2200	750	1000	1000	1000	560
@ 5V	INV.	510							
CMOS	NON-INV.	5100							
@ 10V	INV.	4700							
74XX	NON-INV.	2200							
	INV.	180							
74LXX	NON-INV.	1800							
	INV.	100							
74SXX	NON-INV.	2000							
	INV.	360							
74LSXX	NON-INV.	2000							
	INV.	180							
74HXX	NON-INV.	2000							
	INV.	180							

Fig. 1 Resistor Values for Logic Interface

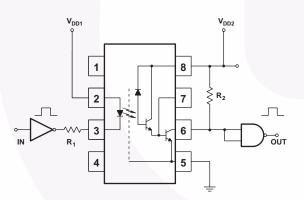


Fig. 2 Non-Inverting Logic Interface

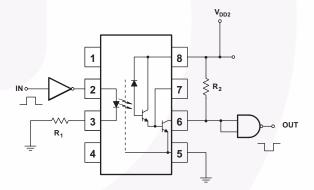


Fig. 3 Inverting Logic Interface

## **Typical Performance Curves**

Fig. 4 LED Forward Current vs. Forward Voltage

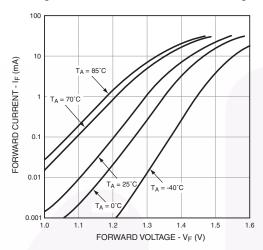


Fig. 6 Non-saturated Rise and Fall Times vs. Load Resistance (6N138 / 6N139 Only)

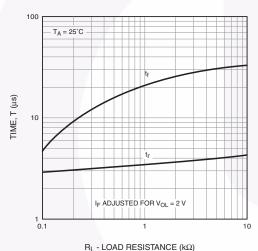


Fig. 8 Propagation Delay To Logic Low vs. Base-Emitter Resistance (HCPL2730 / HCPL2731 Only)

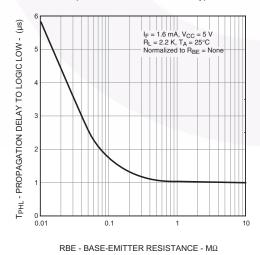


Fig. 5 LED Forward Voltage vs. Temperature

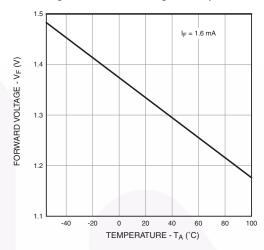


Fig. 7 Non-saturated Rise and Fall Times vs. Load Resistance (HCPL2730 / HCPL2731 Only)

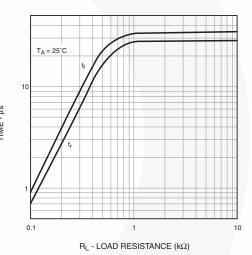
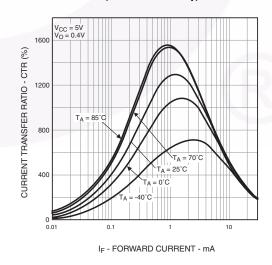
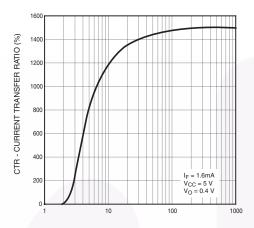


Fig. 9 Current Transfer Ratio vs. Forward Current (6N138 / 6N139 Only)



## Typical Performance Curves (Continued)

Fig. 10 Current Transfer Ratio vs. Base-Emitter Resistance (6N138 / 6N139 Only)



 $\mbox{R}_{\mbox{\footnotesize{BE}}}$  -  $\mbox{\footnotesize{BASE}}$  RESISTANCE (k\$\Omega)

Fig. 12 Output Current vs Output Voltage (6N138 / 6N139 Only)

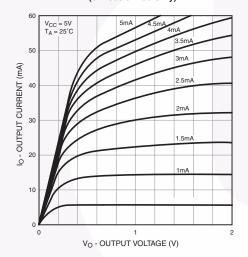


Fig. 14 Output Current vs. Input Diode Forward Current (6N138 / 6N139 Only)

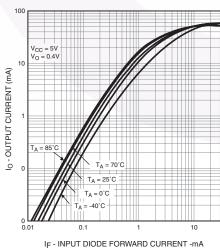


Fig. 11 Current Transfer Ratio vs. Forward Current (HCPL2730 / HCPL2731 Only)

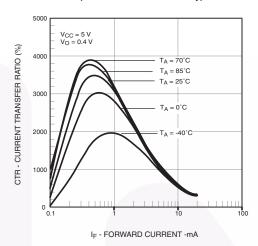


Fig. 13 Output Current vs Output Voltage (HCPL2730 / HCPL2731 Only)

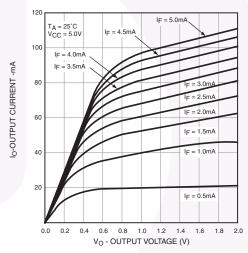
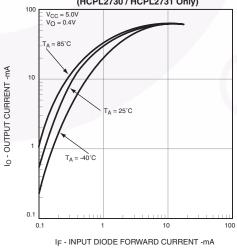


Fig. 15 Output Current vs Input Diode Forward Current (HCPL2730 / HCPL2731 Only)



## **Typical Performance Curves** (Continued)

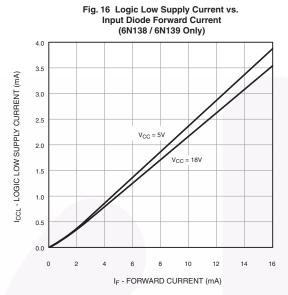


Fig. 17 Logic Low Supply Current vs. Input Diode Forward Current (HCPL2730 / HCPL2731 Only)

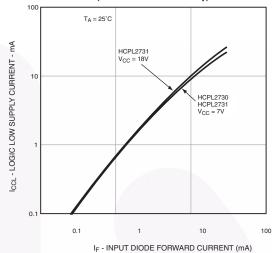


Fig. 18 Propagation Delay vs. Input Diode Forward Current (6N138 / 6N139 Only)

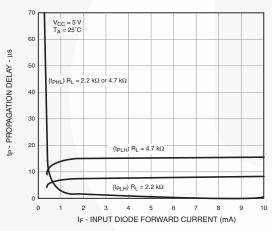


Fig. 19 Propagation Delay vs. Input Diode Forward Current (HCPL2730 / HCPL2731 Only)

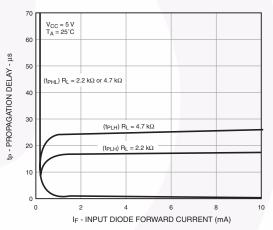


Fig. 20 Propagation Delay to Logic Low vs. Pulse Period (6N138 / 6N139 Only)

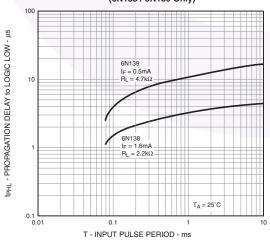
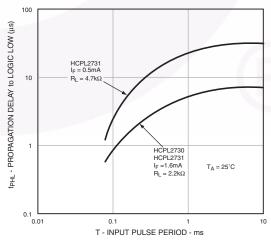


Fig. 21 Propagation Delay to Logic Low vs. Pulse Period (HCPL2730 / HCPL2731 Only)



## Typical Performance Curves (Continued)

Fig. 22 Propagation Delay vs. Temperature (6N138 / 6N139 Only)

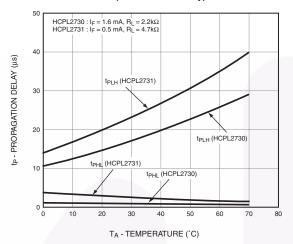
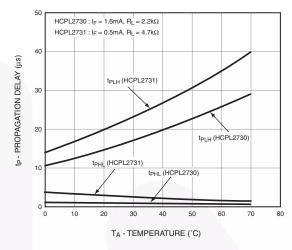
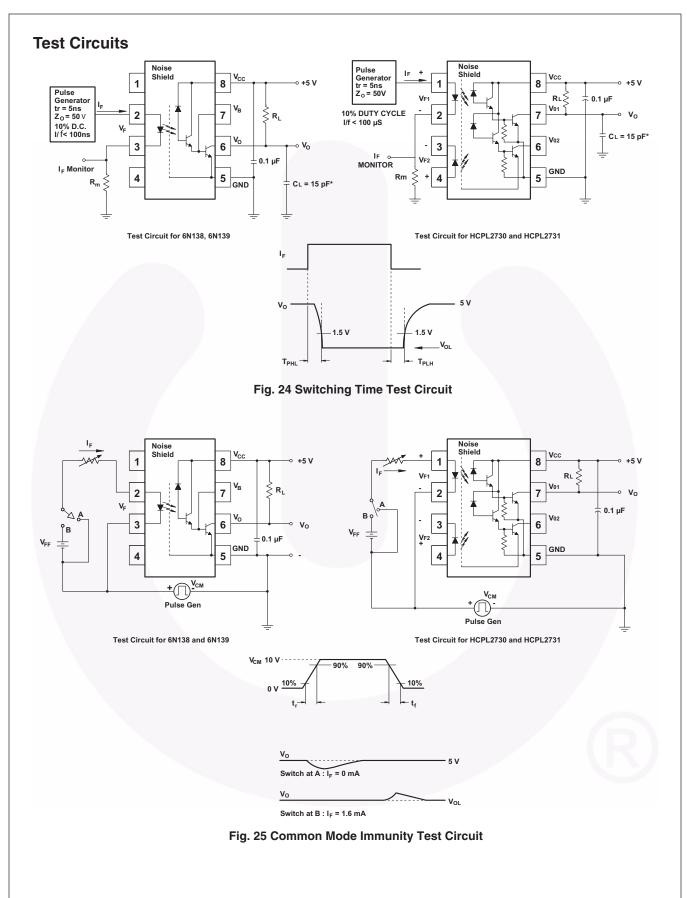


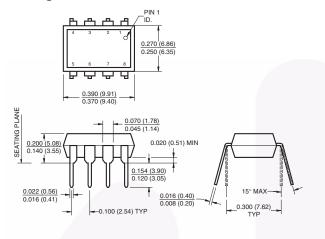
Fig. 23 Propagation Delay vs. Temperature (HCPL2730 / HCPL2731 Only)



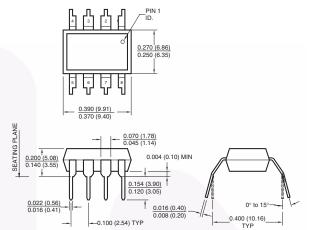


## **Package Dimensions**

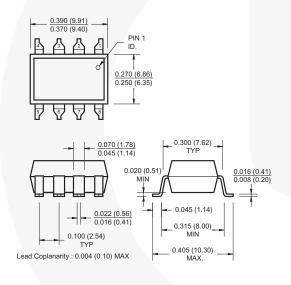
## **Through Hole**



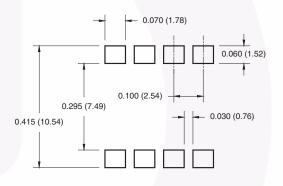
### 0.4" Lead Spacing



#### **Surface Mount**



#### 8-Pin DIP - Land Pattern



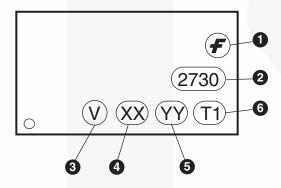
#### Note

All dimensions are in inches (millimeters)

## **Ordering Information**

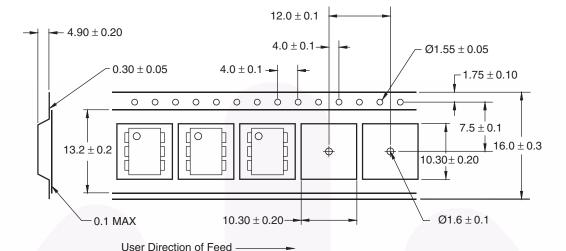
Option	Example Part Number	Description
No Suffix	6N138	Standard Through Hole Device, 50 pcs per tube
S	6N138S	Surface Mount Lead Bend
SD	6N138SD	Surface Mount; Tape and reel
W	6N138W	0.4" Lead Spacing
V	6N138V	VDE0884
WV	6N138WV	VDE0884; 0.4" lead spacing
SV	6N138SV	VDE0884; surface mount
SDV	6N138SDV	VDE0884; surface mount; tape and reel

## **Marking Information**

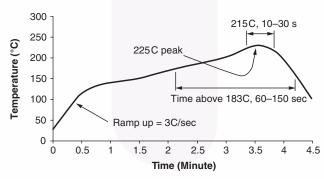


Definiti	Definitions					
1	1 Fairchild logo					
2	Device number					
3	VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table)					
4	Two digit year code, e.g., '07'					
5	Two digit work week ranging from '01' to '53'					
6	Assembly package code					

## **Tape Specifications**



## **Reflow Profile**



- Peak reflow temperature: 225C (package surface temperature)
   Time of temperature higher than 183C for 60–150 seconds
   One time soldering reflow is recommended





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#### Definition of Terms

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