PWM VOLTAGE SOURCE INVERTER BASED STATIC VAr COMPENSATORS (SVC) FOR POWER QUALITY ENHANCEMENT

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1. Introduction

PWM Voltage Source Inverter based Static VAr Compensators (referred to as SVC here onwards) began to be considered a viable alternative to the existing passive shunt compensators and Thyristor Controlled Reactor (TCR) based compensators from mid-eighties onwards. The disadvantages of capacitor/inductor compensation are well known. TCRs could overcome many of the disadvantages of passive compensators. However they suffered from two major disadvantages ;namely slow response to a VAr command and injection of considerable amount of harmonic currents into the power system which had to be cancelled by special transformers and filtered by heavy passive filters.

It became clear in the early eighties that apart from the mundane job of pumping lagging/leading VArs into the power system at chosen points ,VAr generators can assist in enhancing stability of the power system during large signal and small signal disturbances if only they were faster in the time domain. Also ,they can provide reactive support against a fluctuating load to maintain the bus voltage regulation and to reduce flicker problems,provide reactive support to control bus voltages against sag and swell conditions and provide reactive support to correct the voltage unbalance in the source – if only they were fast enough. PWM SVCs covered in this lecture are capable of delivering lagging/leading VArs to a load or to a bus in the power system in a rapidly controlled manner.

High Power SVCs of this type essentially consist of a three phase PWM Inverter using GTOs,Thyristors or IGBTs, a D.C. side capacitor which provides the D.C. voltage required by the inverter,filter components to filter out the high frequency components of inverter output voltage,a link inductor which links the inverter output to the a.c supply side,interface magnetics (if required) and the related control blocks. The Inverter generates a three-phase voltage, which is synchronized with the a.c supply ,from the D.C. side capacitor and the link inductance links up this voltage to the a.c source. The current drawn by the Inverter from the a.c supply is controlled to be mainly reactive(leading or lagging as per requirement) with a small active component needed to supply the losses in the Inverter and Link Inductor (and in the magnetics,if any).The D.C. side capacitor voltage is maintained constant(or allowed to VAry with a definite relationship maintained between its value and the reactive power to be delivered by the Inverter) by controlling this small active current component. The currents are controlled indirectly by controlling the phase angle of Inverter output Voltage with respect to the a.c side source voltage in the "Synchronous Link Based Control Scheme" whereas they are controlled directly by current feedback in the case of "Current Controlled Scheme".In the latter case the Inverter will be a Current Regulated one ,i.e. its switches are controlled in such a way that the Inverter delivers a commanded current at its output rather than a commanded voltage (the voltage required to see that the commanded current flows out of Inverter will automatically be synthesized by the Inverter).Current Control Scheme results in a very fast SVC which can adjust its reactive output within microseconds of a sudden change in the reactive demand.

However,current control schemes will require high frequency switching in the Inverter – switching frequencies which are so high that low frequency devices like thyristors and GTOs are ruled out. Hence they have to be based on MOSFETS or IGBTS.The latter seems to be the current choice with its high voltage and high current rating availability with low conduction losses. However, at present, they are limited to applications in the low voltage systems (400V,1.1kV etc) and at distribution power level rather than transmission and sub-transmission power levels. This is because of the limited maximum voltage/current ratings available in a single device/module.

When it comes to transmission/sub-transmission level GTOs are the preferred devices and they can take switching frequencies below 1-3 kHz. Hence ,at these levels,SVCs are made with the Synchronous Link Control Scheme which gates the Inverter to deliver a voltage output (rather than a regulated current).This kind of Inverter operation makes it possible to implement one of the many specialized PWM switching schemes aimed at minimizing the switching frequency while keeping acceptable level of harmonic content in the Inverter output.

Summing up,SVCs are fast responding generators of reactive power with leading VAr/lagging VAr capability which can provide steady state reactive compensation as well as dynamic compensation during power system transients,sags, swells,flicker etc. Thereby they can contribute significantly to enhancement of Power Quality.High Power SVCs are usually made with devices of low switching frequency capability and hence need special PWM patterns to optimize switching behaviour. Such SVCs use Synchronous Link principle in the control blocks. This lecture deals with this kind of SVCs.*The reader is urged to go through the lecture notes on Synchronous Link based Single Phase PWM Rectifier (pages 70-75) before reading on. Much of what was discussed there is relevant in the SVC context too.*

2. The Basic Principle of Synchronous Link Based SVC

In a synchronous link where two a.c sources of same frequency are connected together by means of a link inductor, active power flows from the leading bus to the lagging one and reactive power flows from the source with higher voltage magnitude to the one with lower voltage magnitude. The active power flow is almost entirely decided by the lead angle whereas the reactive flow is almost entirely decided by the difference in voltage magnitudes provided the inductor is loss free ,the lead angle is small (less than 15 degrees) and the voltage magnitude difference is small(less than 0.1 p.u) . The situation changes slightly if the link contains resistance. If two sources V1 with a phase angle of $\propto$ and V2 with a phase angle of 0 are connected together by means of an inductive link of impedance (R+jX) ohms and if the active power flowing into the source V2 is constrained to be zero (because this represents the SVC situation) the power delivered by the source V1 (which will not be zero and it will be equal to the power absorbed by the resistance in the link) and *the reactive power delivered to the link by the source V2* will be given by the following relations (after a little algebra along with the assumptions that $\propto$ is small and R << X).

Active Power Delivered by V1,P = $(V1^2/R) \propto^2$ *Watts* ---------- (1)

Reactive Power Delivered by V2,Q = $(V1V2/R) \propto$ *VArs* --------- (2)

Also , *Q* = *V2(V2-V1)/X VArs*

where the powers are for a phase and voltages have phase values. These relations can be used upto about 20 degrees for $\propto$.Active Power drawn from the source V1 is independent of sign of phase angle (only V1 can supply losses in R because of the zero active power constraint at V2) whereas the reactive power delivered by V2 is directly proportional to the phase angle. In the SVC context,the source V1 is the power system voltage at the bus where the SVC is connected,V2 is the a.c voltage generated by the Inverter in the SVC, R is the total loss resistance in the link comprising the winding losses in the link inductor,interface magnetics and the inverter switches and snubbers etc. It is also possible to derive the following useful relationships in this context.

The Phase Angle of V1 w.r.t V2 ,$\propto$ = *(R/X) (V2-V1)/V1* --------- (3)

This shows that the relative phase angle is linearly related to the voltage magnitude difference (for small differences) and hence the reactive power delivered by V2 is proportional to the voltage magnitude difference. Thus Q is proportional to $\propto$ or equivalently to (V2-V1). Both points of view will be useful later to understand the two different ways in which this SVC can be controlled.

In the SVC, the required a.c voltage source V2 is generated by inverting the D.C. voltage, which is assumed available across the capacitor in the D.C. side. But if the active power which goes into the inverter from the mains is kept zero, the initially charged capacitor will soon discharge down to zero due to active power losses in the Inverter which the D.C. side will have to supply. The D.C. side voltage will remain constant (or at least controlled) if the power drawn from mains is just enough to supply all the losses which take place everywhere due to the flow of demanded reactive current. The following relation may be derived for the D.C. side ca voltage under this condition.

The D.C. side voltage ,Vd = *(V1/k)(1-(X/R)* $\propto$*) volts* --------- (4)

Where V1 is the rms phase voltage of a.c mains,k is a constant, which also absorbs the modulation index of PWM process in the Inverter.

From the relations cited above two control strategies emerge for the control of a Synchronous Link Based SVC.They are described below. The reference signal to the controller is assumed to be the desired reactive power flow from the SVC.

1. Keep the D.C. side voltage constant by controlling the value of $\propto$.And control the reactive power from the inverter by directly changing (V2-V1) by controlling the modulation depth (i.e. the multiplication factor that comes between the D.C. voltage and the amplitude of a.c output in the Inverter).It should be obvious from the equations 1 to 4 that this strategy will result in an interacting control system.
2. Let the D.C. side voltage vary according to equation(4) and use $\propto$ control to control the reactive power delivered by the SVC.There is only one control variable and that is $\propto$.The modulation index of the Inverter is kept constant and D.C. voltage is allowed to vary. The D.C. voltage increases when the SVC delivers increasing lagging VAr and it decreases when SVC delivers leading VArs.Here the control of VAr is indirect. When the reactive power reference changes, it causes a change in $\propto$ value. The residual voltage across link inductor changes resulting in more active power flow into/out of the Inverter.Increased active power flow into/out of the Inverter results in increase/decrease in the energy storage in the D.C. side capacitor resulting in an increase/decrease in the D.C. side voltage. With a fixed modulation index ,the increase/decrease in the D.C. voltage is straight away passed on to Inverter output voltage V2.Change in the Inverter output voltage results in the desired reactive power change. Obviously the response time is decided by the link inductor and D.C. side capacitor and will be relatively slow.

   In the constant D.C. voltage scheme, the D.C. voltage dynamics is going to be slow since the same mechanism described above will be responsible for maintaining the D.C. voltage. However,the

reactive power flow is controlled by controlling V2 directly by changing the modulation index of the Inverter and this dynamics can be fast. The components which decide the dynamics will be the loss resistance,link inductor value,Inverter filter components and the feed back system parameters.

3. The Inverter and Programmed Harmonic Elimination PWM

A Three-Phase Inverter using IGBTs is shown in Fig.1.In certain cases the neutral wire may not be present and the D.C. side capacitor may be a single one. However, for the purpose of explanation, a neutral point may always be imagined. With this the three phase Inverter becomes three separate single-phase half bridge Inverters sharing the same D.C. source. Bipolar and unipolar PWM schemes using a triangular carrier frequency was discussed in another lecture (page 70-72) in the context of single-phase full bridge converters. Much of the same is applicable here too except that only bipolar PWM is possible for a half bridge topology since no combination of switching patterns for the upper and lower switches of a half bridge can apply zero potential at the load point. Bipolar PWM using a triangular carrier and sinusoidal modulating voltage can be applied here with the modulating waves of the three half bridge sections forming a balanced three phase signal set.

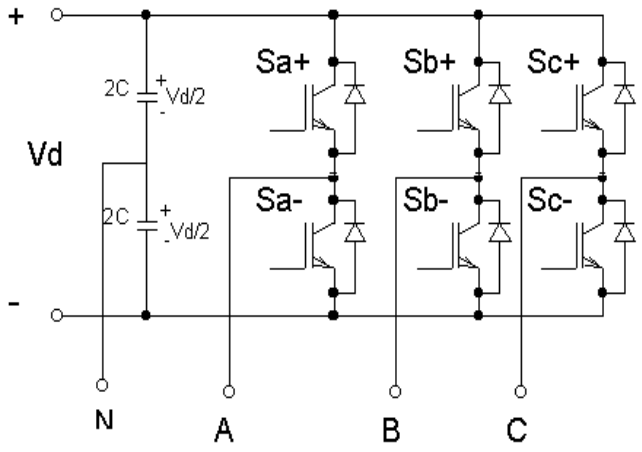

Fig.1 A Three Phase Inverter Circuit

However,the switching frequency required in Sinusoidal Pulse Width Modulation using triangular Carrier to achieve reduction in output harmonics is usually excessive as far as high power devices like GTOs are concerned. Hence, programmed harmonic elimination techniques is preferred at high power levels.

Like in any other PWM scheme, +Vd/2 and –Vd/2 pulses are applied across the load in the programmed harmonic elimination technique also. But in this scheme the position and duration of these pulses are pre-calculated off-line in such a way that (i) certain chosen harmonics are completely eliminated completely in the output and (ii) the fundamental component of the output has a desired value. By a general formulation of Fourier series coefficients of a pulse wave it is possible to derive a set of equations involving angle positions of the positive and negative pulses to satisfy the conditions on elimination of chosen harmonics and on the fundamental amplitude. The maximum possible amplitude will be available when the output is a full square wave(i.e. no harmonics are eliminated) and will be 1.275(Vd/2).But when harmonics are to be eliminated it is not possible to reach this value of fundamental voltage. For every selection of harmonics to be eliminated there exists a maximum value the fundamental component can have and it will be less than 1.275(Vd/2).For example ,it is 1.188(Vd/2) for a scheme where fifth and seventh harmonics are eliminated.Fig.2 shows the normalized pulse pattern which appears at A phase output when fifth and seventh harmonics are sought to be eliminated. The switching frequency of each will be 350Hz with this pattern.

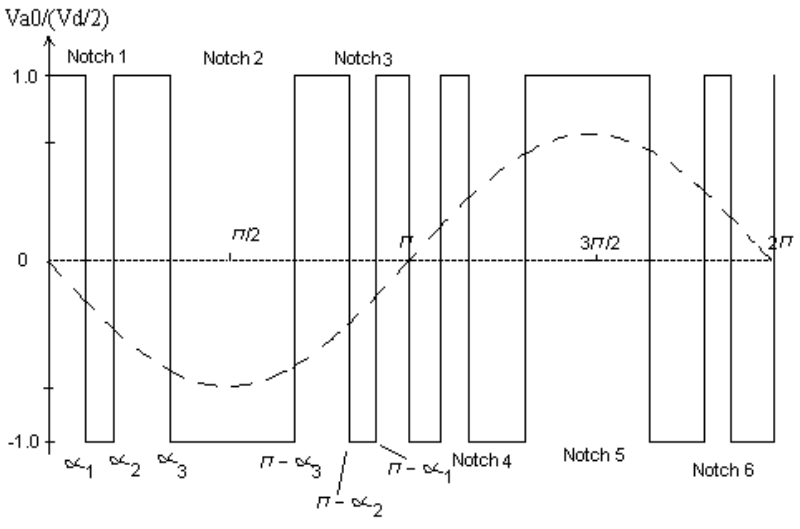

Fig.2. Programmed Harmonic Elimination of Fifth and Seventh Harmonics

The equations which yield the angular positions for a chosen elimination format and fundamental amplitude is transcendental algebraic in nature and require numerical techniques for solution. Moreover for the same harmonic elimination format the switching angles will vary with the fundamental amplitude desired;and the variation can be highly nonlinear. See Fig.3.The nature of equations make an on-line implementation of pattern generation very difficult. In addition, the nonlinear angular position

variation with changes in the desired fundamental component makes it difficult to generate the PWM pattern in real time by analog/digital logic. However, it is possible to implement this scheme using micro processors/controllers and EPROMs.

A sinusoidal reference wave at frequency equal to the desired output frequency of the Inverter is frequency multiplied in a PLL system. The square wave from VCO of PLL is used to clock a UP/DOWN counter. The counter output is used as address bytes of an EPROM which has the required switching pattern at that instant written in it(by off-line computation and EPROM programming).The EPROM has patterns stored for various quantised values of fundamental amplitude. The control signal which sets the fundamental amplitude is A/D converted and the code is used to decide the range of EPROM memory locations to be read out by the counter output. Once in a fundamental cycle the counter is forcibly reset (at zero crossing of reference sine wave usually), to avoid subharmonic components in the output due to jitter in the PLL and other similar errors everywhere. Note that it is possible to shift the phase of the fundamental component of Inverter output with respect to reference sine by shifting the counter reset point with respect to the zero crossing point of reference sine. A three-phase pattern can be similarly generated. However, large memory may be required for fine control of output voltage fundamental value.

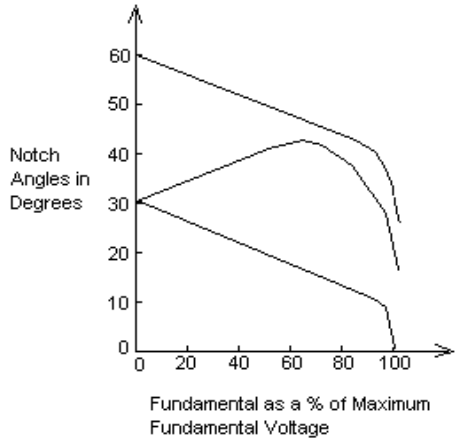

Fig. 3 Programmed Harmonic Elimination of fifth & seventh harmonics

4. Phase Angle Control of SVC

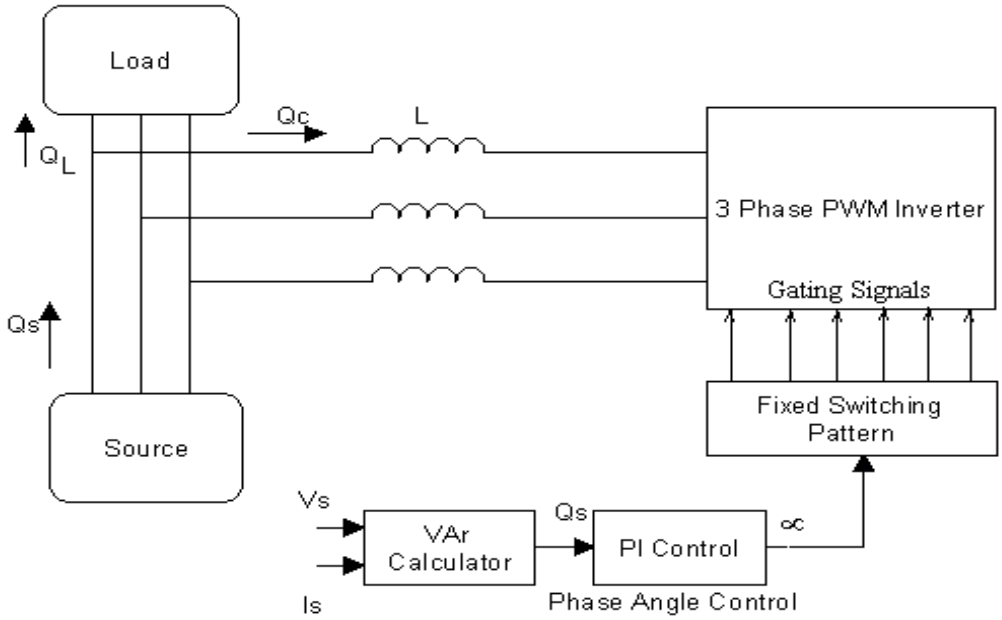

Fig.4. Block Diagram of SVC System with Phase Angle Control Scheme

Fig.4. shows an SVC configured to keep the reactive power delivered by the Source at a zero value as long as the reactive demand from the load is within the SVC rating. Thus, the p.f of the Source will be maintained at unity under steady state conditions by the SVC.The control of SVC reactive power is by pure ∝ control and the D.C. bus voltage is allowed to vary. This scheme, though somewhat slow, results in simplified control hardware.

The source side voltages and currents are sensed and the reactive power is calculated by analog/pulse circuitry. This calculated value is compared with the desired value (usually zero) and the error is processed in a proportional-integral controller. The error output decides the phase shift needed in the inverter output in order to develop the required D.C. bus voltage such that the inverter output voltage magnitude will be sufficient to make the Inverter deliver the VArs required by the load. The Inverter is gated by a fixed PWM

pattern optimised for eliminating chosen harmonics (usually fifth, seventh, eleventh etc; triplen harmonics need not be eliminated since they do not result in current flows in a three wire system). The needed PWM pattern is stored in an EPROM and is read out using the scheme described in the last section. This is by far the most popular scheme used in high power SVCs.

The open loop dynamics of the SVC features a third order transfer function (for small signals) between $\propto$ and Qc, the reactive power delivered by the Inverter.The transfer function has a pair of complex zeros, a real pole and a pair complex poles. Various research workers have derived the following transfer function for the SVC.

$Q_c(s)/\propto(s) = N(s)/D(s)$ where $N(s)=(Vs^2/L)\{s^2+(R/L)s+(k^2/2LC)\}$ and

$D(s)=s^3+(2R/L)s^2+\{(R/L)^2+(k^2/2LC)+\omega^2\}s+(k^2R/2L^2C)$ where all the parameters have the already defined meaning and ω is the system frequency.The step response usually features a rise time ranging from 3-7 cycles of a.c.It is possible to employ a PI controller with suitable gain characteristics to compensate the closed loop system and to obtain a step response rise/fall time between 1 to 3 a.c cycles.

It is not necessary to sense the reactive power in all three phases of the source in the case of balanced operation.However if the source or load is unbalanced all the three phases will have to be monitored to calculate the total source reactive power.But the SVC will be configured to deliver this total demand by dividing it equally among three phases to ensure current balance in SVC.If exact cancellation of reactive power in all the three phases is required under unbalanced conditions a three phase SVC made of three single phase units with entirely independent control will yield better results.

5. SVC with Constant D.C Bus Voltage

The above scheme suffers from the disadvantage of variable D.C. voltage across the Inverter input and sluggish response to changes in reactive demand.The solution is to control the D.C. voltage by phase angle control and to control the reactive power flow by control of modulation index control.Two separate control loops (which interact with each other) are involved here.But by separating the time scale of dynamics it is possible to decouple the interaction to a satisfactory degree.

Control of modulation index i.e. control of fundamental component of inverter output voltage with a constant value of D.C. voltage can not be easily achieved without complex hardware with a large memory requirement as explained before.Hence this scheme of control is better suited for SVCs with Sinusoidal Pulse Width Modulation (SPWM) in the Inverter.While it is true that programmed harmonic elimination is better than SPWM in terms of switching frequency minimisation for a given level of harmonic reduction,SPWM with a synchronised triangle wave carrier at around 2 to 3kHz can be a viable alternative; especially when the fundamental amplitude is to be controlled.This is true even for GTO based inverters using state of the art GTOs.

Only bipolar PWM is possible for a three phase Inverter.Hence SPWM in bipolar format using a triangular carrier in the frequency range of 1 to 3 kHz is assumed in this section.The carrier wave has to be synchronised to the modulating signal (i.e. sine wave) to eliminate subharmonic components in the output.The process of SPWM produces a fundamental component equal to $(Vd/2)(V_{sm}/V_t)$ at the inverter output terminals where V_{sm} is the amplitude of the modulating signal and V_t is the amplitude of the triangle wave.The harmonics are sufficiently shifted in frequency by the PWM process to allow easy filtering.Now the inverter output voltage can be controlled by controlling the amplitude of modulating signal .

Fig.5 shows the block diagram of the SVC with D.C. voltage control.The D.C. voltage is sensed,compared with reference level and the error is processed in a PI controller.The output of the PI controller is converted into a time marker pulse which is time shifted from zero crossing of phase voltage by an amount proportional to the output voltage of PI controller.This time marker pulse will reset the counter in the phase locked sine wave generator and thereby effect phase shift in the Inverter modulating signal .The VAr in the line is calculated in the VAr calculator and this forms the actuating voltage on an analog multiplier which scales up or down the fixed amplitude sine wave generated by PLL-Counter-EPROM-DAC system.The phase shifted and amplitude adjusted sine wave becomes the modulating signal for a SPWM block and the Inverter reproduces the signal at its output after amplification by Vd/2.

The VAr control loop here is essentially of first order due to link inductor and system losses. A high gain PI controller will accelerate the step response of this loop to a level where VAr commands are followed in less than a cycle. The slower voltage control loop will carry out the slow adjustment of phase angle needed to maintain the D.C. voltage constant. A combination of large valued capacitor, low valued inductor, fast VAr control loop and slow D.C. voltage control loop will ensure rapid VAr control with much reduced current amplitude oscillations in the link inductor. This scheme can very effectively provide reactive support during the power system transient conditions and can compensate a highly fluctuating load like an arc furnace.

6. The Reactive Demand Calculator

The speed of response of the SVC is decided by two time delays – the rise time of SVC when a step change is applied to its reactive power command input and the rise time behavior of the reactive demand

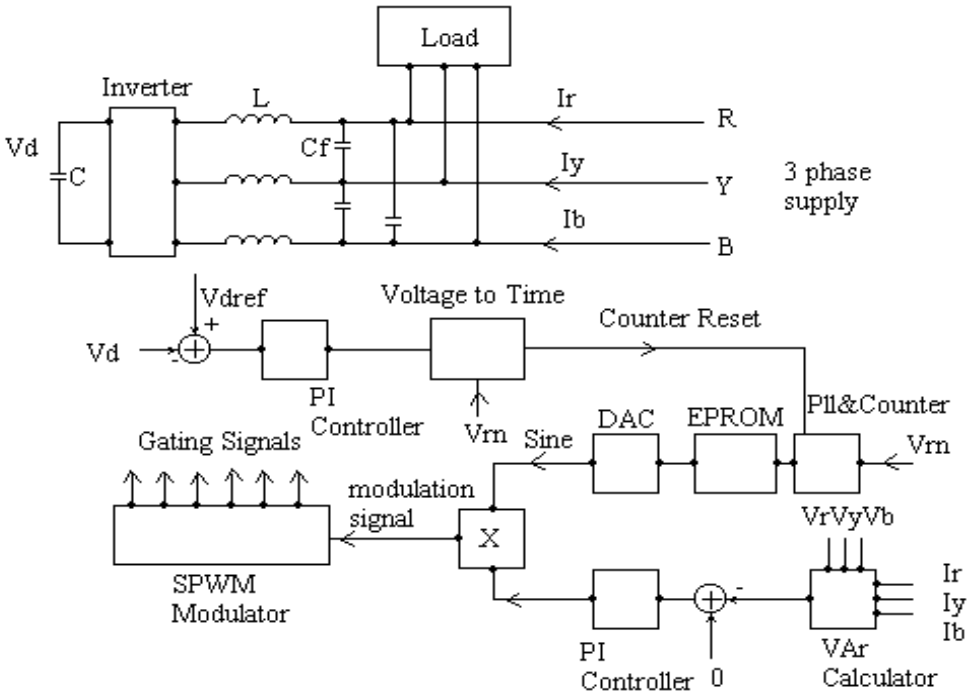

Fig.5. SVC with D.C Voltage Control

calculator when the actual reactive flow in the source line changes suddenly. Hence, the Reactive Power Calculator has to extract the reactive component of the source current rapidly.The reactive command was shown as a VAr flow till now. However, the reactive component of the line current is enough for control purposes. A simple method to extract the reactive content in the current is explained here. Let the source current in one phase be $i(t) = I_0+I_1 \text{ Sin } (\omega t+\theta_1) +I_5 \text{ Sin } (5\omega t+\theta_5) + I_7 \text{ Sin } (7\omega t+\theta_7)+$..... This covers the possibility of a non-linear load which draws harmonic currents and D.C. offsets too. Form the product of this current with unit amplitude cosine wave which is at 90 degrees in phase with that phase voltage. This product signal is called p(t).

$P(t) = I_0 \text{ Cos}\omega t+I_1 \text{ Cos}\omega t \text{ Sin } (\omega t+\theta_1) +I_5 \text{ Cos}\omega t \text{ Sin } (5\omega t+\theta_5) + I_7 \text{ Cos}\omega t \text{ Sin } (7\omega t+\theta_7)+$.....

The integral of this product over integral number of fundamental periods will have content only from $(I_1\text{Sin}\theta_1)/2$ since all other products have zero average over fundamental period.Thus, the strategy is to form this product,integrate it for one period,sample the integrator output and hold the sample,reset the integrator after sampling and allow it integrate the product for the next period.The sampled integrator output will be a quantity proportional to the reactive component of the current.This output can be used as the reactive power signal in the SVC control block.The sampling and integrator reset are performed at zero crossing of sine wave and the product current is taken with the cosine wave.The cosine wave has to be pure,without harmonics.The required sinusoidal templates are obtained by PLL-Counter-EPROM-DAC technique already described.

6. SVCs for PQ Enhancement at Transmission/Subtransmission Level

The SVCs discussed until now were configured for compensating the reactive power taken by a load and for maintaining the utility power factor at unity. Even in this configuration SVC results in PQ enhancement since it can respond rapidly to a rapidly varying load like arc furnace;large hammer mills,stone crushers,ball mills etc;large motors with frequent starts/stops etc.These are potentially troublesome loads from Power Quality point of view.They can cause flicker and sag .Fast responding SVC renders support to bus voltage against these loads.

However, at transmission/subtransmission level the issue of providing voltage support at buses is addressed more directly and SVCs are connected to deliver/take as much reactive power to/from the bus as required to maintain the bus voltage within pre-decided limits. SVC does not try to maintain the power factor at the bus at unity anymore. Rather, it tries to maintain the bus voltage by injecting leading or lagging VArs into the system. In this case there will be an outer control loop which senses the bus voltage, compares it with a set value and processes the error in a PI Controller and sets the reactive reference for the inner control loop. The effectiveness of a given SVC with a specified rating in providing voltage support at a particular bus will depend on the short circuit capacity at that bus. Low value of S.C. capacity implies that the Thevenin's impedance behind the bus voltage is large. In addition, the SVC there will be more effective than similarly rated SVC at another bus with a higher short circuit capacity. But then, a bus with a higher value of short circuit capacity will have better immunity against sags/flickers/swells due to problems elsewhere and hence probably does not need a SVC at all.