November 2,1999

FAIRCHILD SEMICONDUCTOR TM

AN9010

MOSFET Basics

April 1999
R & D 2 Group
Fairchild Korea Semiconductor

CONTENTS

Rev C, November 1999

The Bipolar Power Transistor as a switching device for a power application had few disadvantages and this led to the development of the power MOSFET (Metal Oxide Semiconductor Field Effect Transistor). Power MOSFET is being used in many applications such as SMPS, computer peripherals, automotive, motor control, and etc. in place of BJT, and continuous research led its characteristics to become ideal.

This application note describes general description of power MOSFET and detailed presentation of items of FSC's data book specification.

1. History of Power MOSFETs

The theory of Field Effect Transistor had been advent around 1920~1930 which is 20 years before the Bipolar Junction Transistor has been invented, which is from 1940's and through early 1950s. At that time J.E. Lilienfeld of America suggested a transistor model having two metal contact at each side with metallic plate (Aluminum) on top of the semiconductor. The electric field at the semiconductor surface formed by the voltage supplied at the metallic plate enabled the control of the current flow between the metal contacts, and this was the initial conception of the Field Effect Transistor. But due to the immature semiconductor materials and the technology, the progress of the development was very sluggish. In 1952, W. Shockely introduced JFET (Junction Field Effect Transistors), in 1953, Dacey and Ross materiallized it. In JFET, the metallic plate of Lilienfeld structure was replaced by pn junction, and named the metal contact as source and drain, and also named the field effect electrode as gate. Even though there were continuous research of small-signal MOSFET after that, there was no prominent result for the power MOSFET, and the commercially available products started to come out by 1970s.

History of FSC's Enhancement Type Power MOSFET

In March 1986, FSC formed up a TFT with 9 people, and started the research on the power MOSFET. They started with 60~700V level n-ch power MOSFET development, and in 1987, they successfully developed p-ch power MOSFET. In 1990, 60~200V level logic-level FET and 50~60V level low voltage, low $R_{DS(on)}$ device were developed. In 1991, 800V level, and in 1993, 900V level high voltage MOSFET, and in 1992 current sense FET, and in 1995, 800V level 3~10A sense FET, and in 1996, 600V level 6A low charge MOSFET were developed sequentially. Finally, in 1999 the leading technology of FSC has led to develop Q-FET series.

2. FETs

JFET, MOSFET

1) JFET (Junction Field Effect Transistors)

There are two kinds of JFETs. One is n-channel type and the other is p-channel type. They both control the drain-to-source current by the voltage supplied to the gate. As shown in the Fig. 1 (a), if the bias is not supplied at the gate, the current flows from the drain to the source, and when the bias is supplied at the gate, depletion region begin to grow and reduces the current as shown in Fig. 1 (b). And the reason why the depletion region of the drain is wider than the depletion region of the source is because the reverse bias of the gate and the drain $V_{DG}(=V_{GS}+V_{DS})$ is higher than the V_{GS} (bias between the gate and the source).

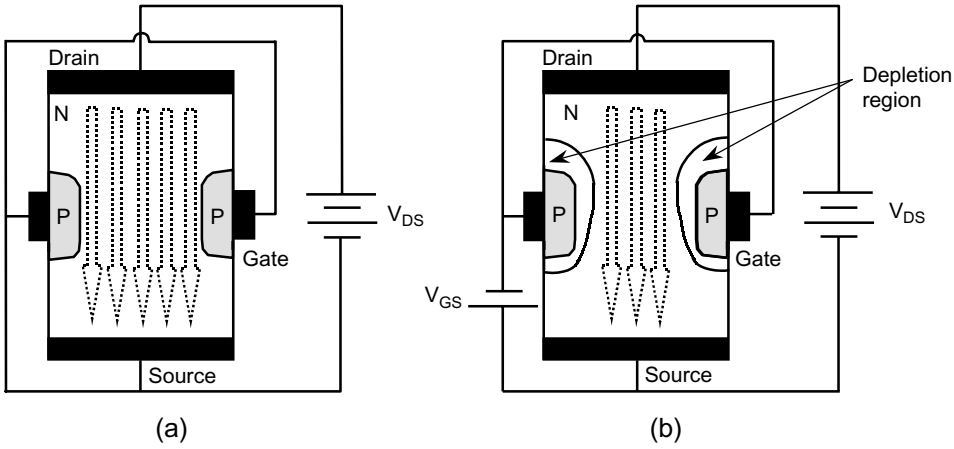


Fig. 1. The structure of JFET and its operation

(a) When V_{GS} (Gate-source voltage) has not been supplied
(b) When V_{GS} (Gate-source voltage) has been supplied

2) MOSFET (Metal Oxide Semiconductor Field Effect Transistors)

There are depletion type and enhancement type, and each has n / p – channel type. The depletion type is normally on, and operates as JFET (Refer to Fig. 2). And the enhancement type is normally off, which means that the drain – t o – source current increases as the voltage at the gate increases. And no current flows when there are no voltage supplied at the gate (Refer to Fig.3).

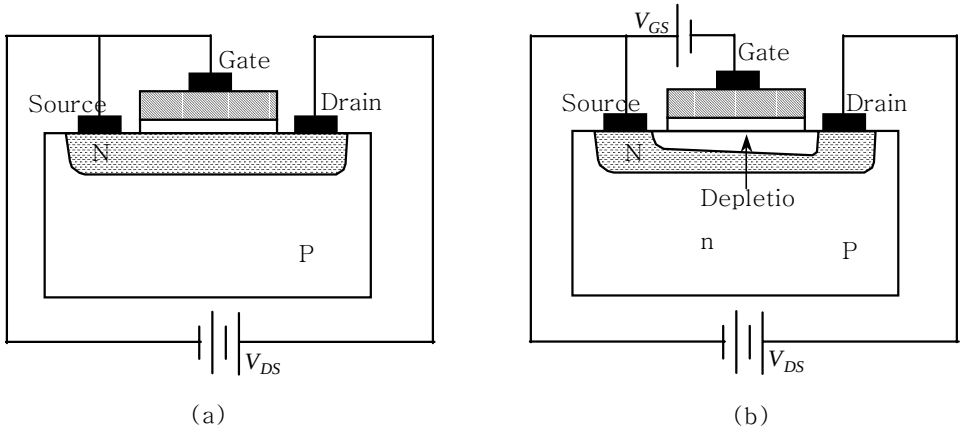


Fig. 2. The structure of depletion type MOSFET and its operation

(a) When V_{GS} (Gate-source voltage) has not been supplied
(b) When V_{GS} (Gate-source voltage) has been supplied

Rev C, November 1999

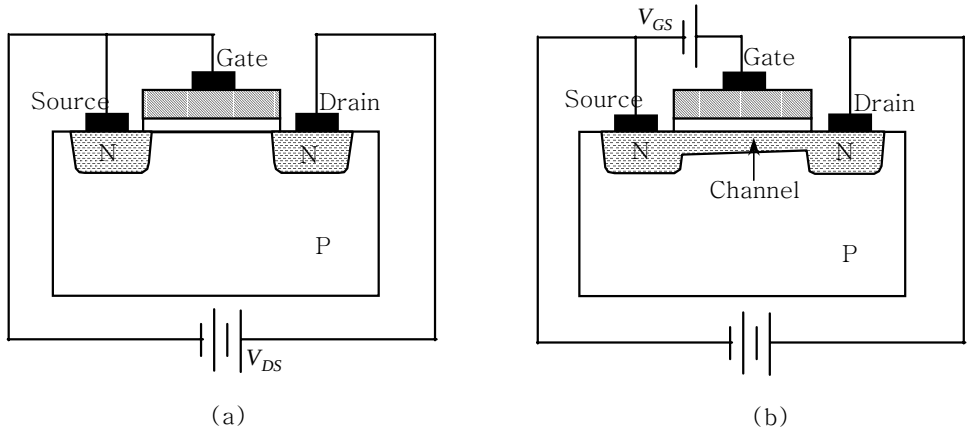


Fig. 3. The structure of enhancement type MOSFET and its operation

(a) When V_{GS} (Gate-source voltage) has not been supplied
(b) When V_{GS} (Gate-source voltage) has been supplied

3. The structure of MOSFET

1) Lateral Channel Structure

All the drain, gate, and the source terminal are placed on the surface of a silicon wafer, and it is suitable for the integration but not for obtaining high power ratings as the length between the source region and the drain region must be far away from each other to obtain better voltage blocking capability, and as the drain-to-source current is inversely proportional to the length.

2) Vertical Channel Structure

The drain and the source are placed in the opposite side of the wafer, and it is suitable for a power device as more space could be used as source region, and as the length between the source region and the drain region is reduced, it is possible to increase the drain-to-source current rating, and it could also increase voltage blocking capability by growing the epitaxial layer (drain drift region).

1. The VMOSFET Structure

   As shown in Fig. 4 (a), this structure has V-groove at the gate region and it is the first commercialized structure. But as there was stability problem in manufacturing, and the high electric field at the tip of V-groove, this VMOSFET structure was pushed out by the DMOSFET structure.

2. The DMOSFET Structure

   As shown in Fig. 4 (b), it has double-diffusion structure having P-base region and N^+ source region, and it is the most commercially successful structure.

3. The UMOSFET Structure

As shown in Fig 4 (c), this structure has U-groove at the gate region. This structure has higher channel density so that it can reduce on-resistance compared to the VMOSFET and the DMOSFET. UMOSFET structure using trench etching technique was commercialized in 1990s.

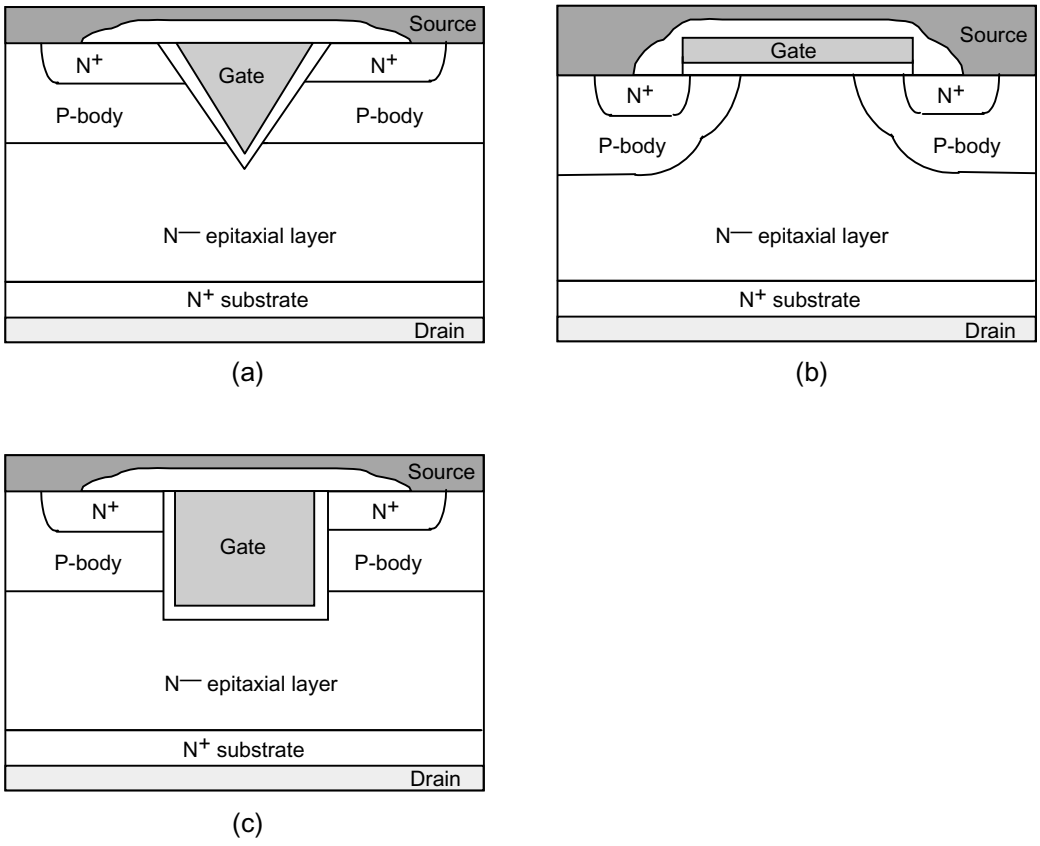


Fig. 4. Vertical Channel Structure

(a) The VMOSFET Structure
(b) The DMOSFET Structure
(c) The UMOSFET Structure

4. The characteristics of MOSFET

1) Advantages

1. High input impedance, Voltage controlled device, Easy to drive.

To maintain on-state, base drive current which is 1/5 or 1/10 of collector current is required, and larger reverse base drive current is needed for the high speed turn-off for the current controlled device, BJT. Due to these characteristics base drive circuit design becomes compli-

cated, and becomes expensive. On the other hand, voltage controlled device MOSFET is a switching device which is driven by channel at the semiconductor surface due to the field effect produced by the voltage applied to the gate electrode, which is isolated from the semiconductor surface. And as the required gate current during switching transient as well as on, off state is small, the drive circuit design is simple and the cost of it can be reduced.

2. Unipolar device, Majority carrier device, Fast switching speed.
   As there are no delay due to storage and recombination of minority carrier as in BJT, the switching speed is faster than the BJT in the orders of magnitude. So it has advantage in the high frequency operation circuit where the switching power loss is dominant.

3. Wide SOA (safe operating area).
   It has a wider SOA than BJT as it is applicable in short period of time with high voltage and high current without any destructive device failure due to second breakdown.

4. Forward voltage drop with positive temperature coefficient, Easy to use in parallel.
   When the temperature increases, the forward voltage drop also increases, and because of this, the current flows equally through each device when the devices are in parallel. So, the MOSFET is more easy to use in parallel than the BJT which has forward voltage drop with negative temperature coefficient.

2) Disadvantage

In high breakdown voltage devices over 200V, the conduction loss of MOSFET is larger than that of BJT that has the same voltage and current rating due to the on-state voltage drop.

3) Basic characteristics

1. Vertically oriented four-layer structure (n^+ p n^- n^+)

2. Parasitic BJT exists between the source and the drain.
   P-type body region becomes base, n^+ source region becomes emitter, and n-type drain region becomes collector (Refer to Fig.5). The breakdown voltage decreases from BV_{CBO} to BV_{CEO}, which is 50 ~ 60 [%] of BV_{CBO} when the parasitic BJT is turned on. At this state, if the drain voltage larger BV_{CEO} is supplied, the device fall into the avalanche breakdown state, and if the drain current cannot be limited externally, it will be destroyed by the second breakdown. So n^+ source region and p-type body region must be shorted by metallization in order to prevent the parasitic BJT turn-on. But if the V_{DS} increase rate is large in high – speed turn – off state, there will be a voltage drop between the base and the emitter, and cause the BJT turn – on. This could be prevented by increasing the doping density of p - body region, which is at the bottom of n^+ source region, and by lowering the speed of MOSFET switching by designing the circuit so that the gate resistance could be large. Due to the source region being short, another parasitic component, diode, is formed up, and this is used in half-bridge and full-bridge converter usefully.

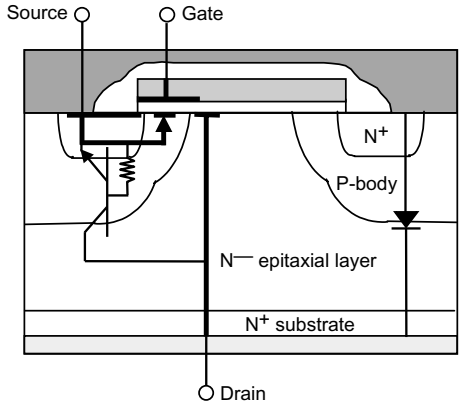


Fig. 5. The MOSFET vertical structure showing the parasitic BJT and diode

3. Output characteristics

i_D characteristics due to V_{DS} in many V_{GS} conditions. (Refer to Fig. 6)

→ It could be divided as the ohmic region, the saturation (=active) region, and the cut-off region.

- Ohmic region: Constant resistance region. If drain-to-source voltage is zero, the drain current also becomes zero regardless of gate–to-source voltage. This region is at the left side of $V_{GS} - V_{GS(th)} = V_{DS}$ boundary line ($V_{GS} - V_{GS(th)} > V_{DS} > 0$), and in this region, even if the drain current is very large, the power dissipation could be maintained by minimizing the $V_{DS(on)}$.
- Saturation region: Constant current region. It is at the right side of $V_{GS} - V_{GS(th)} = V_{DS}$ boundary line, and in this region, the drain current differs by the gate–to-source voltage, not by the drain-to-source voltage. Here, the drain current is called saturated.
- Cut-off region: It is called cut-off region, when the gate-to-source voltage is lower than $V_{GS(th)}$ (threshold voltage).

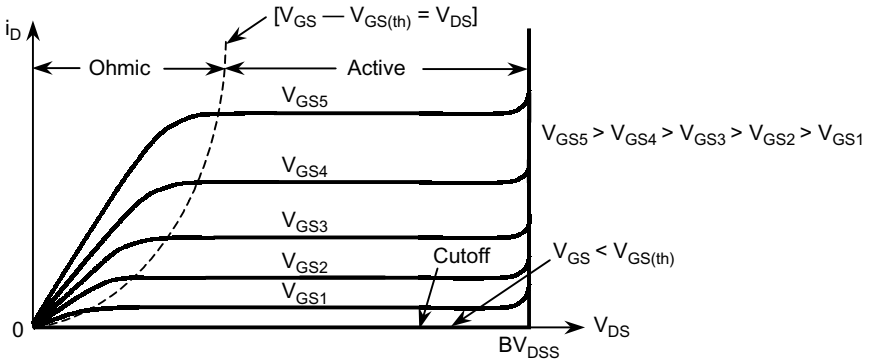


Fig. 6. Output Characteristics

Rev C, November 1999

4. Transfer characteristics

i_D characteristics due to V_{GS} in the active region. (Refer to Fig. 7)

- i_D equation due to V_{GS}

$$i_D = K(V_{GS} - V_{GS(th)})^2$$

$$K = \mu_n C_{OX} \frac{W}{2L}$$

where μ_n: carrier mobility

C_{OX}: gate oxide capacitance per unit area

$C_{OX} = \varepsilon_{OX}/t_{OX}$

ε_{OX}: dielectric constant of the silicon dioxide

t_{OX}: thickness of the gate oxide

W : channel width

L : channel length

In logic-level device, it shows parabolic transfer curve according to above equation, but the power MOSFET follows the above equation, only in low i_D in transfer curve, and other areas show linearity. It is because the mobility of the carrier is not constant but decreases due to increase of the electric field along with the increase of i_D at the inverse layer.

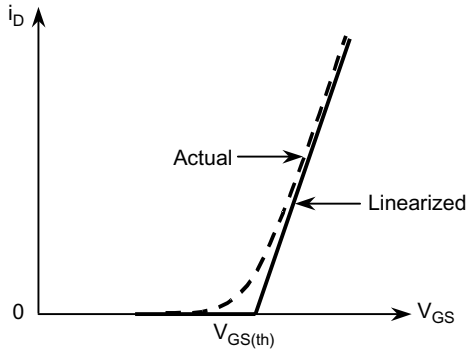


Fig. 7. Transfer Curve

5. Characteristics of MOSFET's ON, OFF.

1) Off state

(1) BV_{DSS}: It is the maximum drain-to-source voltage where the gate and the source are shorted, in other words, in off state, the MOSFET can endure without avalanche breakdown of the body-drain pn junction. The measurement conditions are V_{GS} = 0 [V], I_D = 250 [μA], and the drift region's (N^- epitaxy) length is determined by the BV_{DSS}. Avalanche breakdown, reach-through breakdown, punch-through breakdown, zener breakdown, and dielectric breakdown are the 5 factors, which drives the breakdown. And the following describes about 3 of the factors.

1. Avalanche breakdown

   It is the mobile carriers' sudden avalanche caused by increasing electric field in the depletion region of body-drain pn junction up to a critical value. And it is the most dominant factor among other factors that drives the breakdown.

2. Reach-through breakdown

   It is the special case of avalanche breakdown occurring when the depletion region of the N^- epitaxy contacts the N^+ substrate.

3. Punch-through breakdown

   This is the avalanche breakdown occurring when the depletion region of the body-drain junction contacts the N^+ source region.

(2) I_{DSS}: It is the drain-to-source leakage current when it is in off state where the gate is being shorted with the source. The amount of increase for I_{DSS}, which is sensitive to temperature, is large with the temperature increase, while the amount of increase for BV_{DSS} is very little.

2) Turn-on transient

The process of the channel formation

1. The formation of the depletion region:

   When the small positive gate – to – source voltage is supplied to the gate electrode (Refer to Fig. 8 (a))

   * Positive charge induced in the gate electrode, induct the same amount of negative charge at the oxide – silicon interface (P^--body region, which is underneath the gate oxide), and here the holes are pushed into the semiconductor bulk by the electric field, and the depletion region is formed up by the acceptors charged with negative.

2 The formation of the inversion layer:
As the positive gate – to – source voltage increases (Refer to Fig. 8 (b), (c))

The depletion region gets wider towards the body, and it begins to drag the free electrons to the interface. This free electrons have been created by the thermal ionization. And the free holes created with the free electrons, are pushed into the semiconductor bulk. The holes that haven't been pushed into the bulk are neutralized by the electrons that have been dragged by the positive charges of the holes from the n^+ source. If the supplied voltage keeps increasing, the density of the free holes of the body and the density of the free electrons of the interface becomes equal. At this point, the free electron layer is called inversion layer. And this inversion layer enables the current flow as it becomes the conductive pass(=channel) of the drain and the source of the MOSFET.

Threshold voltage : The gate-to-source voltage which forms up the inverse layer is called $V_{GS(th)}$ (=threshold voltage).

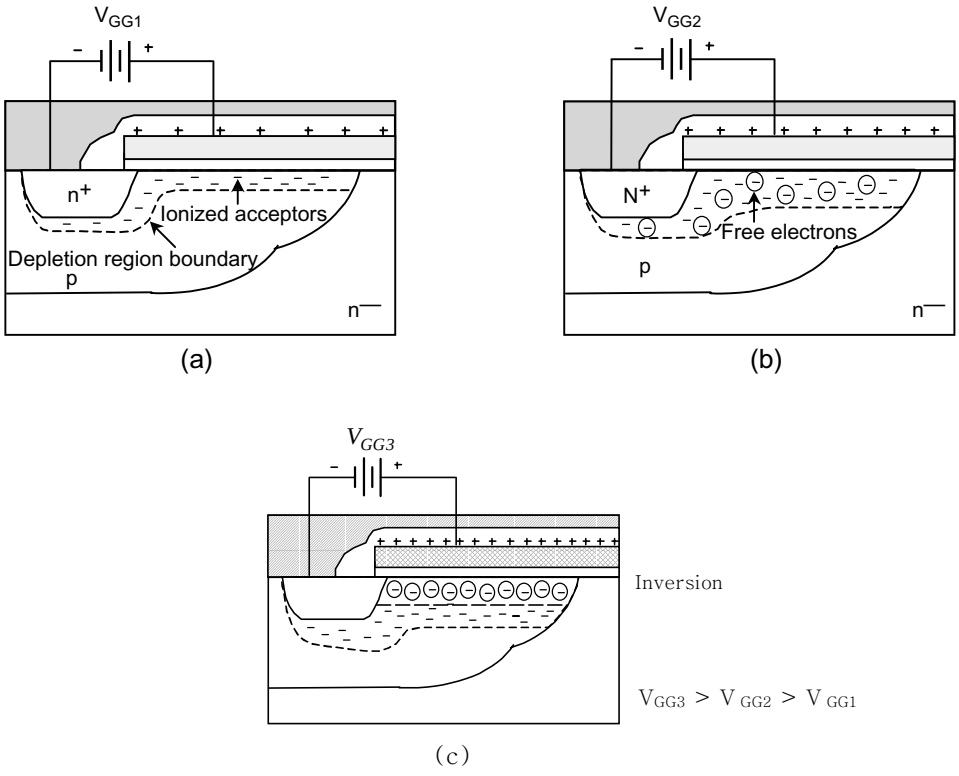


Fig. 8. The process of channel formation
(a) Formation of the depletion region
(b), (c) Formation of the inversion layer

3) On state

Drain current (I_D) changes due to the drain-to-source voltage (V_{DD}) increase. (V_{GS} is constant) In the MOSFET, when the channel has formed up and the V_{DD} is supplied, I_D starts to flow. When the V_{GS} is a constant value, and the V_{DD} is increased, the I_D also increases linearly, But shown in the graph of the MOSFET output characteristics, when the real V_{DD} goes over certain level, the increase rate of I_D decreases slowly. And eventually, it becomes a constant value independent of V_{DD}, and becomes dependent of V_{GS}.

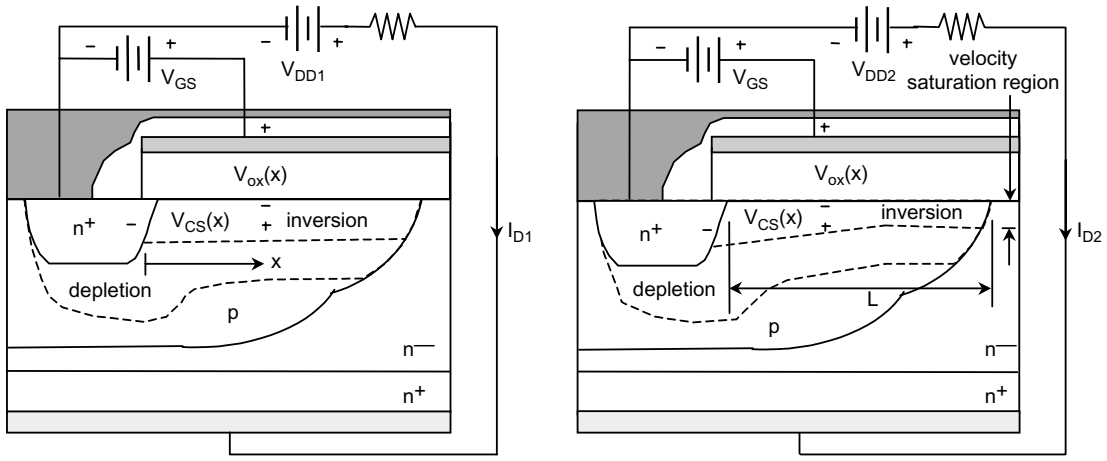


Fig. 9. Inversion layer thickness changes due to the increase of the drain-to-source voltage (V_{DD}). Where, $V_{DD1} < V_{GS} - V_{GS(th)}$, $V_{DD2} > V_{GS} - V_{GS(th)}$, I_{D2} (saturation current) > I_{D1}

(a) spatially uniform
(b) spatially nonuniform

To understand the characteristics, as shown in Fig. 9, we must pay attention to the voltage drop at the $V_{CS}(x)$ due to the ohmic resistance when there are I_D flowing at the inverse layer. ($V_{CS}(x)$ is the channel-to-source voltage from the source at the distance of x). This voltage is equal to the V_{GS}–$V_{ox}(x)$ at each x points ($V_{ox}(x)$ is the gate-to-body voltage crossing the gate oxide from the source at the distance of x), and it has the maximum value, V_{DS} at x=L (the drain end of the channel). As shown in Fig. 9 (a), when the low voltage $V_{DD}=V_{DD1}$ is supplied, low $I_D(=I_{D1})$, which has almost no voltage drop of $V_{CS}(x)$, flows. So as the $V_{ox}(0)$~$V_{ox}(L)$ is constant, the thickness of the inversion layer remains in uniform. And as higher V_{DD} is supplied, I_D increases, and the voltage drop of $V_{CS}(x)$ occurs, and the value of $V_{ox}(x)$ decreases, and these reduces the thickness of the inversion layer starting from x=L. And because of this, the resistance increases, and the graph of I_D starts to become flat, where it use to increase with the increment of the V_{DD}. When $V_{ox}(L)=V_{GS}$–$V_{DS}=V_{GS(th)}$, as I_D increases, the inversion layer at x=L doesn't disappear due to the high electric field ($J=\sigma E$) formed by the reduction of thickness, and maintains the minimum thickness. The high electric field not only maintains the minimum thickness of the inversion layer, it saturates the velocity of the charge carrier at $V_{ox}(L)=V_{GS}$–$V_{DS}=V_{GS(th)}$.

The velocity of the charge carrier initially increases with the increase of the electric field, and at certain point, it becomes saturated. In silicon, when the electric field becomes $1.5x10^4$ [V/cm], it starts the saturation when the drift velocity of the electron is $8x10^6$ [cm/s]. From this point, the device goes into the active region, and when higher V_{DD} is supplied, as shown in Fig. 9 (b) the electric field at x=L increases more, and the channel region which maintained the minimum thickness expands towards the source. V_{DS} becomes $V_{DS}>V_{GS}-V_{GS(th)}$ due to the increase of the V_{DD}, and the I_D is kept constant.

4) Turn-off transient

The reverse process of the turn-on transient is turn-off transient.

6. User's Manual

1) Characteristics of Capacitance

The following are the 3 kinds of parasitic capacitance described in the data book.

- Input capacitance $C_{iss} = C_{gd} + C_{gs}$
- Output capacitance $C_{oss} = C_{gd} + C_{ds}$
- Reverse transfer capacitance $C_{rss} = C_{gd}$

The following figure shows the parasitic capacitance described above.

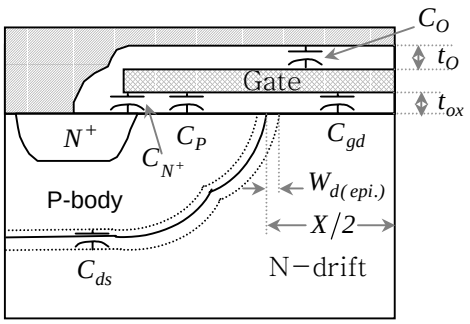


Fig. 10. The vertical structure showing parasitic capacitance

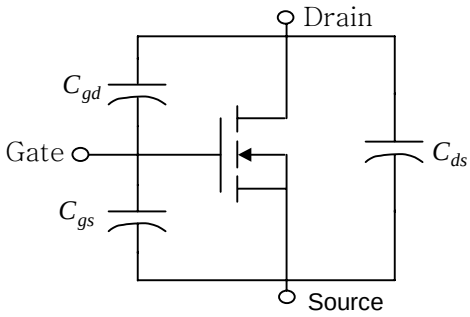


Fig. 11. Equivalent circuit showing parasitic capacitance

(1) C_{gs}: The capacitance between the gate and the source

$$C_{gs} = C_O + C_{N^+} + C_P$$

1. C_O: The capacitance between the gate and source metal

$$C_O = \frac{\varepsilon_I A_O}{t_O}$$

where ε_I: the dielectric constant of the intervening insulator

t_O: the thickness of the intervening insulator

A_O: the area of the overlap between the source and gate electrode

2. C_{N^+}: The capacitance between the gate and n^+ source diffusion region

$$C_{N^+} = \frac{\varepsilon_{ox} A_{N^+O}}{t_{ox}} = C_{ox} A_{N^+O}$$

where ε_{ox}: the dielectric constant of the gate oxide

t_{ox}: the gate oxide thickness

C_{ox}: gate-oxide capacitance per unit area

A_{N^+O}: the area of overlap of the gate electrode over the N^+ emitter

3. C_P: The capacitance between the gate and p-body. It is affected by the gate and the drain voltage and the channel length. The C_P is the only component that is influenced by the change of the drain voltage (V_{DS}) among other C_{gs} components, and when V_{DS} increases, the depletion region expands to the p-body, and decreases the value of C_P. But even if the V_{DS} increases up to the breakdown voltage, there are almost no changes to the value of C_P, as the depletion region doesn't exceed 10% of the p-body. So, the change of C_{gs} due to V_{DS} is very small.

(2) C_{gd}: The capacitance between the gate and the drain.

It is influenced by the voltage of the gate and the drain. When there are V_{DS} variations, the area under C_{gd} (n^--drift region meeting with the gate oxide) is changed, and the value of the capacitance is affected. And as we can see in the following equation, when $V_{DS} >> \phi_B$, the capacitance decreases as V_{DS} increases with the relation of $C_{gd} \propto (1 - k\sqrt{V_{DS}})$.

$$C_{gd(\text{per unit area})} = C_{ox}\left(1 - \frac{2W_{d(epi.)}}{X}\right)$$

where X : the length between the adjoined cells

$W_{d(epi.)}$: the width of the depletion region in the epitaxial layer(= N- drift region)

$$W_{d(epi.)} = \sqrt{\frac{2k_s\varepsilon_o(V_{DS} + \phi_B)}{qC_B}}$$

As C_{gd} increase ($1+g_{fs}R_L$(load resistance)) times due to the Miller effect, it prominently decreases the frequency characteristics.

Frequency response of the power MOSFET

As the frequency response of the power MOSFET is limited by the charging and discharging of the input capacitance, if the C_{gs} and C_{gd}, which determines the input capacitance become smaller, it is possible to work in high frequency. As the input capacitance is unrelated to the temperature, MOSFET's switching speed is also unrelated to the temperature.

(3) C_{ds}: The capacitance between the drain and the source.

The capacitance varies due to the variation of the C_{ds}'s thickness, which is the junction thickness of the p-body and the n^-- drift region, with the change of V_{DS}.

$$C_{ds(\text{per unit area})} = \sqrt{\frac{q k_s \varepsilon_o C_B}{2(V_{DS} + \phi_B)}}$$

where q : elementary electronic charge (1.9×10^{-19} [C])

k_s: silicon dielectric constant

ε_o: the permeability of free space (8.86×10^{-14} [F/cm])

C_B: epitaxial layer background concentration [atoms/cm^3]

V_{DS}: drain-to-source voltage

ϕ_B: diode potential

As shown in the equation above, when $V_{DS} >> \phi_B$, C_{ds} decreases as V_{DS} increases with the relation of $C_{gd} \propto (1/\sqrt{V_{DS}})$.

2) Characteristics of the gate charge

It is the amount of charge that is required during the MOSFET's turn-on or turn-off transient.

In the data book, following types of charges are stated.

Total Gate Charge …… Q_g (The amount of charge during $t_0 \sim t_4$)

Gate-Source Charge …… Q_{gs} (The amount of charge during $t_0 \sim t_2$)

Gate-Drain (" Miller ") Charge ….. Q_{gd} (The amount of charge during $t_2 \sim t_3$)

The following figure shows the gate-source voltage, gate-source current, drain-source voltage, and drain-source current during the turn-on, and divided them into 4 sections to show the equivalent circuits at the diode-clamped inductive load circuit.

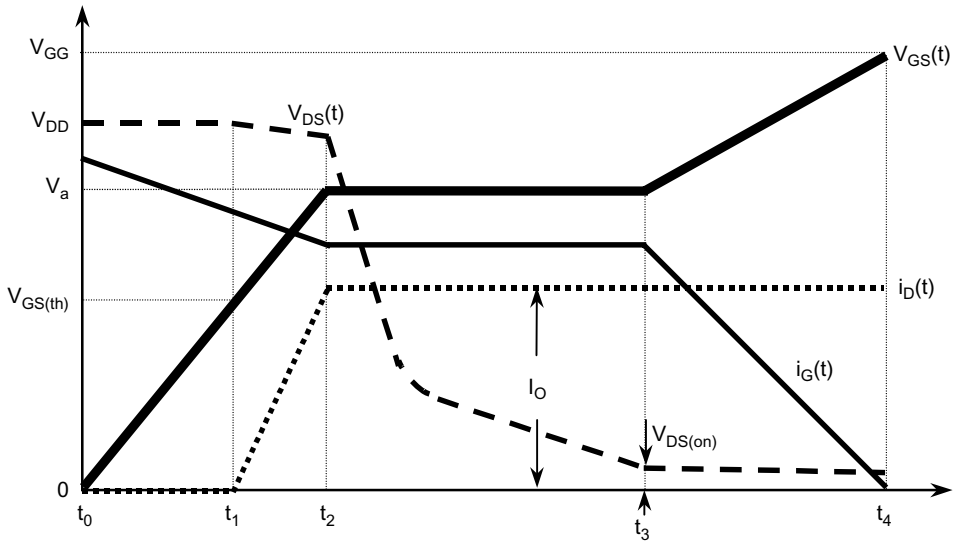


Fig. 12. The graph of $V_{GS}(t)$, $i_G(t)$, $V_{DS}(t)$, $i_D(t)$ when turn on

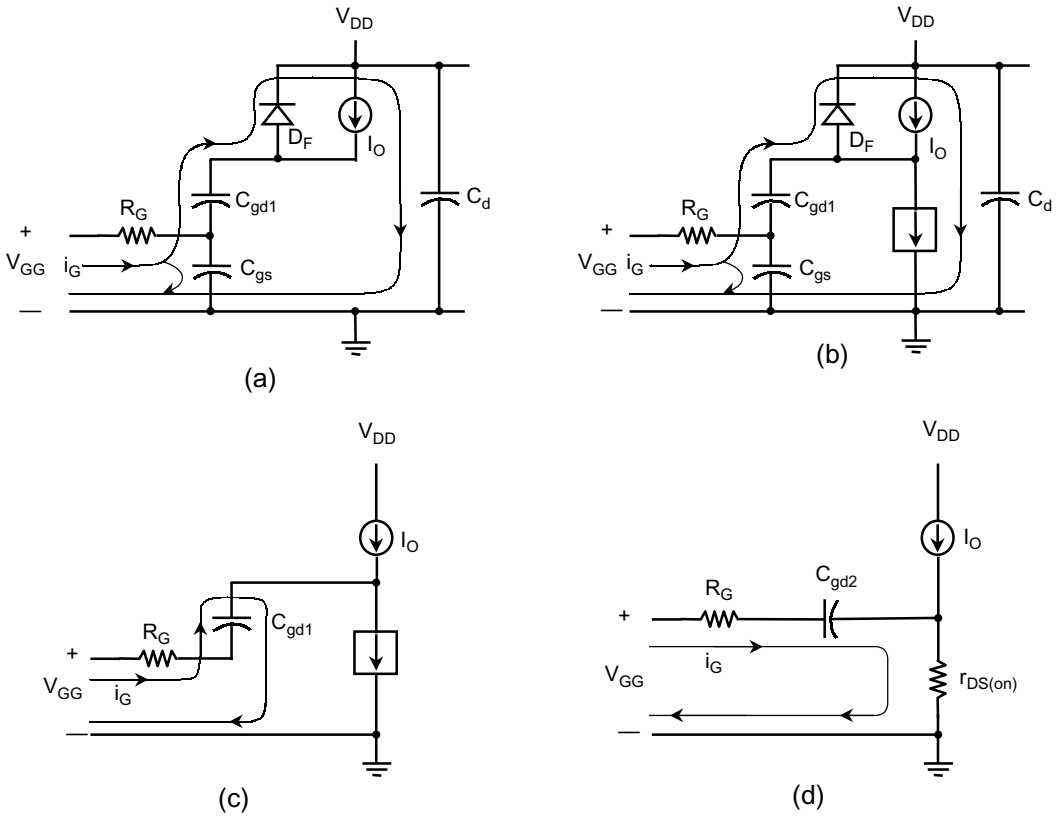


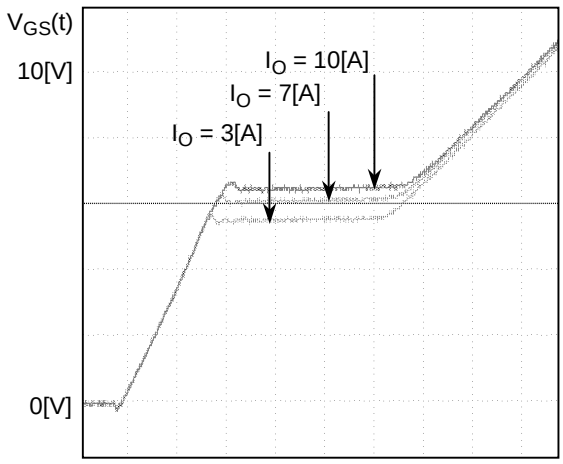
Fig. 13. Equivalent circuits of the MOSFET turn – on
divided into 4 periods at diode – clamped inductive load circuit.

(a) equivalent circuit of period $t_0 \sim t_1$
(b) equivalent circuit of period $t_1 \sim t_2$
(c), (d) equivalent circuit of period $t_2 \sim t_3$
(d) equivalent circuit of period t_3

1. $t_0 \sim t_1$: As i_G charges C_{gs} and C_{gd}, V_{GS} increases from 0[V] up to $V_{GS(th)}$. The graph of increasing $V_{GS}(t)$ looks to be linearly increasing, but it is in fact an exponential curve having a time constant of $\tau_1 = R_G(C_{gs} + C_{gd1})$. As shown in Fig. 13 (a), V_{DS} is still equal to V_{DD}, and i_D is zero. The MOSFET is still in the state where it hasn't been turned on.

2. $t_1 \sim t_2$: V_{GS} increases exponentially passing $V_{GS(th)}$, and as V_{GS} continues to increase, i_D begins to increase and reaches to the full load current (I_O). So (V_a) varies to I_O condition in t_2. When i_D is smaller than I_O, and when it is in the state where the D_F is being conducted, V_{DS} maintains the V_{DD}, but the real graph shows the voltage which is little less than V_{DD}. This is caused by the voltage drop due to the inductance existing in the line of the circuit.

Following graph shows the $V_{GS}(t)$ measuring the V_a variation in accordance with i_D conditions in turn-on state.



Device : FQP10N20

Test Condition : V_{DS} = 160[V]
V_{GS} = 10[V]

Division : $V_{GS}(t)$: 2[V]/div
t : 1[μsec]/div

3. $t_2 \sim t_3$: V_{GS} is a constant value in accordance with the transfer characteristics as it is in an active region where i_D is the full load current (I_O). So, i_G can only flow through C_{gd}, and can be obtained by the following equation.

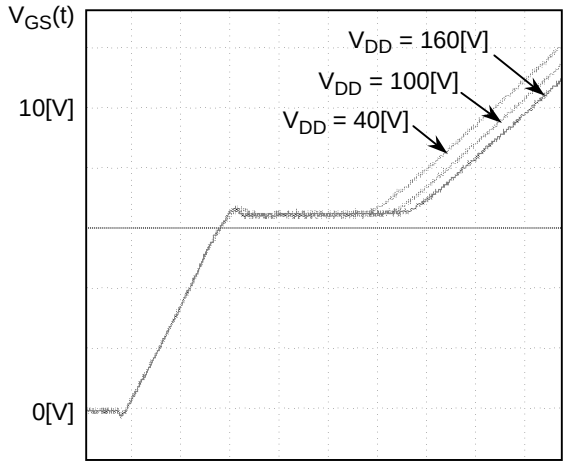
$$i_G = \frac{V_{GG} - V_a}{R_G}$$

So, the V_{DS} can be configured as the following ratios.

$$\frac{dv_{DG}}{dt} = \frac{dv_{DS}}{dt} = \frac{i_G}{C_{gd}} = \frac{V_{GG} - V_a}{R_G C_{gd}}$$

This is the region where the MOSFET is still operating in the active region, and as the V_{DS} decreases, it gets closer to the ohmic region. When V_{DD} increases, $t_2 \sim t_3$ (flat region of V_{GS}) also increases.

Following figure is the graph of $V_{GS}(t)$ showing the variation of $t_2 \sim t_3$ (flat region of V_{GS}) in accordance with the V_{DD} condition.



Device : FQP10N20

Test Condition : I_O = 10[A]
V_{GS} = 10[V]

Division : $V_{GS}(t)$: 2[V]/div
t : 1[μsec]/div

At t_3, V_{DS} becomes $V_{DS(on)}=I_O \bullet r_{DS(on)}$, and the transient is completed. And the MOSFET is placed at the boundary of getting into the ohmic region from the active region.

4. $t_3 \sim t_4$: It is the period where it operates in an ohmic region. The V_{GS} increases up to V_{GG} with the time constant of $\tau_2 = R_G(C_{gs} + C_{gd2})$

3)Drain-source on resistance ($R_{DS(on)}$)

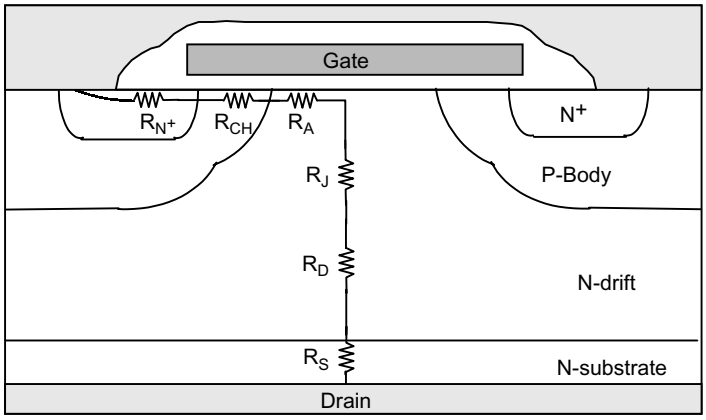


Fig. 14. The vertical structure of MOSFET showing internal resistance

$R_{DS(on)}$ in MOSFET is the total resistance between the source and the drain during an on state, and it is an important parameter determining maximum current rating and the loss. To reduce $R_{DS(on)}$, enhancing the integrity of the chip and using trench technique are used. This can be stated as a following equation.

$$R_{DS(on)} = R_{N^+} + R_{CH} + R_A + R_j + R_D + R_S$$

where R_{N^+}: It is the resistance of the source region with N^+ diffusion, and it only takes very little portion of resistance compare to other components that forms up the $R_{DS(on)}$. And it can be ignored in high voltage power MOSFET.

R_{CH}: It is the resistance of the channel region where it is the most dominant factor of $R_{DS(on)}$ in low voltage MOSFET. This resistance can be varied by the ratio of the channel's width to the length, the thickness of the gate oxide, and the gate drive voltage.

R_A: As the gate drive voltage is supplied, charges start to accumulate in N^- epi. Surface (the plate under C_{gd}), and forms up a current path between the channel and the JFET region. And the resistance of this accumulation region is R_A. The resistance varies by the charge in the accumulation layer, and the mobility for the free carriers at the surface. And if the gate electrode is reduced, its effect is same as reducing the length of the accumulation layer, so the value of R_A is reduced while R_J increases.

R_J: N^- epi. region between the P-bodies is called JFET region as the P-body region acts like the gate region of JFET. And the resistance of this region is R_J.

R_D: The resistance occurring from right below the P-body to the top of the substrate is called R_D, and it is the most dominant factor in high voltage MOSFETs

R_S: This is the resistance of the substrate region, and this factor can be ignored in high voltage MOSFETs. But in low voltage MOSFETs where the breakdown voltage is below 50[V], it becomes a factor which can have large effect on the $R_{DS(on)}$.

Additional resistances can arise from a non-ideal contact between the source/drain metal and the N^+ semiconductor regions as well as from the leads used to connect the device to the package.

$R_{DS(on)}$ increases with the temperature. (positive temperature coefficient)
The reason is because the mobility of the hole and electron decreases as the temperature rises, and the $R_{DS(on)}$ in accordance with the temperature of p / n- channel power MOSFET can be estimated with the following equation.

$$R_{DS(on)}(T) = R_{DS(on)}(25°C)\left(\frac{T}{300}\right)^{2.3}$$

where T : absolute temperature

This is an important characteristics in the view of device stability and paralleling. So as to say that it doesn't need any external circuit's assistance to show good current sharing when $R_{DS(on)}$ increases with the temperature and it is connected in parallel.

4) Threshold voltage ($V_{GS(th)}$)

It is the minimum gate bias which enables the channel to be formed between the source and the drain. The drain current increases in proportion to $(V_{GS}–V_{GS(th)})^2$ in the saturation region.

1. High $V_{GS(th)}$
   As high gate bias voltage is needed to turn-on the power MOSFET, it becomes difficult to design a gate drive circuitry.

2. Low $V_{GS(th)}$
   When $V_{GS(th)}$ of the n-channel power MOSFET becomes negative due to the existence of the charges in gate oxide, it shows the characteristic of normally-on where conductive channel exists even in zero gate bias voltage. Even if the $V_{GS(th)}$ is positive, and the value is very small, there could be a turn-on either by the noise signal of the gate terminal or by increasing gate voltage during high speed switching.

   The $V_{GS(th)}$ can be controlled by the gate oxide thickness. And normally the gate oxide is made thick in high voltage device so that the $V_{GS(th)}$ is set as 2~4[V], and the gate oxide is made thin in low voltage device (logic level) so that $V_{GS(th)}$ can be 1 ~ 2 [V]. $V_{GS(th)}$ can also be controlled not only by the gate oxide thickness but also by the back ground doping (The density of P-body for the n-channel power MOSFET). And it increase in proportional to a square root of the background doping.

   Temperature characteristic

   $V_{GS(th)}$ decreases as the temperature increases, and the decrease rate can be varied due to the gate oxide thickness and background doping level. In other words, the decrease rate increase when the gate oxide becomes thicker and the background doping level increases.

5) Transconductance (g_{fs})

It is the gain of the MOSFET. It can be expressed as the following equation meaning the amount of change in drain current by the amount of change in the gate-source bias voltage.

$$g_{fs} = \left[\frac{\Delta I_{DS}}{\Delta V_{GS}}\right]_{V_{DS}}$$

In measurement, V_{DS} should be set so that the device could be activated in the saturation region, and V_{GS} should be supplied so that the I_{DS} becomes 1/2 of the maximum current rating. g_{fs} varies by the channel width/length, and by the gate oxide thickness. And as shown in Fig. 15, after $V_{GS(th)}$, g_{fs} increases dramatically with the increase of the drain current and it becomes a constant after the drain current reaches at a certain point (at higher values of drain current). If g_{fs} is large enough, high current handling capability could be gained from the low gate drive voltage and the high frequency response is possible.

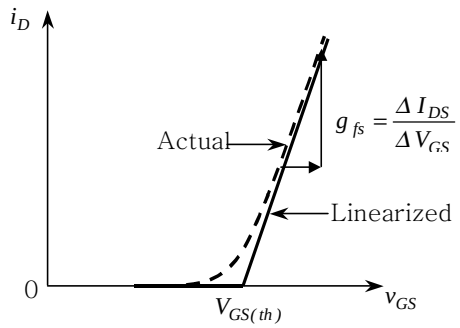


Fig. 15. Transfer Curve & g_{fs}

Temperature characteristic

g_{fs} decreases as the temperature increases due to the reduction of the mobility. From the following equation similar to the $R_{DS(on)}$ and the temperature relation, it is possible to know the g_{fs} changes by the temperature.

$$g_{fs}(T) = g_{fs}(25°C)\left(\frac{T}{300}\right)^{-2.3}$$

where T : absolute temperature

6) Drain-Source Breakdown Voltage (BV_{DSS}), Breakdown Voltage Temp. Coeff. ($\Delta BV/\Delta T_J$)

BV_{DSS} is the maximum drain-to-source voltage where the gate and the source are shorted, in other words, in off state, the MOSFET can endure without avalanche breakdown of the body-drain pn junction. The measurement conditions are V_{GS}=0[V],I_D=250[μA], and the length of the drift region (N^- epitaxy) is determined by the BV_{DSS}. Avalanche breakdown, reach-through breakdown, punch-through breakdown, zener breakdown, and dielectric breakdown are the 5 factors, which drives the breakdown.

Temperature characteristic

As junction temperature increases, it also increases linearly, and whenever it goes up 100 [°C], 10[%] of BV_{DSS} at 25 [°C] increase (Refer to the breakdown voltage temp. coefficient ($\Delta BV/\Delta T_J$) and Fig. 7. breakdown voltage vs. temperature in the data book.)

7) Drain-to-Source Leakage Current (I_{DSS})

It can be measured by providing the maximum drain-to-source voltage and 80 [%] of the voltage (T_C=125[°C]) in off state where the gate is shorted to the source. I_{DSS} is more sensitive to the temperature than BV_{DSS}, and it has positive temperature coefficient.

8) Gate – to – Source Voltage (V_{GS})

It means the maximum operating gate – to – source voltage, and the negative voltage handling capability enables the enhancement of the turn – off speed by providing reverse bias to the gate and the source.

9) Gate – Source Leakage, Forward / Reverse (I_{GSS})

It can be measured by providing the maximum operating gate – to – source voltage (V_{GS}) between the gate and the source. Forward / reverse is decided in accordance with the polarity of the V_{GS}. I_{GSS} is dependent on the quality of gate oxide and device size.

10) Switching characteristics ($t_{d(on)}$, t_r, $t_{d(off)}$, t_f)

The power MOSFETs have good switching characteristics as there are no storage time caused by minority carrier, and no variation caused by the temperature. Following figure shows the switching sequence divided into few parts.

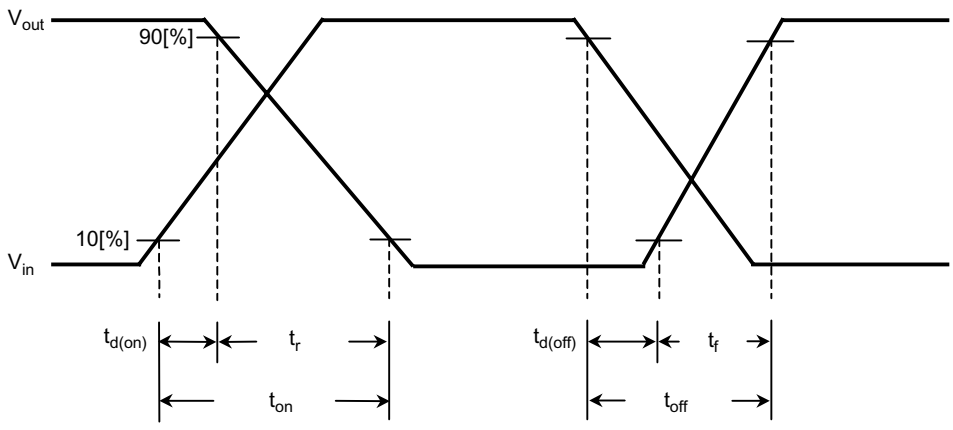


Fig. 16. Resistive switching waveforms

$t_{d(on)}$(turn-on delay time): This is the time for the gate voltage V_{GS} to reach up to the threshold voltage $V_{GS(th)}$, and the input capacitance during this period is C_{gs}+C_{gd}, and this also means that this time is the charging time to bring up the capacitance to the threshold voltage.

t_r (rise time): It is the time after the V_{GS} reaches the $V_{GS(th)}$ to complete the transient. It can be divided into 2 regions. One is the time where the drain current starts from zero(increasing with the gate voltage in accordance with the transfer characteristics) and reaching up to the load current, and another region is when the drain voltage starts to drop and reaching up to on-state voltage drop. As shown in the gate charge characteristics graph, the V_{GS} maintains in as a constant value as the drain current is constant in this region, where the voltage decreases. During the rise time, as both the high voltage and the high current exists in the device, high power dissipation occurs. So the rise time should be reduced by reducing the gate series resistance and the drain-gate capacitance (C_{gd}). After this, the gate voltage continues to increase up to the supplied voltage level. But, as the drain voltage and the current are already in steady–state, they are not affected during this region.

$t_{d(off)}$(turn-off delay time): The gate voltage operates in the supplied voltage level during the on state, and when the turn-off transient starts, it starts to decrease. The $t_{d(off)}$ is the time for the gate voltage to reach up to the point where it is required to make the drain current become saturated at the value of load current. And during this time, there are no changes to the drain voltage and the current.

t_f (fall time): It is the time where the gate voltage reaches the threshold voltage after $t_{d(off)}$. And it can be divided into the region where the drain voltage reaches the supply voltage from on-state voltage, and the region where the drain current reaches zero from the load current. As there are a lot of power dissipation in t_r region during turn-on state, the power dissipation occurs in the t_f region during turn-off state, so the t_f must be reduced as much as possible. After this, the gate voltage continues to decrease until it reaches zero. But, as the drain voltage and the current are already in steady – state, they are not affected during this region.

11) Single – Pulsed Avalanche Energy; Unclamped Inductive Switching (E_{AS})

(1) Power MOSFET Turn-off (In inductive load circuit)

While in on-state (supplying positive voltage exceeding the threshold voltage in n-channel device), the electrons flows into the drain from the source through inversion layer (=channel) of the body surface, and forms up a current flow from the drain to the source, if it is an inductive load, this current will increase linearly. To turn-off the MOSFET, the gate voltage can be removed or supply a reverse voltage so that it could eliminate the inversion layer of the body surface. Once the charges at the inversion layer starts to be removed and the channel current (drain current) starts to be reduced, the inductive load increases the drain voltage so that it could maintain the drain current. And when the drain voltage increases, the drain current is divided into the channel current and the

displacement current. The displacement current is the current made as the depletion region is developed at the drain-body diode, and it is proportional to dv_{DS}/dt (The ratio of drain voltage rise by the time). The dv_{DS}/dt is limited by how fast the gate can be discharged and by how fast the drain-body depletion region can be charged. Specially, the charge of the drain-body depletion region is determined by the C_{ds} and the magnitude of the drain current. When the drain voltage increases, and cannot be clamped by external circuit, (UIS) drain-body diode starts to build the current carriers through the avalanche multiplication, and the device falls into the sustaining mode. While in the sustaining mode, all the drain current (avalanche current) goes through the drain-body diode, and can be controlled by the (channel current equals to zero) inductor load. If the current (leakage current, displacement current (dv_{DS}/dt current), avalanche current) flowing at the body region underneath the source is large enough, the parasitic bipolar transistor becomes active, there can be a device failure.

Fig. 17 shows the drain voltage and the current when single pulse (width: t_P) is supplied at the unclamped inductive load circuit.

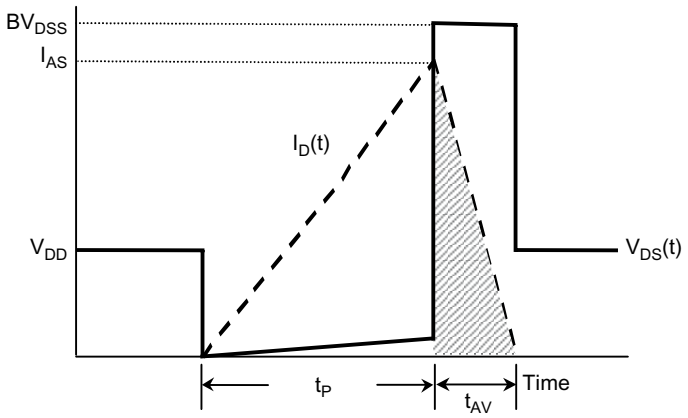


Fig. 17. Unclamped inductive switching waveforms.

$I_D(t)$ can be changed by the inductor load size, supply voltage (V_{DD}) and the gate pulse width (t_P). The shaded area of avalanche region (t_{AV}) shows the dissipation energy (E_{AS}). E_{AS} and t_{AV} can be obtained with the following equation.

$$E_{AS} = \frac{1}{2} L_L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

$$t_{AV} = \frac{L_L I_{AS}}{BV_{DSS}}$$

(2) Power MOSFET failure has following characteristics during the inductive turn-off.

1. It has same electrical characteristics as the second breakdown of the bipolar transistor.

2. Independent from dv_{DS}/dt.
   While maintaining the gate turn-off voltage constantly, and changes the magnitude of the external gate resistance, the magnitude of the gate turn-off current changes, and because of this, the dV_{DS}/dt changes. If dV_{DS}/dt current makes the device failure, the voltage that can lead the second breakdown should be decreased with the increase of dV_{DS}/dt. But when measuring the second breakdown voltage while changing the external gate resistance (changing dV_{DS}/dt), the highest voltage could be measured at the highest dV_{DS}/dt. ("TURN-OFF FAILURE OF POWER MOSFETS", David L. Blackburn)

3. The voltage where the failure occurs increases with the temperature.

4. Critical current reduces as temperature increases.
   Critical current represents the maximum value of the drain current that can safely turn-off the device in unclamped mode, and at the current exceeding this, the second breakdown occurs.

5. It has nothing to do with the magnitude of the load inductance.
   →Due to the avalanche current from the drain-body diode, the parasitic bipolar transistor is activated, and because of this, the MOSFET failure begins.

12) Repetitive Avalanche Rating (E_{AR}, I_{AR})

E_{AR}: It represents avalanche energy for each pulse under repetitive condition.

I_{AR}: It represents the maximum avalanche current, and it is same as I_D rating of the device.

13) Drain-to-Source dv/dt Ratings

When high dv/dt is supplied at the drain, there is a possibility of current conduction in the power MOSFET, and in some cases, this can destroy the device. Following describes the some of dv/dt that causes the turn-on.

(1) Static dv/dt

1. False turn-on

2. Parasitic transistor turn-on

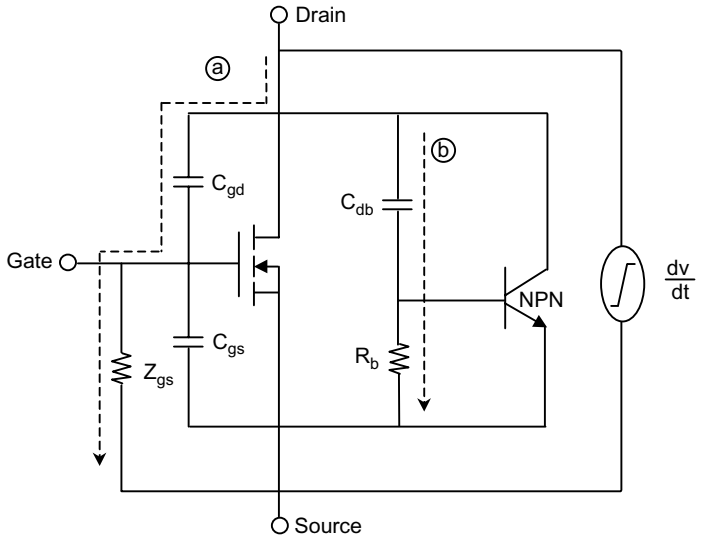


Fig. 18. Equivalent circuit of N-channel MOSFET

1. In off state, the sudden increase of the drain voltage changes the voltage across the parasitic capacitance, which is between the drain and the gate, and develops the displacement current (a) of C*dv/dt. And if the voltage exceeding $V_{GS(th)}$ develops between the gate and the source due to the displacement current and the gate-to-source impedance (Z_{gs}), the MOSFET does a false turn-on. Here the parasitic capacitance between the drain and the gate can be C_{gd} or can be larger than C_{gd} in accordance with the circuit layout. Z_{gs} is the impedance of the drive circuit, and it can be presented as a series of R, L, battery components. Due to the false turn-on, the device fall into the current conduction state, and in severe cases, high power dissipation develops in the device and brings the destructive failure. The following equation shows the voltage drop V_{GS} across Z_{gs}, and shows the dv/dt capability in this mode.

$$V_{GS} = Z_{gs} C_{gd} \left[\frac{dv}{dt}\right]$$

$$\left[\frac{dv}{dt}\right] = \frac{V_{GS(th)}}{Z_{gs} C_{gd}}$$

   To increase dv/dt capability, the gate drive circuit with very low impedance should be used, and increase the $V_{GS(th)}$. But in the drive circuit with the low impedance, the cost is expensive and increasing the $V_{GS(th)}$ is related to the increasing of $R_{DS(on)}$. And as the $V_{GS(th)}$ has the negative temperature coefficient, the possibility of false turn-on increases as the temperature rises. But typically, gate voltage doesn't go over the threshold voltage, and the high device resistance limits the device current, so the device destruction due to the false turn-on can hardly happen.

2. In off state, the sudden increase of the drain voltage, changes the voltage across C_{db}, and it develops the current (b) flowing through R_b. And when the voltage across the R_b goes over

V_{be} (emitter-base forward bias voltage where the parasitic bipolar transistor is turned on, approximately 0.7[V]), the parasitic bipolar transistor is turned on. When the parasitic bipolar transistor is turned on, the breakdown voltage of the device is reduced from BV_{CBO} to BV_{CEO} which is 50 ~ 60 [%] of BV_{CBO}. And if the drain voltage larger than BV_{CEO} is supplied, the device falls into the avalanche breakdown, and if the drain current cannot be limited externally, the device could be destroyed by the second breakdown. The following equation shows the dv/dt capability in this mode.

$$\left[\frac{dv}{dt}\right] = \frac{V_{be}}{R_b C_{db}}$$

From the above equation, it is easy to see that the dv/dt capability can be determined by the internal device structure. For high dv/dt capability, the R_b value must be small, and this can be maintained by increasing the doping level of P-body region, and reducing the length of the N^+ emitter as small as possible. R_b is also affected by the drain voltage, and as the drain voltage increases, the depletion layer expands and enlarges the R_b value. When the temperature increases, as R_b is increased by the reduction of mobility, and as the V_{be} decreases, the possibility of turn-on of the parasitic transistor increases. But as the base and the emitter is shorted by the source contact, the R_b value is very small. So, this won't happen unless the dv/dt is enormously large.

→ In false turn-on, the dv/dt can be controlled externally, but in parasitic transistor's turn-on, the dv/dt is determined by the device design. And this is the difference between these two modes.

(2) Dynamic dv/dt

If there is an sudden current interruption such as clamped inductive turn-off in high speed switching, the device is destroyed by the simultaneous stresses such as high drain current, high drain-source voltage and the displacement current at the parasitic capacitance.

(3) Diode recovery dv/dt

It is the most problem causing characteristics and in a specific application such as circuit using body drain diode, it is the main cause for the dv/dt failure. So the maximum value of dv/dt is stated in the data book so that the device can be used where it doesn't go over the diode recovery dv/dt ability. Fig. 19 shows the motor control circuit application which has diode recovery dv/dt problem.

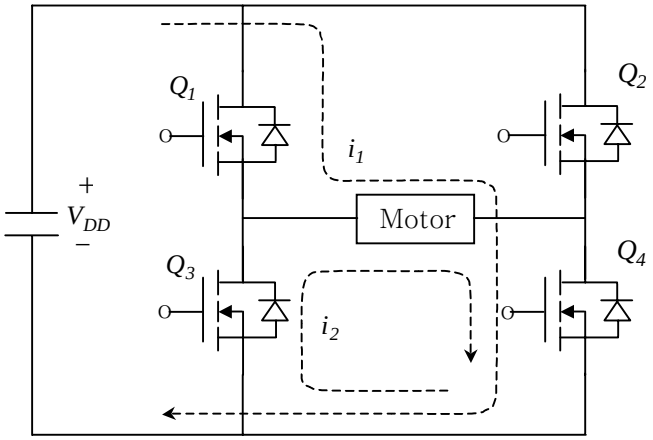


Fig. 19. motor control circuit

First, Q_1 and Q_4 becomes conducted, and in the state where the current i_1 pass has been formed, if the Q_1 is turned-off for the motor speed control, the current flows through the parasitic diode (freewheeling diode) of Q_3 as i_2. At this time, the parasitic diode of Q_3 falls into the forward bias state, and due to the characteristic of the diode, the minority charge starts to accumulate. And when the Q_1 is turned on, the current pass again becomes i_1, and the minority charge accumulated in the parasitic diode Q_3 is removed by the diode reverse recovery current. (Fig. 20. section a of I_S). Once the minority charge have been removed in certain level, the depletion region of the body drain diode expands and makes more serious reverse recovery current (Fig. 20. section b of I_S), and if this turns on the parasitic bipolar transistor, the Q_3 is destroyed. Fig. 20 shows the diode recovery dv/dt test circuit & waveforms in our data book, and from this test, not only dv/dt but also V_{SD} (diode forward voltage), t_{rr} (reverse recovery time), and Q_{rr} (reverse recovery charge) data could be obtained. In the test, the V_{DD} value must be less or equal to the BV_{DSS}, typically the V_{DD} is set as the 80[%] of BV_{DSS}, and the pulse period of driver V_{GS} must be controlled so that the I_S can become the continuous drain current I_D.

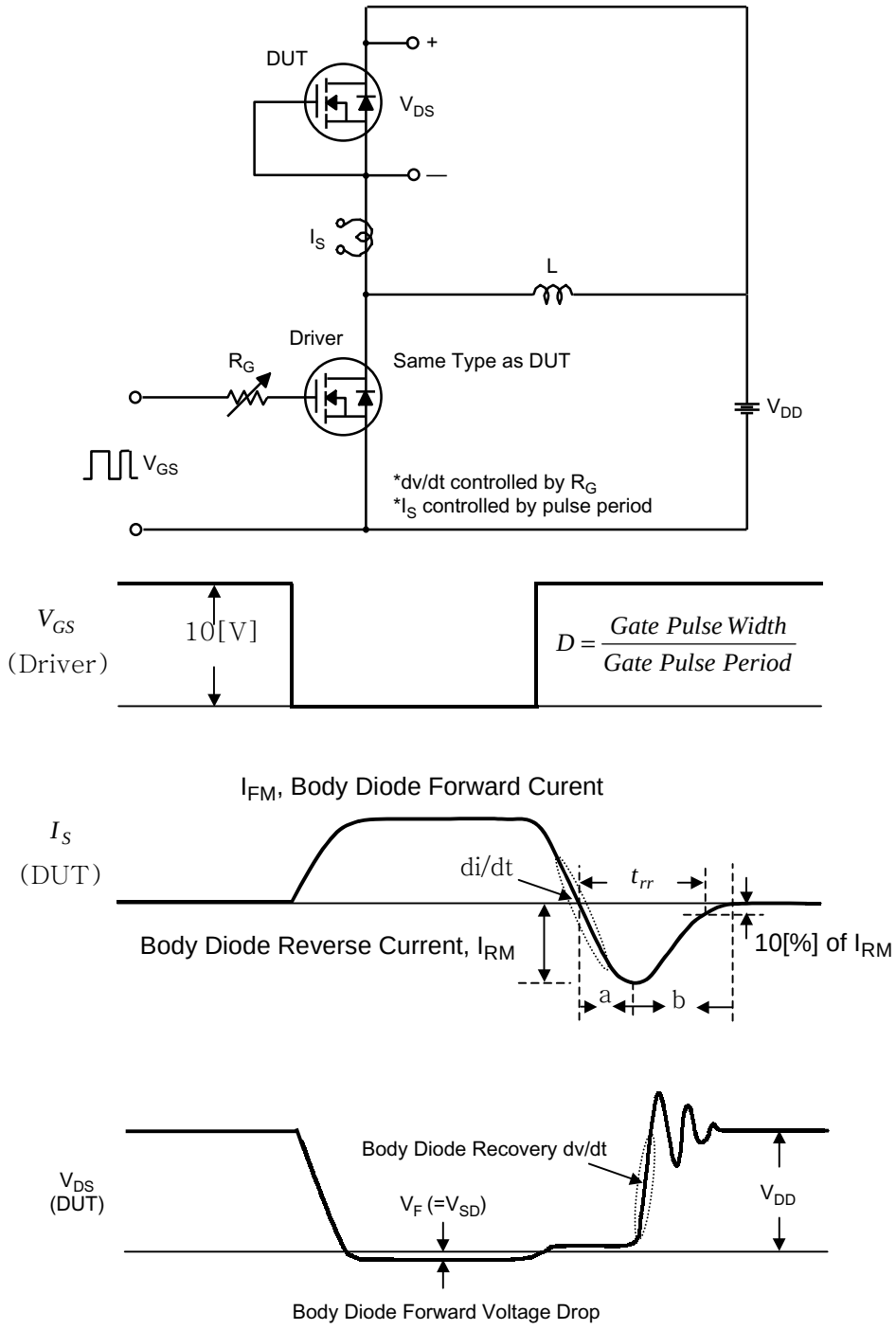


Fig. 20. Diode recovery dv/dt test circuit & waveforms

Rev C, November 1999

The value of di/dt and dv/dt becomes larger as R_G is reduced. First t_{rr} can be obtained by measuring the part shown in the wave of I_S where the di/dt (It is measured from the point where it is 50[%] of I_{FM} above the ground to the point where it is 75[%] of I_{RM} below the ground) is 100[A/μs], and Q_{rr} can be obtained as (I_{RM} x t_{rr})/2. dv/dt can be measured from the point where it is between 10[%] ~ 90[%] of V_{DD} with the di/dt condition (It is measured from the point where it is 50[%] of I_{FM} above the ground to the point where it is 75[%] of I_{FM} below the ground) stated at the data book. I_S (continuous source current), and I_{SM} (pulsed – source current) presents the current rating of the source – drain diode, and $I_S = I_D$ (continuous drain current), $I_{SM} = I_{DM}$ (drain current – pulsed).

14)Thermal Characteristics (T_J, $R_{\theta JC}$, $R_{\theta SA}$, $Z_{\theta JC}(t)$)

The power loss of the device is changed into heat and increases the junction temperature, and because of this, the characteristics of the device becomes worse and the lifetime reduces. So, it is very important to reduce the junction temperature by discharging the heat from the chip junction, and the thermal impedance ($Z_{\theta JC}(t)$) is used as a scale to evaluate these kinds of ability.

Meaning of the words for the thermal characteristics

T_J (Junction Temperature)

T_C (Case Temperature): Temperature of a point of the package which has the semiconductor chip inside.

T_S (Heat Sink Temperature)

T_A (Ambient Temperature) : Ambient temperature of the environment of the operating device.

$R_{\theta JC}$ (Junction – to – Case Thermal Resistance)

$R_{\theta CS}$ (Case – to – Sink Thermal Resistance)

$R_{\theta SA}$ (Sink – to – Ambient Thermal Resistance)

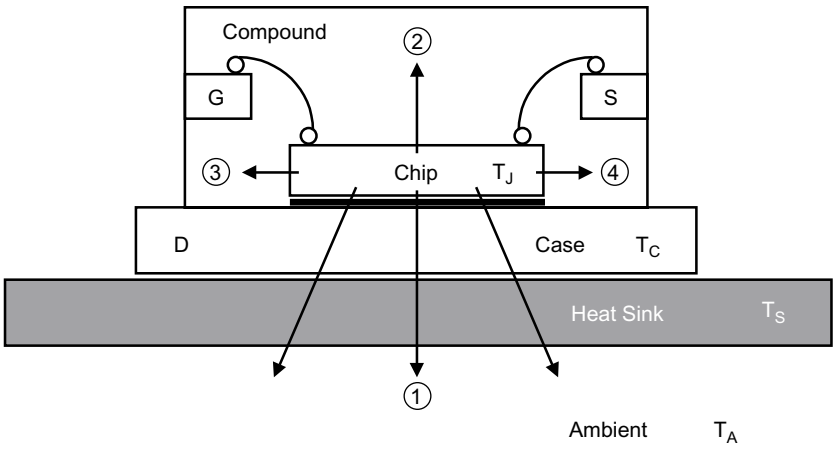


Fig. 21. The path of the thermal discharge at the chip junction

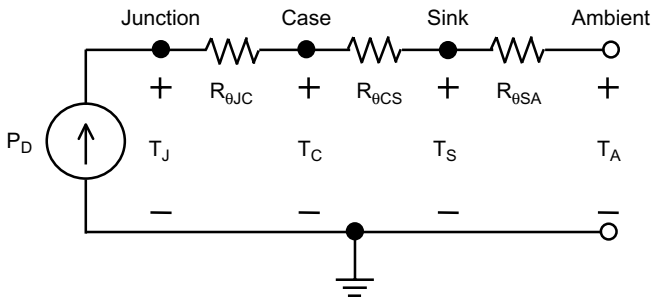


Fig. 22. An equivalent circuit based on thermal resistance

As in Fig. 21, the heat produced at the chip junction normally discharges over 80[%] in the direction of ① and discharges about 20[%] in the direction of ② ③ ④. The path of the thermal discharge can be regarded as same as the movement of the current, and it can be expressed as Fig. 22 considering the thermal resistance. But this is only for the DC operation, and most operation in real MOSFET application is a switching operation with fixed duty factor, so it is presented as the thermal impedance as the thermal capacitance should be taken into the consideration along with the thermal resistance. The thermal resistance from chip junction to the ambient is $R_{\theta JA}$ (junction – to – ambient thermal resistance), and the equivalent circuit could be expressed as following equation.

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA}$$

1. $R_{\theta JC}$ (Junction – to – Case Thermal Resistance)
   $R_{\theta JC}$ is the internal thermal resistance at the chip junction to the package case. And when the size of the die is fixed, it is the thermal resistance of pure package where it is determined by the package design, and lead frame material. $R_{\theta JC}$ can be measured under the condition of T_C = 25[°C] and can be written as the following equation.

$$R_{\theta JC} = \frac{T_J - T_C}{P_D} [°C/W]$$

   The condition T_C = 25[°C] means that the infinite heat sink has been mounted.

   - Infinite heat sink: The case temperature of the Package is equal to the environment temperature. It is the heat sink, which can realize $T_C = T_A$.

2. $R_{\theta CS}$ (Case – to – Sink Thermal Resistance)
   It is the thermal resistance from the package case to the heat sink. And it can be different due to the package and the mounting method to the heat sink.

3. $R_{\theta SA}$ (Sink – to – Ambient Thermal Resistance)
   It is the thermal resistance from the heat sink to the ambient, and it is determined by the heatsink design.

Thermal Response Characteristics

Fig. 11 of the data book, the graph of the thermal response, shows the change of $Z_{\theta JC}(t)$ (junction–to–case thermal impedance) due to the change of the square wave pulse duration with few duty factor condition. $Z_{\theta JC}(t)$ can decide the junction temperature rise with the equation of @ Notes: 3. $T_{JM}–T_C=P_{DM}*Z_{\theta JC}(t)$ (Considering the power dissipation being a constant value (P_{DM}) during conduction period as in Fig. 11 of the data book) , and it becomes saturated to the maximum value of ($R_{\theta JC}$) as it reaches the low frequency or into the DC operation where the duty factor D=1. Fig. 23 shows the junction temperature rise increases with the increasing duty factor.

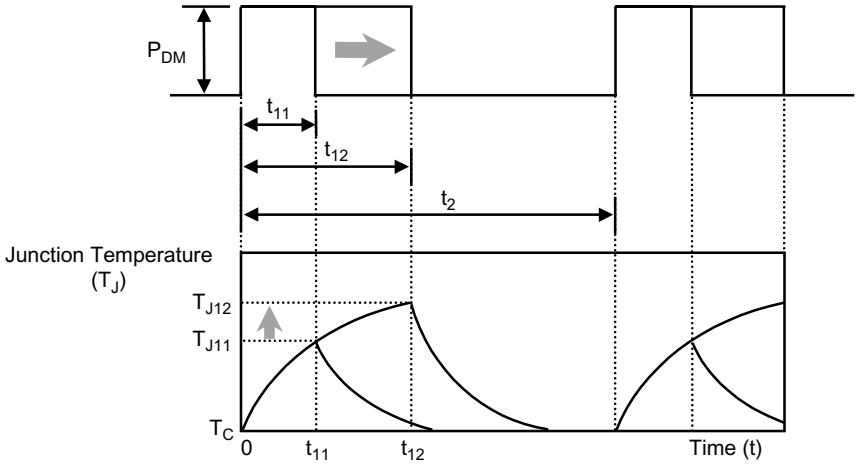


Fig. 23. The change of junction temperature due to the conduction time

A single pulse curve determines the thermal resistance for a repetitive power pulses having a constant duty factor (D) as following equation.

$$Z_{\theta JC}(t) = R_{\theta JC} \bullet D + (1–D) \bullet S_{\theta JC}(t)$$

where $Z_{\theta JC}(t)$: thermal impedance for the repetitive power pulses with the duty factor D.

$S_{\theta JC}(t)$: thermal impedance for the single pulse.

15) Continuous Drain Current (I_D), Drain Current - Pulsed (I_{DM})

(1) Continuous Drain Current (I_D)

As shown in the equation below, the I_D rating is determined by the heat removal ability of the device. Fig. 10. of the data book, the graph of max. drain current vs. case temperature, shows the increasing permissible I_D as T_C decreases.

$$I_D(T_C) = \sqrt{\frac{T_{Jmax} - T_C}{R_{DS(on)}(T_{Jmax}) \bullet R_{\theta JC}}}$$

Where $R_{DS(on)}(T_{Jmax})$: maximum value of on-resistance in appropriate drain current condition ($\frac{1}{2} \bullet I_D$ in the data book) at T_{Jmax}. as maximum $R_{DS(on)}$ specified in the data book is at T_C = 25[°C], $R_{DS(on)}$ (T_{Jmax}) could easily be analogized by the Fig. 8's graph of on-resistance vs. temperature in the data book.

$R_{\theta JC}$: maximum junction – to – case thermal resistance

T_C: case temperature

In real device application where it is unable to maintain the temperature at the T_C = 25[°C] and keeps increasing, the I_D(60 ~ 70 [%] of I_D at T_C = 25[°C]) at T_C = 100[°C] is more usable specification.

(2) Drain Current - Pulsed (I_{DM})

The drain current over continuous drain current rating is permitted where it doesn't go over maximum junction temperature, and the maximum upper limit is I_{DM}. I_{DM} is about 4 times the value of I_D as shown in the following equation.

$$I_{DM} = I_D(T_C = 25[°C]) \times 4$$

Repetitive rating: Pulse width limited by maximum junction temperature

16) Total Power Dissipation (P_D), Linear Derating Factor

(1) $P_D(T_C) = I_D^2(T_C) \bullet R_{DS(on)}(T_{Jmax}) = \frac{T_{Jmax} - T_C}{R_{\theta JC}}$

(2) Linear derating factor = $\frac{1}{R_{\theta JC}}$

17) Safe Operating Areas (SOA)

(1) SOA (FBSOA):

It defines the maximum value of the drain – source voltage and drain current which can guarantee the safe operation when the device is at the forward bias.

(2) Boundaries

1. The right - hand boundary : maximum drain – source voltage rating
2. The horizontal line :
   DC: maximum rated continuous drain current at T_C = 25[°C].

   For MOSFETs, excluding package limitations, maximum rated continuous drain current can be determined by the $R_{DS(on)}(T_{Jmax})$ as the equation below.

$$I_D(T_C) = \sqrt{\frac{T_{Jmax} - T_C}{R_{DS(on)}(T_{Jmax}) \bullet R_{\theta JC}}}$$

   Single pulse: Maximum rated drain current - pulsed

$$I_{DM} = I_D(T_C) \times 4$$

3. The upper limit with + slope: The boundary where the power can be limited by the drain – to – source on – resistance.
4. The upper limit with – slope : It is determined by the transient thermal impedance and the maximum junction temperature

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™
CoolFET™
CROSSVOLT™
E^2CMOS^{TM}
FACT™
FACT Quiet Series™
FAST®
FASTr™
GTO™
HiSeC™
ISOPLANAR™
MICROWIRE™
POP™
PowerTrench®
QFET™
QS™
Quiet Series™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
TinyLogic™
UHC™
VCX™

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.
As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.