

SN74ALVCH16269 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS SCES019N-JULY 1995-REVISED JULY 2004

FEATURES

- Member of the Texas Instruments Widebus™ Family
- Operates From 1.65 V to 3.6 V
- Max t_{pd} of 5 ns at 3.3 V
- ±24-mA Output Drive at 3.3 V
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

DESCRIPTION/ORDERING INFORMATION

This 12-bit to 24-bit registered bus exchanger is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH16269 is used in applications in which two separate ports must be multiplexed onto, or demultiplexed from, a single port. The device is particularly suitable as an interface between DRAMs synchronous and high-speed microprocessors.

Data is stored in the internal B-port registers on the low-to-high transition of the clock (CLK) input when the appropriate clock-enable (CLKENA) inputs are low. Proper control of these inputs allows two sequential 12-bit words to be presented as a 24-bit word on the B port. For data transfer in the B-to-A direction, a single storage register is provided. The select (SEL) line selects 1B or 2B data for the A outputs. The register on the A output permits the fastest possible data transfer, extending the period during which the data is valid on the bus. The control terminals are registered so that all transactions are synchronous with CLK. Data flow is controlled by the active-low output enables (OEA, OEB1, OEB2).

DGG	-	DL PAC	KAGE
	(TOF	P VIEW)	
	2 3	55 54] OEB2] CLKENA2] 2B4] GND] 2B5] 2B6] V _{CC}
			2B7 2B8 2B9
GND A4	11		GND 2B10
A6 A7 A8			2B12 1B12 1B11
A9 GND A10	17 18	40 39	1B10 GND 1B9
A11 A12 V _{CC}	20 21 22	37 36 35	1B8 1B7 V _{CC}
1B1 1B2 GND 1B3 NC	25 26	31] 1B6] 1B5] GND] 1B4] CLKENA1
SEL	28	29	Ĵсlk

NC - No internal connection

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
	SSOP - DL		SN74ALVCH16269DL	ALVCH16269	
	SSOF - DL	Tape and reel	SN74ALVCH16269DLR	ALVCH10209	
-40°C to 85°C	TSSOP - DGG	Tape and reel	SN74ALVCH16269DGGR	ALVCH16269	
	VFBGA - GQL	Topo and real	SN74ALVCH16269KR	- VH269	
	VFBGA - ZQL (Pb-free)	Tape and reel	74ALVCH16269ZQLR		

(1) Package drawings, standard packing guantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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DESCRIPTION/ORDERING INFORMATION (CONTINUED)

To ensure the high-impedance state during power up or power down, a clock pulse should be applied as soon as possible, and \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. Due to \overline{OE} being routed through a register, the active state of the outputs cannot be determined before the arrival of the first clock pulse.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

GQL OR ZQL PACKAGE (TOP VIEW)

	_	1	2	3	4	5	6	
Α	$\left(\right)$			С				
в		О	С	С	С	С	С	
С		С	С	\bigcirc	С	С	С	
D		С	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	
Е		С	\bigcirc			С	С	
F		С	\bigcirc			\bigcirc	\bigcirc	
G		С	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	
н		\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	
J		С	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	
κ		С	\bigcirc	\bigcirc	С	\bigcirc	С	
								/

TERMINAL ASSIGNMENTS

	1	2	3	4	5	6
Α	2B3	OEB1	OEA	OEB2	CLKENA2	2B4
В	2B1	2B2	GND	GND	2B5	2B6
С	A2	A1	V _{CC}	V _{CC}	2B7	2B8
D	A4	A3	GND	GND	2B9	2B10
Е	A6	A5			2B11	2B12
F	A7	A8			1B11	1B12
G	A9	A10	GND	GND	1B9	1B10
Н	A11	A12	V _{CC}	V _{CC}	1B7	1B8
J	1B1	1B2	GND GND		1B5	1B6
κ	1B3	NC	SEL	CLK	CLKENA1	1B4

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FUNCTION TABLES

OUTPUT ENABLE

I	NPUTS	6	OUTPUTS				
CLK	CLK OEA OEB		Α	1B, 2B			
\uparrow	↑нн		Z	Z			
↑	н	L	Z	Active			
\uparrow	LH		Active	Z			
\uparrow	L	L	Active	Active			

A-TO-B STORAGE ($\overline{OEB} = L$)

	INPUTS			OUTI	PUTS
CLKENA1	CLKENA1 CLKENA2		Α	1B	2B
L	Н	\uparrow	L	L	2B ₀ ⁽¹⁾
L	Н	\uparrow	Н	Н	2B ₀ ⁽¹⁾
L	L	\uparrow	L	L	L
L	L	\uparrow	Н	н	Н
н	L	\uparrow	L	1B ₀ ⁽¹⁾	L
н	L	\uparrow	н	1B ₀ ⁽¹⁾	Н
Н	Н	Х	Х	1B ₀ ⁽¹⁾	2B ₀ ⁽¹⁾

(1) Output level before the indicated steady-state input conditions were established

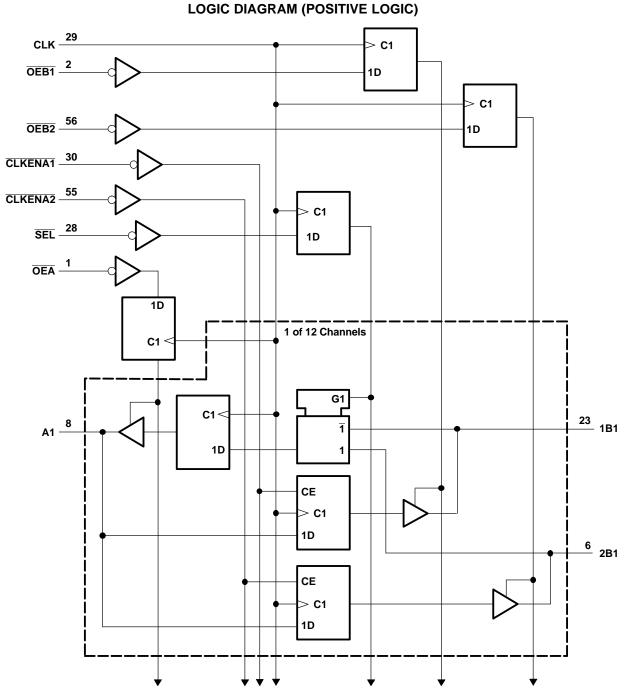
B-TO-A	STORAGE	$(\overline{OEA} = L)$
--------	---------	------------------------

	INPU	JTS		OUTPUT
CLK	SEL	1B	2B	Α
Х	Н	Х	Х	A ₀ ⁽¹⁾ A ₀ ⁽¹⁾
Х	L	Х	Х	A ₀ ⁽¹⁾
↑	Н	L	Х	L
↑	Н	Н	Х	н
↑	L	Х	L	L
↑	L	Х	Н	Н

 Output level before the indicated steady-state input conditions were established

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Pin numbers shown are for the DGG and DL packages.



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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range	Supply voltage range			
V	Innut voltogo rongo	Except I/O ports ⁽²⁾	-0.5	4.6	V
VI	Input voltage range	I/O ports ⁽²⁾⁽³⁾	-0.5	V _{CC} + 0.5	v
Vo	D Output voltage range ⁽²⁾⁽³⁾		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V ₁ < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
I _O	Continuous output current			±50	mA
	Continuous current through each V_{CC} or GN	1D		±100	mA
		DGG package		81	
θ_{JA}	Package thermal impedance ⁽⁴⁾	DL package		74	°C/W
		GQL/ZQL package		42	
T _{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) This value is limited to 4.6 V maximum.

(2)

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		1.65	3.6	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 imes V_{CC}$		
VIH	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	($0.35 \times V_{CC}$	
VIL	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
VI	Input voltage		0	V _{CC}	V
Vo	Output voltage		0	V _{CC}	V
-		V _{CC} = 1.65 V		-4	
		V _{CC} = 2.3 V		-12	س ۸
I _{OH}	High-level output current	$V_{CC} = 2.7 V$	-12		mA
		$V_{CC} = 3 V$		-24	
		V _{CC} = 1.65 V		4	
	Level and a devidence of	V _{CC} = 2.3 V		12	
I _{OL}	Low-level output current	$V_{CC} = 2.7 V$	$V_{CC} = 2.7 V$		mA
		$V_{CC} = 3 V$		24	
$\Delta t/\Delta v$	Input transition rise or fall rate	· · · ·		10	ns/V
T _A	Operating free-air temperature		-40	85	°C

 All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP ⁽¹⁾	MAX	UNIT
	I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} - 0.2			
	I _{OH} = -4 mA	1.65 V	1.2			
	I _{OH} = -6 mA	2.3 V	2			
V _{OH} V _{OL}		2.3 V	1.7			V
	I _{OH} = -12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = -24 mA	3 V	2			
	I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	
	I _{OL} = 4 mA	1.65 V			0.45	
	I _{OL} = 6 mA	2.3 V			0.4	
VOL	1	2.3 V			0.7	V
	$I_{OL} = 12 \text{ mA}$	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	$V_{I} = V_{CC} \text{ or } GND$	3.6 V			±5	μA
	V _I = 0.58 V	1.65 V	25			
	V _I = 1.07 V	1.65 V	-25			
	V _I = 0.7 V	2.3 V	45			
I _{I(hold)}	V _I = 1.7 V	2.3 V	-45			μA
	V _I = 0.8 V	3 V	75			
	V ₁ = 2 V	3 V	-75			
	$V_{\rm I} = 0$ to 3.6 V ⁽²⁾	3.6 V			±500	
I _{OZ} ⁽³⁾	$V_0 = V_{CC}$ or GND	3.6 V			±10	μA
I _{CC}	$V_{I} = V_{CC}$ or GND, $I_{O} = 0$	3.6 V			40	μA
ΔI_{CC}	One input at V_{CC} - 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			750	μA
C _i Control inputs	$V_{I} = V_{CC} \text{ or } GND$	3.3 V		3.5		pF
Cio A or B ports	$V_{O} = V_{CC}$ or GND	3.3 V		9		pF

TEXAS

STRUMENTS www.ti.com

(1) All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$. (2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.



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TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			V _{CC} =	$V_{CC} = 1.8 V$ $V_{CC} = 2.5 V$ $\pm 0.2 V$		V _{CC} = 2.7 V		V _{CC} = ± 0.3		UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	,		(1)		135		135		135	MHz
tw	Pulse duration,	CLK high or low	(1)		3.3		3.3		3.3		ns
		A data before CLK [↑]	(1)		2		2		1.7		
		B data before CLK↑	(1)		2.2		2.1		1.8		
t _{su}	Setup time	SEL before CLK↑	(1)		1.6		1.6		1.3		ns
		CLKENA1 or CLKENA2 before CLK↑	(1)		1		1.2		0.9		
		OE before CLK↑	(1)		1.5		1.6		1.3		
		A data after CLK↑	(1)		0.7		0.6		0.6		
		B data after CLK↑	(1)		0.7		0.6		0.6		
t _h	Hold time	SEL after CLK↑	(1)		1.1		0.7		0.7		ns
		CLKENA1 or CLKENA2 after CLK1	(1)		1		0.8		1.1		
1		OE after CLK↑	(1)		0.8		0.8		0.8		

(1) This information was not available at the time of publication.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{cc} =	= 1.8 V	V _{CC} = 2 ± 0.2	2.5 V V	V _{CC} = 2	2.7 V	V _{CC} = 3 ± 0.3	8.3 V V	UNIT
	(INPUT)	(001901)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			(1)		135		135		135		MHz
	CLK	В		(1)	1	8.2		7.3	1	6.2	20
t _{pd}	ULK	A		(1)	1	6.4		5.8	1	5	ns
		В		(1)	1	7.9		6.7	1	6.1	20
t _{en}	CLK	A		(1)	1	7.6		6.2	1	5.9	ns
		В		(1)	1	8.1		6.9	1	6.1	20
t _{dis}	CLK	А		(1)	1	7.5		6.8	1	5.6	ns

(1) This information was not available at the time of publication.

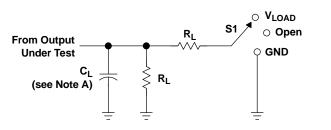
OPERATING CHARACTERISTICS

 $T_A = 25^{\circ}C$

PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT	
<u> </u>	Power dissipation capacitance per exchanger	All outputs enabled		(1)	87	120	pF	
C _{pd}		All outputs disabled	C _L = 50 pF, f = 10 MHz	(1)	80.5	118		

(1) This information was not available at the time of publication.





LOAD CIRCUIT

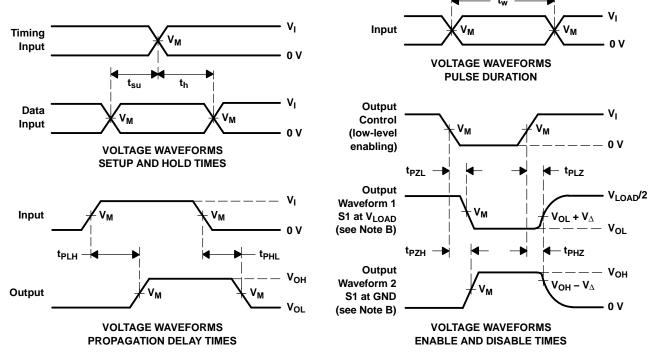
TEST	S1
t _{pd}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

IEXAS *IRUMENTS*

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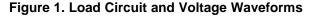
Γ	N.	INPUT		V	v	<u>^</u>	Б	v	
	V _{CC}	VI	t _r /t _f	V _M	V _{LOAD}	C∟	RL	V_{Δ}	
	1.8 V	V _{CC}	≤2 ns	V _{CC} /2	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V	
	2.5 V \pm 0.2 V	V _{CC}	≤2 ns	V _{CC} /2	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V	
	2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V	
	3 V \pm 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V	

PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control. C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.





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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
74ALVCH16269DGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74ALVCH16269DGGRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74ALVCH16269DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74ALVCH16269DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALVCH16269DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALVCH16269DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALVCH16269DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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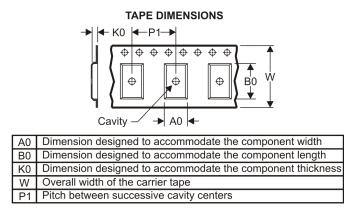
PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVCH16269DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74ALVCH16269DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

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PACKAGE MATERIALS INFORMATION

29-Jul-2011



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVCH16269DGGR	TSSOP	DGG	56	2000	346.0	346.0	41.0
SN74ALVCH16269DLR	SSOP	DL	56	1000	346.0	346.0	49.0

MECHANICAL DATA

MSSO001C - JANUARY 1995 - REVISED DECEMBER 2001

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

DL (R-PDSO-G**)



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118



MECHANICAL DATA

MTSS003D - JANUARY 1995 - REVISED JANUARY 1998

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153



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