

Approved	Design

TOSHIBA SD Card Specification



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Revision Histories

Application

This document describes the specifications of the Toshiba standard SD Card.

To commence the design of the host system for SD Card, please confirm the latest information and refer the 9.Host Interface design notes.

1.Production Code

Toshiba Standard SD Card:

	Capacity	Model Name	Production Code
SD Card	256MB	SD-M2564B1	20533815



2. Product Overview

The SD Card is a Memory Card of Small and Thin with SDMI compliant Security method.

(SDMI: Secure Digital Music Initiative)

Contents in the Card can be protected by CPRM based security. This contents security can be accomplished by SD Card, host, and security application software combinations.

3.SD Card Features

Table 1:SD card Features

Label Design, Contents, Media Format

Design	Toshiba Standard (Fig .1)	
Contents	None (OEM Design Available)	ID, MKB
Security Functions	SD Security Specification Ver.1.0 Compliant (CPRM Based) *CPRM: Contents Protection for Recording Media Specification	Programmed (Toshiba Specific)
Logical Format	SD File System Specification Ver.1.0 Compliant (DOS-FAT Based formatted)	

Physical, Electrical

Electrical	Operating Voltage: 2.7V to 3.6 V (Memory Operation) Interfaces: SD Card Interface, (SD: 4 or 1bit) SPI Mode Compatible SD Physical Layer Specification Ver.1.0 Compliant	
Physical	L: 32, W: 24, T: 2.1 (mm), Weight: 3g (Max) 2g (typ.) SD Physical Layer Specification Ver.1.0 Compliant (Detailed Dimensions attached: sheet. 1)	
Durability	SD Physical Layer Specification Ver.1.0 Compliant	

Accessories

Guarantee	Not Applied (Available with OEM requirement)	
Description	Not Applied (Available with OEM requirement)	
Card Case	Not Applied (Available with OEM requirement)	
Card Label	Not Applied (Available with OEM requirement)	
Packaging	Not Applied (Available with OEM requirement)	

4. Compatibility

Compliant Specifications

- SD Memory Card Specifications
 - Compliant with PHYSICAL LAYER SPECIFICATION Ver.1.0. (Part1)
 - Compliant with FILE SYSTEM SPECIFICATION Ver.1.0. (Part2)
 - Compliant with SECURITY SPECIFICATION Ver.1.0. (Part3)

Supplementary Explanation are described in “ 8.Others: Limited Conditions, SD Specification Compliance” in this document.

5. Physical Characteristics

5.1. Environmental Characteristics

1) Standard Operation Conditions

Absolute Maximum Temperature Range: $T_a = -25$ to $+85$ degrees centigrade
(Humidity less than RH = 95 %, Non condensed)

Recommended Operating Conditions: $T_a = 0$ to $+55$ degrees centigrade
(Humidity RH = 20% to 85 % Non condensed)

Note:

Absolute maximum temperature range shows the maximum range which can operate in some condition, and DOES NOT mean a guaranteed operation in any conditions.

For the Stable operations, the recommended operating conditions are suggested or please ask for the customized conditions to Toshiba sales representatives.

2) Storage Temperature

Absolute Maximum Temperature Range: $T_{stg} = -40$ to $+85$ degrees centigrade
(Humidity less than RH = 95% Non condensed)

Recommended Storage Conditions: $T_{stg} = -20$ to $+65$ degrees centigrade
(Humidity RH = 5% to 85% Non condensed)

Note:

Absolute maximum temperature range shows the maximum range to store.

However, DOES NOT mean a guaranteed conditions for long term.

There are some impacts on the SD card if stored in this temperature rage for long term.

For the long term storage period, the recommended storage conditions is suggested or please ask for the customized conditions to Toshiba sales representatives.

5.2.Physical Characteristics**1) Hot Insertion or Removal**

Toshiba SD Card can remove or insert without power off the host system described in the SD Physical Layer Specification 8.3.1.

The connector to realize the Hot Insertion or Removal is defined in the 9.2.2. of the PHYSICAL LAYER SPECIFICATION.

2) Mechanical Write Protect Switch

A mechanical sliding tablet on the side of the card can use for write protect switch. The host system shall be responsible for this function.

The card is in a “Write Protected” status when the tablet is located on the “Lock “ position. The host system shall not write nor format the card in this status.

The card is in “Write Enabled” status when the tablet is moved to the opposite position (Un-Lock). (Please refer the figures below for the tablet polarity.)

Please slide the tablet till the dead end (stopped position).

The tablet is set on the “Write Enabled” position when it is shipped.

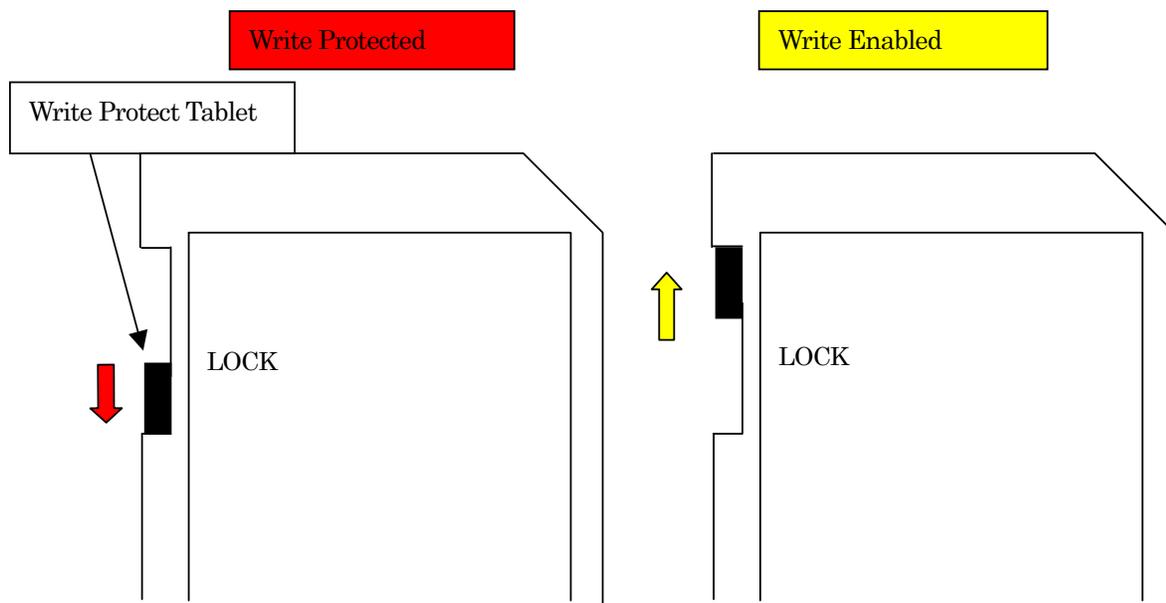


Fig 2: Write Protect Tablet Polarity (Front View)

6. Electrical Interface outlines

6.1. SD card pins

Table 2 describes the pin assignment of the SD card.
 Fig.3 describes the pin assignment of the SD card.

Please refer the detail descriptions by SD Card Physical Layer Specification.

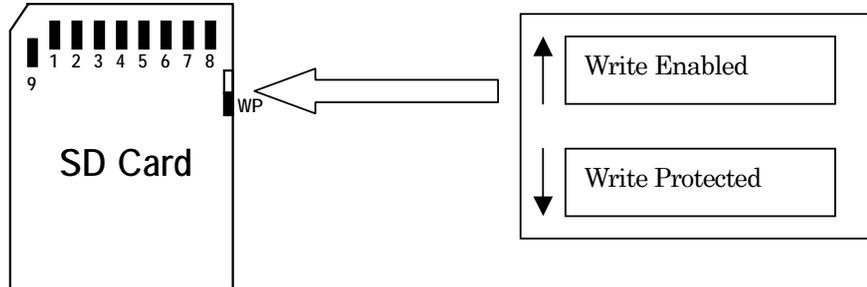


Fig3: SD Card Pin assignment (Back view of the Card)

Table 2:SD card pin assignment

Pins	SD Mode			SPI Mode		
	Name	IO type ¹	Description	Name	IO Type	Description
1	CD/ DAT3	I/O /PP	Card Detect/ Data Line [Bit3]	CS	I	Chip Select (Negative True)
2	CMD	PP	Command/Response	DI	I	Data In
3	V _{SS1}	S	Ground	V _{SS}	S	Ground
4	V _{dd}	S	Supply Voltage	V _{dd}	S	Supply Voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V _{SS2}	S	Ground	V _{SS2}	S	Ground
7	DAT0	I/O /PP	Data Line [Bit0]	DO	O/PP	Data Out
8	DAT1	I/O /PP	Data Line [Bit1]	RSV	-	Reserved (*)
9	DAT2	I/O /PP	Data Line [Bit2]	RSV	-	Reserved (*)

1) S: Power Supply, I: Input, O: Output, I/O: Bi-directionally, 'PP' - IO using push-pull drivers

(*) These signals should be pulled up by host side with 10-100k ohm resistance in the SPI Mode.

6.2 SD Card Bus Topology

The SD Memory Card supports two alternative communication protocols: SD and SPI Bus Mode.

Host System can choose either one of modes. Same Data of the SD Card can read and write by both modes.

SD Mode allows the 4-bit high performance data transfer. SPI Mode allows easy and common interface for SPI channel.

The disadvantage of this mode is loss of performance, relatively to the SD mode.

6.2.1 SD Bus Mode protocol

The SD bus allows the dynamic configuration of the number of data line from 1 to 4 Bi-directional data signal. After power up by default, the SD card will use only DAT0. After initialization, host can change the bus width.

Multiplied SD cards connections are available to the host. Common V_{dd} , V_{ss} and CLK signal connections are available in the multiple connections. However, Command, Respond and Data lined (DAT0-DAT3) shall be divided for each card from host.

This feature allows easy trade off between hardware cost and system performance. Communication over the SD bus is based on command and data bit stream initiated by a start bit and terminated by stop bit.

Command:

Commands are transferred serially on the CMD line. A command is a token to starts an operation from host to the card. Commands are sent to an addressed single card (addressed Command) or to all connected cards (Broad cast command).

Response:

Responses are transferred serially on the CMD line.

A response is a token to answer to a previous received command. Responses are sent from an addressed single card or from all connected cards.

Data:

Data can be transfer from the card to the host or vice versa.

Data is transferred via the data lines.

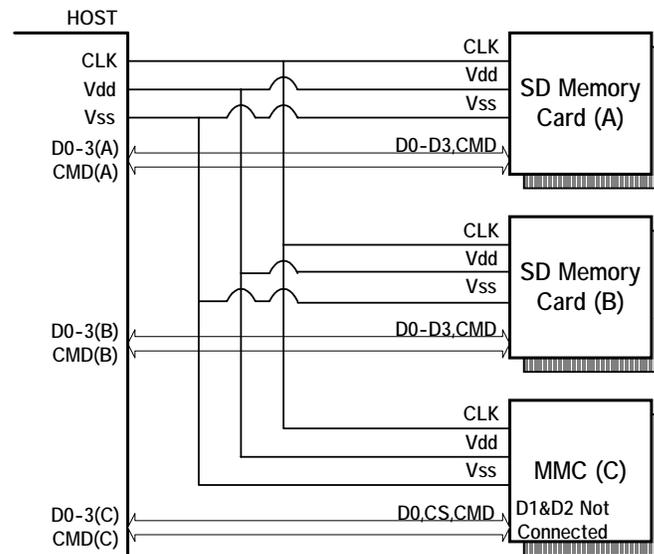


Fig 4: SD Card (SD Mode) connection Diagram

- CLK : Host card Clock signal
- CMD : Bi-directional Command/ Response Signal
- DAT0 - DAT3: 4 Bi-directional data signal
- V_{dd} : Power supply
- V_{ss} : GND

Table 3.: SD Mode Command Set

(+: Implemented, -: Not Implemented)

CMD Index	Abbreviation	Implementa tion	Note
CMD0	GO_IDLE_STATE	+	
CMD2	ALL_SEND_CID	+	
CMD3	SEND_RELATIVE_ADDR	+	
CMD4	SET_DSR	-	DSR Register is not implemented.
CMD7	SELECT/DESELECT_CARD	+	
CMD9	SEND_CSD	+	
CMD10	SEND_CID	+	
CMD12	STOP_TRANSMISSION	+	
CMD13	SEND_STATUS	+	
CMD15	GO_INACTIVE_STATE	+	
CMD16	SET_BLOCKLEN	+	
CMD17	READ_SINGLE_BLOCK	+	
CMD18	READ_MULTIPLE_BLOCK	+	
CMD24	WRITE_BLOCK	+	
CMD25	WRITE_MULTIPLE_BLOCK	+	
CMD27	PROGRAM_CSD	+	
CMD28	SET_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD29	CLR_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD30	SEND_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD32	ERASE_WR_BLK_START	+	
CMD33	ERASE_WR_BLK_END	+	
CMD38	ERASE	+	
CMD42	LOCK_UNLOCK	-	Card Lock/Unlock Function is not implemented.
CMD55	APP_CMD	+	
CMD56	GEN_CMD	-	This command is not specified.
ACMD6	SET_BUS_WIDTH	+	
ACMD13	SD_STATUS	+	
ACMD22	SEND_NUM_WR_BLOCKS	+	
ACMD23	SET_WR_BLK_ERASE_COUNT	+	
ACMD41	SD_APP_OP_COND	+	
ACMD42	SET_CLR_CARD_DETECT	+	
ACMD51	SEND_SCR	+	
ACMD18	SECURE_READ_MULTI_BLOCK	+	
ACMD25	SECURE_WRITE_MULTI_BLOCK	+	
ACMD26	SECURE_WRITE_MKB	+	
ACMD38	SECURE_ERASE	+	
ACMD43	GET_MKB	+	
ACMD44	GET_MID	+	
ACMD45	SET_CER_RN1	+	
ACMD46	SET_CER_RN2	+	
ACMD47	SET_CER_RES2	+	
ACMD48	SET_CER_RES1	+	
ACMD49	CHANGE_SECURE_AREA	+	

- CMD28, 29,30 and CMD42 are Optional Commands.
- CMD4 is not implemented because DSR register (Optional Register) is not implemented.
- CMD56 is for vender specific command. Which is not defined in the standard card.

6.2.2 SPI Bus mode Protocol

The SPI bus allows 1 bit Data line by 2-chanel (Data In and Out).

The SPI compatible mode allows the MMC Host systems to use SD card with little change.
The SPI bus mode protocol is byte transfers.

All the data token are multiples of the bytes (8-bit) and always byte aligned to the CS signal.

The advantage of the SPI mode is reducing the host design in effort.

Especially, MMC host can be modified with little change.

The disadvantage of the SPI mode is the loss of performance versus SD mode.

Caution: Please use SD Card Specification. DO NOT use MMC Specification.

For example, initialization is achieved by ACMD41, and be careful to Register. Register definition is different, especially CSD Register.

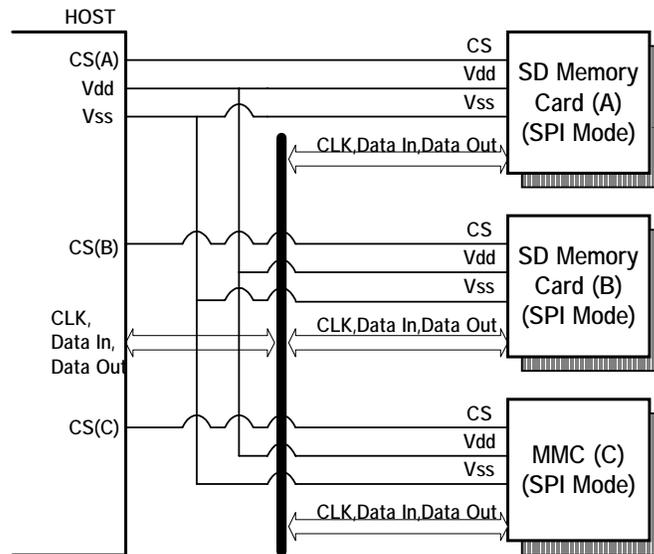


Fig 5: SD card (SPI mode) connection diagram

- CS: Card Select Signal
- CLK: Host card Clock signal
- Data in: Host to card data line
- Data out: card to host data line
- V_{dd} : Power supply
- V_{ss} : GND

Table.4: SPI Mode Command set
(+: Implemented, -: Not Implemented)

CMD Index	Abbreviation	Implementa tion	Note
CMD0	GO_IDLE_STATE	+	
CMD1	SEND_OP_CND	+	NOTICE: DO NOT USE (SEE Fig.6 and 9.2)
CMD9	SEND_CSD	+	
CMD10	SEND_CID	+	
CMD12	STOP_TRANSMISSION	+	
CMD13	SEND_STATUS	+	
CMD16	SET_BLOCKLEN	+	
CMD17	READ_SINGLE_BLOCK	+	
CMD18	READ_MULTIPLE_BLOCK	+	
CMD24	WRITE_BLOCK	+	
CMD25	WRITE_MULTIPLE_BLOCK	+	
CMD27	PROGRAM_CSD	+	
CMD28	SET_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD29	CLR_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD30	SEND_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD32	ERASE_WR_BLK_START_ADDR	+	
CMD33	ERASE_WR_BLK_END_ADDR	+	
CMD38	ERASE	+	
CMD42	LOCK_UNLOCK	-	Card Lock/Unlock Function is not implemented.
CMD55	APP_CMD	+	
CMD56	GEN_CMD	-	This command is not specified.
CMD58	READ_OCR	+	
CMD59	CRC_ON_OFF	+	
ACMD6	SET_BUS_WIDTH	+	
ACMD13	SD_STATUS	+	
ACMD22	SEND_NUM_WR_BLOCKS	+	
ACMD23	SET_WR_BLK_ERASE_COUNT	+	
ACMD41	SD_APP_OP_COND	+	
ACMD42	SET_CLR_CARD_DETECT	+	
ACMD51	SEND_SCR	+	
ACMD18	SECURE_READ_MULTI_BLOCK	+	
ACMD25	SECURE_WRITE_MULTI_BLOCK	+	
ACMD26	SECURE_WRITE_MKB	+	
ACMD38	SECURE_ERASE	+	
ACMD43	GET_MKB	+	
ACMD44	GET_MID	+	
ACMD45	SET_CER_RN1	+	
ACMD46	SET_CER_RN2	+	
ACMD47	SET_CER_RES2	+	
ACMD48	SET_CER_RES1	+	
ACMD49	CHANGE_SECURE_AREA	+	

- CMD28, 29,30 and CMD42 are Optional Commands.
- CMD56 is for vender specific command. Which is not defined in the standard card.

6.3. Card Initialize

To initialize the Toshiba SD card, follow the following procedure is recommended example.

1) Supply Voltage for initialization.

Host System can apply the Operating Voltage from initialization to the card.

Apply more than 74 cycles of Dummy-clock to the SD card.

2) Select operation mode (SD mode or SPI mode)

In case of SPI mode operation, host should drive 1 pin (CD/DAT3) of SD Card I/F to “Low” level. Then, issue CMD0.

In case of SD mode operation, host should drive or detect 1 pin of SD Card I/F (Pull up register of 1 pin is pull up to “High” normally).

Card maintain selected operation mode except re-issue of CMD0 or power on below is SD mode initialization procedure.

3) Send the ACMD41 with Arg = 0 and identify the operating voltage range of the Card.

4) Apply the indicated operating voltage to the card.

Reissue ACMD41 with apply voltage storing and repeat ACMD41 until the busy bit is cleared.

(Bit 31 Busy = 1) If response time out occurred, host can recognize not SD Card.

Note: In MMC-SPI Mode, CMD1 can use in this state.

However, **do not use CMD1 in case of SD Mode.**

5) Issue the CMD2 and get the Card ID (CID).

Issue the CMD3 and get the RCA. (RCA value is randomly changed by access, not equal zero)

6) Issue the CMD7 and move to the transfer state.

If necessary, Host may issue the ACMD42 and disabled the pull up resistor for Card detect.

7) Issue the ACMD13 and poll the Card status as SD Memory Card. Check SD_CARD_TYPE value. If significant 8 bits are “all zero”, that means SD Card. If it is not, stop initialization.

8) Issue CMD7 and move to standby state.

Issue CMD9 and get CSD.

Issue CMD10 and get CID.

9) Back to the Transfer state with CMD7.

Issue ACMD6 and choose the appropriate bus-width.

Then the Host can access the Data between the SD card as a storage device.

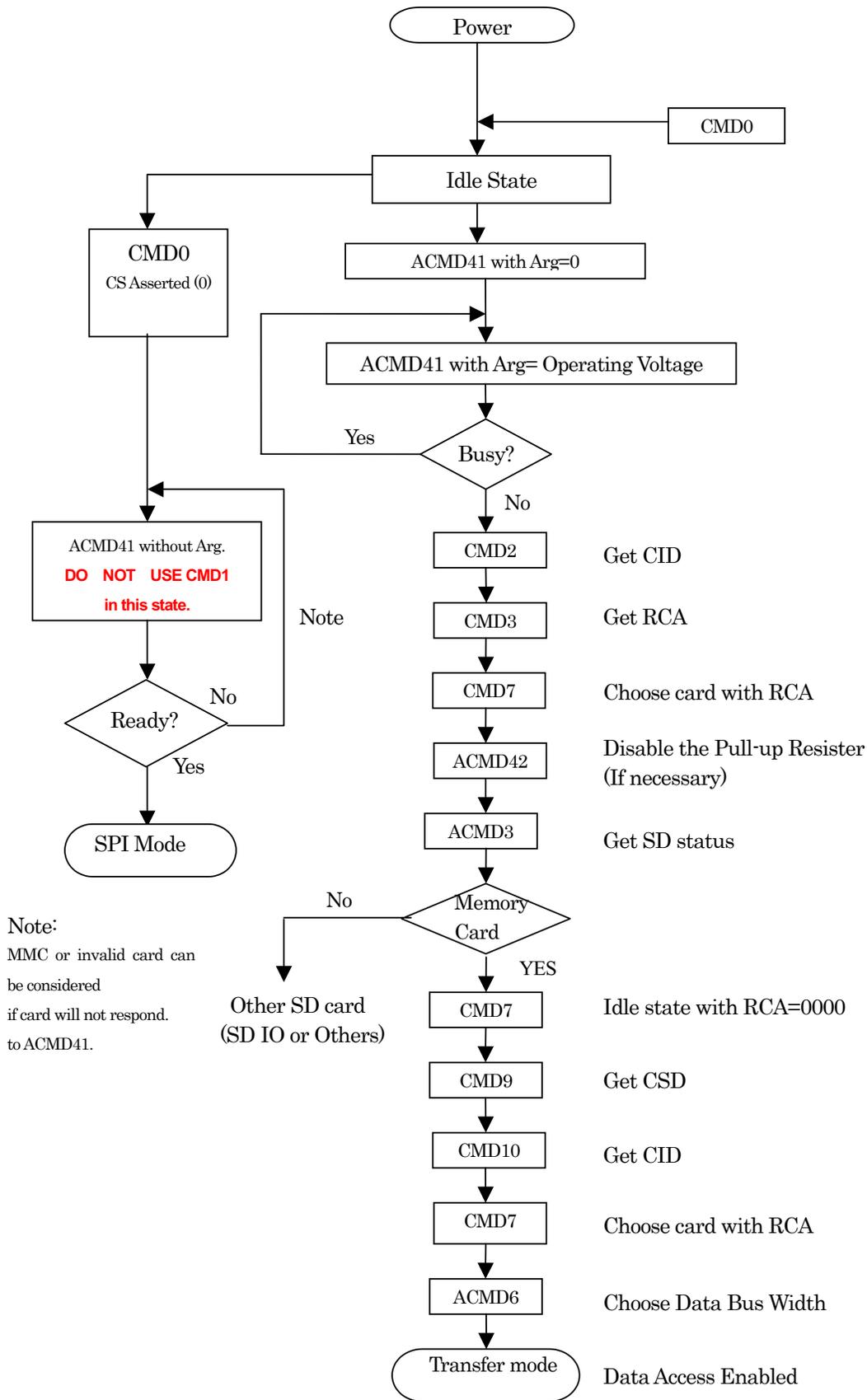


Fig 6. SD card Initialize Procedure

6.4. SD card Electrical Characteristics

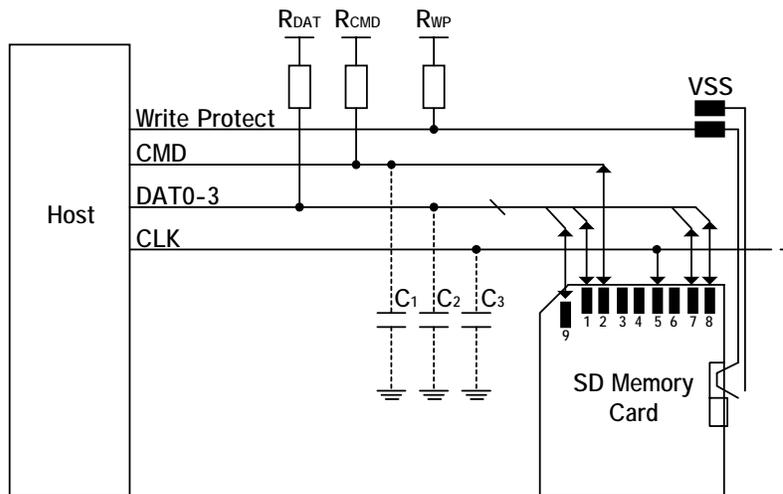


Fig7: SD card Connection diagram

6.4.1 Absolute Maximum Conditions

Table 5: Absolute Maximum Conditions

Item	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 to 5.0	V
Input Voltage	V_{IN}	-0.3 to $V_{DD}+0.3$	V

6.4.2 DC Characteristics

Table 6: DC Characteristics

Item	Symbol	Condition	MIN.	Typ.	MAX.	Unit	Note
Supply Voltage 1	V _{DD}	-	2.0	-	3.6	V	For CMD0, 15,55, ACMD41 Only
Supply Voltage 2		-	2.7	-	3.6	V	For All commands
Input Voltage	High Level	V _{IH}	-	VDD*0.625	-	-	V
	Low Level	V _{IL}	-	-	-	VDD*0.25	V
Output Voltage	High Level	V _{OH}	VDD = 2V IOH = -100uA	VDD*0.75	-	-	V
	Low Level	V _{OL}	VDD = 2V IOL = 100uA	-	-	VDD*0.125	V
Standby Current	I _{CC1}	3.6V Clock 25MHz	-	-	30	mA	
		2.7V Clock Stop	-	-	0.2		
Operation Voltage	I _{CC2}	3.6V/25MHz	-	-	80	mA	Write
		2.7V/25MHz	-	-	80		Read
Input Voltage Setup Time	Vrs	-	-	-	250	ms	

Table 7: Signal Capacitance

Item	Symbol	Min.	Max.	Unit	Note
Pull up Resistance	R _{CMD} R _{DAT}	10	100	K Ohm	
Bus Signal Line Capacitance	C _L	-	250	pF	F _{PP} <5MHz (21Cards)
Bus Signal Line Capacitance	C _L	-	100	pF	F _{PP} <20MHz (7Cards)
Single Card Capacitance	C _{CARD}	-	10	pF	
Pull up Resistance inside card(pin1)	R _{DAT3}	10	90	K Ohm	

Note: WP pull-up (R_{wp}) Value is depend on the Host Interface drive circuit.

6.4.3 AC Characteristics

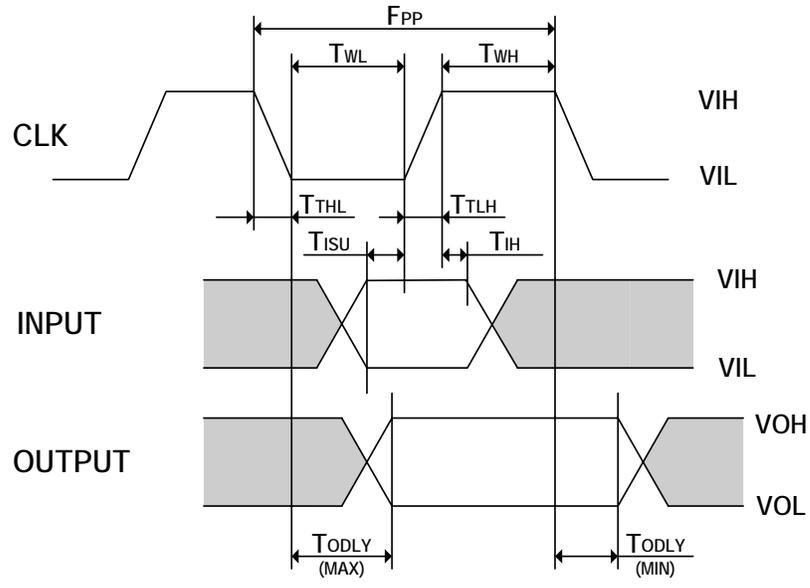


Fig 8: AC Timing Diagram

Table 8: AC Characteristics

Item	Symbol	Min.	Max.	Unit	Note
Clock Frequency (In any Sates)	F_{sty}	0	25	MHz	$CL < 100pF$ (7Cards)
Clock Frequency (Data transfer Mode)	F_{PP}	0.1	25	MHz	$CL < 100pF$ (7Cards)
Clock Frequency (Card identification Mode)	F_{OD}	100	400	kHz	$CL < 250pF$ (21Cards)
Clock Low Time	T_{WL}	10	-	ns	$CL < 100pF$ (7Cards)
Clock High Time	T_{WH}	10	-	ns	
Clock Rise Time	T_{TLH}	-	10	ns	
Clock Fall Time	T_{THL}	-	10	ns	
Clock Low Time	T_{WL}	50	-	ns	$CL < 250pF$ (21Cards)
Clock High Time	T_{WH}	50	-	ns	
Clock Rise Time	T_{TLH}	-	50	ns	
Clock Fall Time	T_{THL}	-	50	ns	
Input Setup Time	T_{ISU}	5	-	ns	$CL < 25pF$ (1Cards)
Input Hold Time	T_{IH}	5	-	ns	
Output Delay Time	T_{ODLY}	0	14	ns	

7.Card Internal Information

7.1. Security Information

MKB (Media Key Block) and Media ID are Toshiba Standard Information. These informations are compliance with the CPRM.

Note: The security information is NOT Development information for evaluation.

Host System shall be compliance with the CPRM to use the security function.

This information is kept as confidential because of security reasons.

7.2. SD Card Registers

The SD card has six registers and SD Status information: OCR, CID, CSD, RCA, DSR, SCR and SD Status.

DSR IS NOT SUPPORTED in this card.

There are two types of register groups.

MMC compatible registers: OCR, CID, CSD, RCA, DSR, and SCR

SD card Specific: SD Status

Table.9: SD card Registers

Resister Name	Bit Width	Description
OCR	32	Operation Conditions (VDU Voltage Profile and Busy Status Information)
CID	128	Card Identification information
CSD	128	Card specific information
RCA	16	Relative Card Address
DSR	16	Not Implemented (Programmable Card Driver): Driver Stage Register
SCR	64	SD Memory Card's special features
SD Status	512	Status bits and Card features

7.2.1. OCR Register

This 32-bit register describes operating voltage range and status bit in the power supply.
(Refer Appendix 2. for the detail)

Table.10: OCR register definition

OCR bit position	VDD voltage window	Initial value		
		64MB	128MB	256MB
31	Card power up status bit (busy)	"0" = busy "1" = ready		
30-24	reserved	All '0'		
23	3.6 – 3.5	1		
22	3.5 – 3.4	1		
21	3.4 – 3.3	1		
20	3.3 – 3.2	1		
19	3.2 – 3.1	1		
18	3.1 – 3.0	1		
17	3.0 – 2.9	1		
16	2.9 – 2.8	1		
15	2.8 – 2.7	1		
14	2.7 – 2.6	0		
13	2.6 – 2.5	0		
12	2.5 – 2.4	0		
11	2.4 – 2.3	0		
10	2.3 – 2.2	0		
9	2.2 – 2.1	0		
8	2.1 – 2.0	0		
7	2.0 – 1.9	0		
6	1.9 – 1.8	0		
5	1.8 – 1.7	0		
4	1.7 – 1.6	0		
3-0	reserved	All '0'		

bit 23-4: Describes the SD Card Voltage

bit 31 indicates the card power up status. Value "1" is set after power up and initialization procedure has been completed.

7.2.2. CID Register

The CID (Card Identification) register is 128-bit width. It contains the card identification information.
 (Refer Appendix 3. for the detail) The Value of CID Register is vender specific.

Tabel.11: CID Register

Field	Width	CID-slice	Initial Value		
			64MB	128MB	256MB
MID	8	[127:120]	02 h		
OID	16	[119:104]	"TM" (544D h)		
PNM	40	[103:64]	"SD064" (5344303634 h)	"SD128" (5344313238h)	"SD256" (5344323536h)
PRV	8	[63:56]	(a) Product revision		
PSN	32	[55:24]	(a) Product serial number		
-	4	[23:20]	All '0'		
MDT	12	[19:8]	(b) Manufacture date		
CRC	7	[7:1]	(c) CRC		
-	1	[0:0]	1		

(a), (b): Depends on the SD Card. Controlled by Production Lot.
 (c) Depends on the CID Register

• **MID**

8 bit binary number, Indicates the Manufacture ID allocated by the SDA.
 → 02 -h (Indicates Toshiba) (Unit: -h means Hex-decimal value, here after)

• **OID**

16 bit binary number, Indicates the Manufacture ID allocated by the SDA.
 → 544D -h = "TM" in ASCII String (Indicates Toshiba)

• **PNM**

5 ASCII Characters long (40 bit), Toshiba Product Code.
 → Toshiba Standard SD card indicates as below by capacity.
 64MB: "SD064"(5344303634 -h)
 128MB: "SD128"(5344313238 -h)
 256MB: "SD256"(5344323536 -h)

• **PRV**

Product Revision of the card.
 → Currently 00 -h = Rev.0. 0:This number may be changed without any notice by TOSHIBA.

• **PSN**

32 bit serial number of unsigned integer.
 → Uniquely assigned integer

• **MDT**

The manufacturing date composed of two-hexadecimal digits.
 → CID-Slice [11:8] Month Field (Exp. 1h = January)
CID-Slice [19:12] Year Field (Exp. 0h = 2000)

• **CRC**

Checksum of CID contents.
 → CRC 7 Checksum (See Chapter 7. of the SD PHYSICAL SPECIFICATION)

7.2.3. CSD Register

CSD is Card-Specific Data register provides information on 128bit width.
Some field of this register can writable by PROGRAM_CSD (CMD27).

Table.12: CSD Register

Field	Width	Cell Type ⁽¹⁾	CSD slice	Initial Value		
				64MB	128MB	256MB
CSD_STRUCTURE	2	R	[127:126]	00		
-	6	R	[125:120]	All '0'		
TAAC	8	R	[119:112]	0_0101_101(200us)		
NSAC	8	R	[111:104]	00000000		
TRAN_SPEED	8	R	[103:96]	0_0110_010(25Mbps)		
CCC	12	R	[95:84]	0_0_0_1_0_0_1_1_0_1_0_1		
READ_BL_LEN	4	R	[83:80]	1001(512Bytes)		
READ_BL_PARTIAL	1	R	[79:79]	1		
WRITE_BLK_MISALIGN	1	R	[78:78]	0		
READ_BLK_MISALIGN	1	R	[77:77]	0		
DSR_IMP	1	R	[76:76]	0		
-	2	R	[75:74]	All '0'		
C_SIZE	12	R	[73:62]	E27 -h	E6F -h	E93 -h
VDD_R_CURR_MIN	3	R	[61:59]	110(60mA)		
VDD_R_CURR_MAX	3	R	[58:56]	110(80mA)		
VDD_W_CURR_MIN	3	R	[55:53]	110(60mA)		
VDD_W_CURR_MAX	3	R	[52:50]	110(80mA)		
C_SIZE_MULT	3	R	[49:47]	011	100	101
ERASE_BLK_EN (Note)	1	R	[46:46]	1		
SECTOR_SIZE	7	R	[45:39]	0011111		
WP_GRP_SIZE	7	R	[38:32]	0000000		
WP_GRP_ENABLE	1	R	[31:31]	0		
-	2	R	[30:29]	All '0'		
R2W_FACTOR	3	R	[28:26]	101		
WRITE_BL_LEN	4	R	[25:22]	1001		
WRITE_BL_PARTIAL	1	R	[21:21]	0		
-	5	R	[20:16]	All '0'		
FILE_FORMAT_GRP	1	R/W ⁽¹⁾	[15:15]	0		
COPY	1	R/W ⁽¹⁾	[14:14]	0		
PERM_WRITE_PROTECT	1	R/W ⁽¹⁾	[13:13]	0		
TMP_WRITE_PROTECT	1	R/W	[12:12]	0		
FILE_FORMAT	2	R/W ⁽¹⁾	[11:10]	00		
-	2	R/W	[9:8]	All '0'		
CRC	7	R/W	[7:1]	(CRC)		
-	1	-	[0:0]	1		

Cell Types: R: Read Only, R/W: Writable and Readable, R/W(1): One-time Writable / Readable

Note: Erase of one data block is not allowed in this card. This information is indicated by "ERASE_BLK_EN".

Host System should refer this value before one data block size erase.

• **CSD_STRUCTURE**

Version number of the related CSD structure.

Table 12-1: CSD_STRUCTURE

CSD_STRUCTURE	CSD_STRUCTURE VERSION	Valid for SD PHYSICAL LAYER SPECIFICATION Version
0	CSD Version 1.0	Version 1.0
1-3	Reserved	

→ Version 1.0 Compliant

• **TAAC**

Defines the asynchronous part of the data access time.

Table 12-2: TAAC Access Time Definition

TAAC bit	Code
2:0	Time Unit 0 = 1ns, 1 = 10ns, 2 = 100ns, 3 = 1 μ S, 4 = 10 μ S, 5 = 100 μ S, 6 = 1ms, y = 10ms
6:3	Time Value 0 = Reserved, 1 = 1.0, 2 = 1.2, 3 = 1.3, 4 = 1.5, 5 = 2.0, 6 = 2.5, 7 = 3.0, 8 = 3.5, 9 = 4.0, A = 4.5, B = 5.0, C = 5.5, D = 6.0, E = 7.0, F = 8.0
7	Reserved

→ 200 μ s

• **NSAC**

Defines the worst case for the clock dependent factor of the data access time.

Unit is 100 clock cycle.

Total access time equal TAAC plus NSAC, calculation with actual clock frequency.

This is average delay by the first clock out put for data block.

→ 0 clock Cycle

• **TRAN_SPEED**

The following table defines the maximum data transfer rate per one data line.

Table 12-3: Maximum Data Transfer Rate Definition

TRAN_SPEED bit	Code
2:0	Transfer Rate Unit 0 = 100kbit/s, 1 = 1Mbit/s, 2 = 10Mbit/s, 3 = 100Mbit/s, 4-7 = Reserved
6:3	Time Value 0 = Reserved, 1 = 1.0, 2 = 1.2, 3 = 1.3, 4 = 1.5, 5 = 2.0, 6 = 2.5, 7 = 3.0, 8 = 3.5, 9 = 4.0, A = 4.5, B = 5.0, C = 5.5, D = 6.0, E = 7.0, F = 8.0
7	Reserved

→ Trans Rate is 25Mbps

•CCC

The Card Class Command Register (CCC) defines which command classes are supported by this card.

Table12-4:Supported Card Command Classes

CCC bit	Supported Card command Class
0	Class 0
1	Class 1
...	
11	Class 11

→ Class 0,2,4,5,8, are supported

•READ_BL_LEN

The Maximum read data block length for reading is computed as $2^{\text{READ_BL_LEN}}$.
 READ_BL_LEN is always equal to WRITE_BL_LEN.

Table12-5:DATA Block Length

READ_BL_LEN	Block Length
0-8	Reserved
9	$2^9 = 512\text{Bytes}$
...	
11	$2^{11} = 2048\text{Bytes}$
12-15	Reserved

→512Bytes on this card

•READ_BL_PARTIAL (Always = 1)

This is always data "1" in SD Memory Card so it can be read by Byte unit for Block data.

→"1":This card can partially readable by Byte unit.

•WRITE_BLK_MISALIGN

Define whether the data block to be written by one command can be spread over more than one physical block of the Flash Memory Device.

Table 12-6:WRITE_BLK_MISALIGN

WRITE_BLK_MISALIGN	Across Block Boundaries Write
0	Not Allowed
1	Allowed

→"0":Not allowed on this card

•**READ_BLK_MISALIGN**

Define whether the data block to be read by one command can be spread over more than one physical block of the Flash Memory Device.

Table 12-7:READ_BLK_MISALIGN

READ_BLK_MISALIGN	Across Block Boundaries Read
0	Not Allowed
1	Allowed

→"0": Invalid on this card

•**DSR_IMP**

If set, a driver stage register (DSR) is implemented (supported).

Table 12-8 :DSR_IMP

DSR_IMP	DSR Type
0	DSR NOT Implemented
1	DSR Implemented

→"0": DSR NOT implemented

•**C_SIZE**

This parameter is used to compute the user's data card capacity(Not include the security area) as below.

Memory Capacity = BLOCKNR * BLOCK_LEN

BLOCKNR = (C_SIZE + 1) * MULT

MULT = 2^{C_SIZE_MULT+2} (C_SIZE_MULT < 8)

BLOCK_LEN = 2^{READ_BLK_LEN} (READ_BLK_LEN < 12)

Therefore the maximum capacity of the 64MB card is:

3624*32*512/1024/1024 = 56.625MB

→ The user's data card capacity is as below.

- 64MB : 56.625 MB
- 128MB : 115.5 MB
- 128MB : 233.25 MB

•**VDD_R_CURR_MIN,VDD_W_CURR_MIN**

The maximum values for Read/Write currents at VDD:MINIMUM.

Tab 12-9 VDD_R_CURR_MIN, VDD_W_CURR_MIN VDD_R_CURR_MIN VDD_W_CURR_MIN	Code for current consumption @ VDU
2:0	0 = 0.5mA, 1 = 1mA, 2 = 5mA, 3 = 10mA, 4 = 25mA, 5 = 35mA, 6 = 60mA, 7 = 100mA

→60mA@Vdd = 2.7 V (Minimum)

• **VDD_R_CURR_MAX, VDD_W_CURR_MAX**

The maximum values for Read/Write currents at VDD:MAXMUM.

Table 12-10:VDD_R_CURR_MAX,VDD_W_CURR_MAX

VDD_R_CURR_MAX VDD_W_CURR_MAX	R/W current Maximum
2:0	0 = 0.5mA, 1 = 5mA, 2 = 10mA, 3 = 25mA, 4 = 35mA, 5 = 45mA, 6 = 80mA, 7 = 200mA

→80mA @VDU = 3.3 V (Maximum) on this card

• **C_SIZE_MULT**

This parameter is used to compute the user's data card capacity not include the security protected are refer to C_SIZE.

Table 12-11:Multiply Factor for the Device Size

C_SIZE_MULT	MULT
0	$2^2 = 4$
1	$2^3 = 8$
2	$2^4 = 16$
3	$2^5 = 32$
4	$2^6 = 64$
5	$2^7 = 128$
6	$2^8 = 256$
7	$2^9 = 512$

→64 MB : $2^5 = 32$ is on this card

128MB : $2^6 = 64$ is on this card

256MB : $2^7 = 128$ is on this card

• **ERASE_BLK_EN**

(Caution!: This is different from MMC. Please be careful.)

WRITE_BL_LEN defines whether erase of one write block(see WRITE_BL_LEN) is allowed.

Table12-12:ERASE_BLK_EN

ERASE_BLK_EN	Description
0	Host cannot erase by WRITE_BL_LEN
1	Host can erase by WRITE_BL_LEN

→"1" : Can erase by WRITE_BL_LEN unit

So should be check this value, and recognize how to erase.

•SECTOR_SIZE

Sector defines the minimum erasable size. SECTOR_SIZE indicates the minimum erasable size as the number of write blocks.

→ 1 Sector-size = 32 Write Blocks on this card

•WP_GRP_SIZE

WP_GRP_SIZE defines the minimum number of sectors that can be set for the write protect group (WP_Group). A value of '0' means 1WP-Group = 1 erase sector,'127 means 1WP-Group = 128 sectors.

→"1" : 1WP-Group is one sector on this card

•WP_GRP_ENABLE

A value of "0" means not implemented (supported) the WP-Group functions.

Table12-13:WP_GRP_ENABLE

WP_GRP_ENABLE	Description
0	NOT Implemented
1	Implemented

→"0": WP Group is not Implemented on this card

•R2W_FACTOR

That is calculated R2W_FACTOR defines a multiple number for typical write time as a multiple of the read access time.

Table12-14:R2W_FACTOR

R2W_FACTOR	Multiples of read Access Time
0	1
1	2(Write half as fast as read)
2	4
3	8
4	16
5	32
6,7	Reserved

→"5": Typical write time = Read Access time x 32 on this card

•WRITE_BL_LEN

The maximum write block length is calculated as $2^{\text{WRITE_BL_LEN}}$.

Table12-15:DATA Block Length

WRITE_BL_LEN	Block Length
0-8	Reserved
9	$2^9 = 512\text{Bytes}$
...	
11	$2^{11} = 2048\text{Bytes}$
12-15	Reserved

→"9": 512Bytes on this card

•WRITE_BL_PARTIAL

WRITE_BL_LEN defines whether partial block write is available.

Table12-16:Write Data size

WRITE_BL_PARTIAL	Block Oriented write Data size
0	Only the WRITE_BL_LEN size or 512Bytes are available
1	Partial size (Minimum 1Byte) write available

→"0": Partial size write is not available on this card

•FILE_FORMAT_GRP/FILE_FORMAT

Indicates the selected group of file format group and file format.

Table12-17:File Format

FILE_FORMAT_GRP	FILE_FORMAT	Kinds
0	0	Hard disk-like File system with partition table
0	1	DOS FAT (floppy-like) with boot sector only (No partition table)
0	2	Universal File Format
0	3	Others/Unknown
1	0,1,2,3	Reserved

Further information is given in SD Memory Card FILE SYSTEM SPECIFICATION.

→ [0.0]: Hard disk-like file system with partition table on this card

•COPY

Defines the contents of this card is original (=0) or duplicated (1).
This bit is one time programmable.

Table12-18: COPY

COPY	Description
0	Original
1	Copy

→"0": Original on this card

•PERM_WRITE_PROTECT

Permanently protects the whole card content against write or erase.
This bit is one time programmable.

Table12-19: PERM_WRITE_PROTECT

PERM_WRITE_PROTECT	Description
0	Not protected/Writable
1	Permanently Write protected

→"0": Not Protected/Writable on this card

•TMP_WRITE_PROTECT

Temporarily protects the whole card content against write or erase.

Table12-20: TMP_WRITE_PROTECT

TMP_WRITE_PROTECT	Description
0	Not protected/Writable
1	Temporarily Write Erase protected

→"0": Not Protected/Writable on this card

•CRC

Calculated CRC for default data is set here.
Host System is responsible to re-calculate this CRC if any CSD contents are changed.

7.2.4. RCA Register

The writable 16bit relative card address register carries the card address in SD Card mode.

7.2.5. DSR Register

This register is not implemented on this card

7.2.6. SCR Register

SCR (SD Card Configuration Register) provides information on SD Memory Card's special features. The size of SCR Register is 64 bit.

Table13: SCR Register

Field	Width	Cell Type	SCR Slice	Value		
				64MB	128MB	256MB
SCR_STRUCTURE	4	R	[63:60]	0000		
SD_SPEC	4	R	[59:56]	0000		
DATA_STAT_A FTER_ERASE	1	R	[55:55]	1		
SD_SECURITY	3	R	[54:52]	010		
SD_BUS_WIDT HS	4	R	[51:48]	0101		
-	16	R	[47:32]	All '0'		
-	32	R	[31:0]	All '0'		

•SCR_STRUCTURE

Version number of the related structure in the SD Card PHYSICAL LAYER SPECIFICATION.

Table13-1: SCR_STRUCTURE

SCR_STRUCTURE	SCR STRUCTURE VERSION	Valid for SD PHYSICAL LAYER SPECIFICATION
0	SCR Version 1.0	Version 1.0
1-15	Reserved	

→"0": Version 1.0 Compliant on this card

•SD_SPEC

Describes the SD PHYSICAL LAYER SPECIFICATION version supported by this card.

Table13-2: SD_SPEC

SD_SPEC	SD PHYSICAL LAYER SPECIFICATION Version
0	Version 1.0
1-15	Reserved

→"0" = Version 1.0 Compliant on this card

•DATA_STAT_AFTER_ERASE

This indicates the block “0” or “1” after erase operation.

→“1” on this card

•SD_SECURITY

Describe the security algorithm supported by the Card.

Table13-3: Supported Security Algorithm

SD_SECURITY	Supported algorithm
0	No Security
1	Security Protocol 1.0
2	Security Protocol 2.0
3-7	Reserved

Security protocol 1.0: n Bus encryption

→“2”: Security Protocol 2.0 on this card

•SD_BUS_WIDTHS

Indicates the DAT bus width that a supported by this card.

Table 13-4:Supported Bus Widths

SD_BUS_WIDTHS	Supported BUS width
0 bit position	1 bit(DAT0)
1 st bit position	Reserved
2 nd bit position	4 bit(DAT0-3)
3 rd bit position	Reserved

→“0101”: 1 and 4 bit supported.

7.2.7. SD Status

Table14:SD Status

Identifier	Width	Type	SD Status Slice	Value		
				64MB	128MB	256MB
DAT_BUS_WIDTH	2	SR	[511:510]	00		
SECURED_MODE	1	SR	[509]	0		
-	13	-	[508:496]	All '0'		
SD_CARD_TYPE	16	SR	[495:480]	0x0000		
SIZE_OF_PROTECTED AREA	32	SR	[479:448]	0x28	0x28	0x28
-	136	-	[447:312]	All '0'		
-	312	-	[311:0]	All '0'		

S: Status bit

R: Set based on Command Response

•DAT_BUS_WIDTH

Indicate the currently defined data bus width that was defined by SET_BUS_WIDTH command.

Table14-1:DAT_BUS_WIDTH

DAT_BUS_WIDTH	Bus Width
'00'	1 bit(default)
'01'	Reserved
'10'	4 bit width
'11'	Reserved

•SECURED_MODE

Indicates whether card is in secure mode operation.

Table14-2:SECURED_MODE

SECURED_MODE	Secured Mode Status
'0'	NOT Secured Mode
'1'	Secured Mode

•SD_CARD_TYPE

SD Card type described here.(Various SD types to be defined in the future.)

Table14-3:SD_CARD_TYPE

SD_CARD_TYPE	SD Card Type
'0000'h	SD Memory Card

•SIZE_OF_PROTECTED_AREA

Show the size of protected area.

The actual area = (SIZE_OF_PROTECTED_AREA) * MULT * BLOCK_LEN

→ Protected Area depends on the Memory Types as below.

64MB : 640KB

128MB : 1280KB

256MB : 2560KB

7.3. Logical Format

Toshiba SD card is formatted before shipping compliant to the SD Card FILE SYSTEM SPECIFICATION.

Following parameters may be changed if the host system is not compliant with the SD Card Format Specification.

The logical format parameters are described in the Table 15,16,17,18 .

The data of the logical format is described in Appendix 3-1,3-2,3-3,3-5.

7.3.1. SD card Capacities

Table 15: SD Card capacities

Item	Card Capacities					
	64MB		128MB		256MB	
	Sector	KB	Sector	KB	Sector	KB
Hole Capacity	117, 248	58, 624	239, 104	119, 552	482, 816	241, 408
User Data Area Size	115, 968	57, 984	236, 544	118, 272	477, 696	238, 848
Protected Area Size	1, 280	640	2, 560	1, 280	5, 120	2, 560

7.3.2.SD card System information

Table.16: SD card System information

Item		Card Capacities		
		64MB	128MB	256MB
User Data Area	Data Boundary unit size (KB)	16	32	32
	Cluster Size (KB)	16		
Protected Area	Data Boundary unit size (KB)	1	4	4
	Cluster Size (KB)	1	4	4

7.3.3.MBR, Boot Sector parameters

Table 17: Master Boot Record a Partition Table

BP	Data Length	Field Name	Contents		
			64MB	128MB	256MB
0	446	Master Boot Record	All 0x00		
446	16	Partition Table(partition1)	Refer Table 18		
462	16	Partition Table(partition2)	All 0x00		
478	16	Partition Table(partition3)	All 0x00		
494	16	Partition Table(partition4)	All 0x00		
510	2	Signature Word	0x55(BP510),0xAA(BP511)		

Table 18: Partition Table

BP	Data Length	Field Name	Contents		
			64MB	128MB	256MB
0	1	Boot Indicator	0x00		
1	1	Starting Head	1	3	3
2	2	Starting Sector/Starting Cylinder	8/0	2/0	4/0
4	1	System ID	0x06	0x06	0x06
5	1	Ending Head	7	7	15
6	2	Ending Sector/Ending Cylinder	32/453	32/924	32/933
8	4	Relative Sector	39	97	99
12	4	Total Sector	115,929	236,447	477,597



Table.19: Extended FDC Descriptor

BP	Data Length	Field Name	Contents		
			64MB	128MB	256MB
0	3	Jump Command	0xEB(BP0),0x00(BP1),0x90(BP2)		
3	8	Creating System Identifier	(Card Specific 8Byte-Data)		
11	2	Sector Size	512		
13	1	Sectors per Cluster	32		
14	2	Reserved Sector Count	1		
16	1	Number of FATs	2		
17	2	Number of Root-directory Entries	512		
19	2	Total Sectors	0	0	0
21	1	Medium Identifier	0xF8		
22	2	Sectors per FAT	12	31	62
24	2	Sectors per Track	32		
26	2	Number of Sides	8		16
28	4	Number of Hidden Sectors	39	97	99
32	4	Total Sectors	115,929	236,447	447,596
36	1	Physical Disk Number	0x80		
37	1	Reserved	0x00		
38	1	Extended Boot Record Signature	0x29		
39	4	Volume ID Number	(Card Specific 4Byte Data)		
43	11	Volume Label	"NO NAME "		
54	8	File System Type	"FAT12 "	"FAT16 "	
62	448	(Reserved for system use)	All 0x00		
510	2	Signature Word	0x55(BP510),0xAA(BP511)		

7.3.4 FAT

FAT1 and FAT2 are consisted with the same data.

64MB: FAT12, 128MB/256MB: FAT16 .

Table.20: FAT

BP	64MB	128MB	256MB
	FAT12	FAT16	
0	0xF8		
1	0xFF		
2	0xFF		
3	0x00	0xFF	
4	0x00		
5	0x00		
....	0x00		
End	0x00		

7.3.5. Root Directory Entries

Initial values are All "0x00" .

7.3.6. User Data Area

Initial values are All "0xFF".

8.Others: Limited Conditions, SD Specification Compliance

1) Non Supported Registers:

DSR Register (Optional register : PHYSICAL LAYER SPECIFICATION 5.6)

2)Non Supported Functions:

Programmable Card Output Driver(Optional in PHYSICAL LAYER SPECIFICATION 6.5)

Card 's Internal Write Protect (Optional in PHYSICAL LAYER SPECIFICATION 4.3.5.)

Card Lock, Unlock Function (Optional in PHYSICAL LAYER SPECIFICATION 4.3.6.)

3) Non Specified Command:

CMD4 SET_DSR

CMD56 GEN_CMD

9.Host System Design Guidelines

The purpose of this guideline is a reference to help the design of the SD Memory Card interface of the Host system.

The description here does not make any warranty fitness for particular host.

The implementations of the host systems are different in each system.

Please design the SD Memory Card Host systems considering the each condition.

Mandate: Mandate requirement to the Host implementation

Recommendation: Recommended Implementation, Just General Example

9.1.Retry after Memory write (Mandate)

Please issue the ACMD22 and check written blocks if it occurs error by checking the written blocks after Memory write. (CMD25: WRITE_MULTIPLE_BLOCK)

Please retry CMD25 blocks if written blocks is different from your expectation.

Background

The Flash Memory used in this card has possibility of Memory Write (Program) Error.

If the Memory Write Error occurs in some memory page, the Write error may impacts other pages in the same block.

9.2.SPI-Mode initialization (Mandate)

SD Card shall be initialized by ACMD41. Do NOT use CMD1 for SPI-Mode initialization.

9.3.SPI-Mode RSV pin Pull up(Mandate)

RSV(#8,#9 in SPI Mode) shall be pulled up by 10-100k-ohm resistors.

(See 6.1. SD Card Pins)

9.4.Prohibition during Write (Mandate)

Do not turn off the power or remove the SD Memory Card from the slot before read/write/ mutual authentication operation is complete. Avoid using the SD Memory Card when the battery is low. Power shortage, power failure and/or removal of the SD Memory Card from the slot before read/write/mutual authentication operation is complete will cause malfunction of the SD Memory Card, loss of data and/or damage to data.

Please comment and inform this prohibition to the end users in proper way. (Manual or Instructions)

9.5.Process after Timeout in case of Read or Write (Recommendation)

If there are no-response after the timeout passed in case of read or write (Recommendation), please issue the CMD12(Stop Transmission) and stop the data transfer to prevent the host stuck on waiting for the response.

(Reference :7.3.3. Data Token, 7.3.4.Data Error Token of SD PHYSICAL LAYER SPECIFICATION.)

In case of SPI mode, there are some restrictions regarding to access the out of range boundary.

1) Response error (*1) will be occurred when host issue CMD12 over the out of range boundary under WRITE_MULTIPLE (CMD25, ACMD25) action.

Host should neglect CMD12 error status.

2) This maybe occurred when SD CLK is low frequency.

In case of out of range token maybe duplicated, please check case (a) and case (b) when issue CMD12 after reading before the boundary using READ_MULTIPLE (CMD18, ACMD18).

(a) Response error maybe occurred (*1)

(b) Response of CMD12 maybe not issued.

- Re-issue CMD12, then next command can be received
- Neglect the response of re-issue CMD12

*1: Response Error Descriptions

➤ If CRC Check is On.

Com CRC Error is responded.

➤ If CRC Check is Off.

In case of 1) above, R1=0x44(Parameter Error & Illegal Command) .

In case of 2) above, R1=0x44(Illegal Command) .

9.6.Host Timeout Setup (Recommendation)

The timeout value is recommended as below. (Table. 21.)

The memory Erase function requires the longest time before the Card Response.

The erase time for Memory Block is also included for the Timeout value in the Data erase operation in the SD Memory Card. (Table. 22)

The Host system should chose the appropriate block size considering the erase time.

Table21:Recommended Time out value

Condition	Recommended Value (Max.)
Waiting for the CMD Response	64cycles
Read Data output after issue the Commands	100ms
Busy Status Change	1s

Table22:Erase time reference value

64MB	The Host system should chose the appropriate block size considering the erase time.
128MB	
256MB	

NOTE: The Value in this table is Reference for setting the timeout value.

9.7. SD Command (Mandate)

1)CMD0 continuously issue

Do NOT continue the CMD0 with 1Pin(CD/DAT3)='Low' just after CMD0 or the SD Card initialized in SPI mode.

In case of 1 pin (CD/DAT3)="Low", it means SPI mode so be careful to the duration of CMD0 issue.

Please choose the appropriate timing interval for CMD0 to prevent this problem.

The interval is related with the pull up Resistor value. of the host side.

2)After the Security Read Command

Please issue the CMD13 to ensure the status change to the transmission state or wait more than 100 us, after issue the ACMD18 or ACMD43.

9.8. Pull Up resistors (Recommendation)

CMD and DAT [2:0] can pull up with 10-100k ohm resistors by the host side.

DAT3 can pull up with 10-90 k ohm resistor by the host side.

Please disable the Card-Internal pull up on CD by ACMD42 before access. (Refer Fig. 7)

The pull up resistor value on WP switch can be calculated by host buffer characteristics.

9.9. Write/ Erase Size management: (Recommendation)

1)Erase Unit

The erase size is recommended to using Boundary unit indicated by Erase Sector size below.

The erase unit size is given as below.

$$\text{Erase Sector Size} = \text{Block_length} \times (\text{SECTOR_SIZE}) = 512 \text{ Byte} \times 32\text{-block} = 16\text{K Byte}$$

(Block_length can calculate from WRITE_BL_LEN)

2)Faster Write

Multiple block write by command :WRITE_MULTIPLE(CMD25,ACMD25) allows faster data write.

TENTATIVE

Appendix 2-5: initial value of SD Status

64MB

Field	DA	SRSV	SD_CARD_TYPE	SIZE_OF_PROTECTED_AREA	RSV
Bit Position	5	5	5	5	5
2進数表示	1	0	0	0	0
Hexadecimal	0	0	0	0	0

128MB

Field	DA	SRSV	SD_CARD_TYPE	SIZE_OF_PROTECTED_AREA	RSV
Bit Position	5	5	5	5	5
2進数表示	1	0	0	0	0
Hexadecimal	0	0	0	0	0

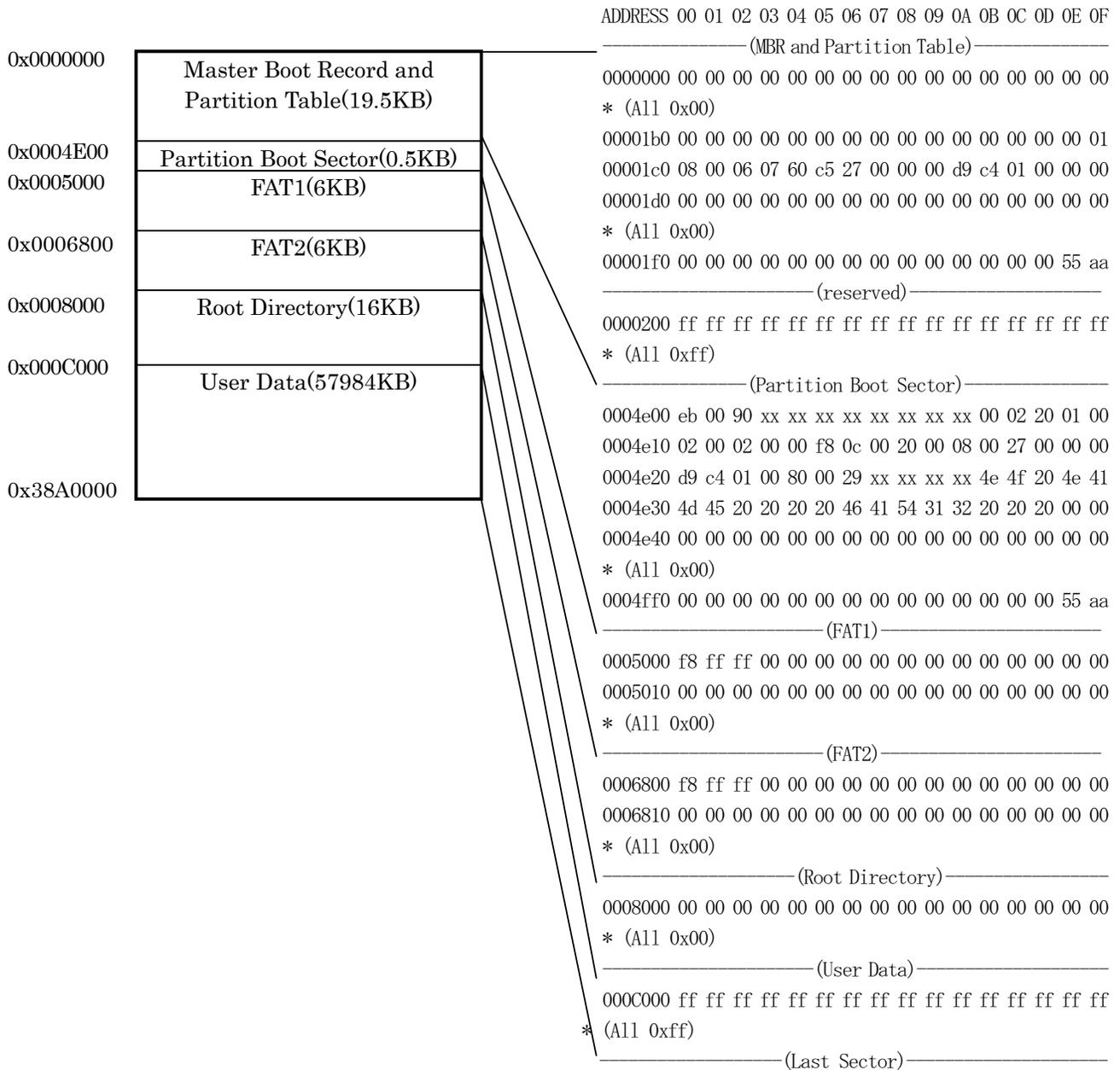
256MB

Field	DA	SRSV	SD_CARD_TYPE	SIZE_OF_PROTECTED_AREA	RSV
Bit Position	5	5	5	5	5
2進数表示	1	0	0	0	0
Hexadecimal	0	0	0	0	0

Appendix 3-1 : Memory Map and Dump Data of User Data Area

Last address of this memory map indicates “actual last address + 1”.

(1)64MB Card

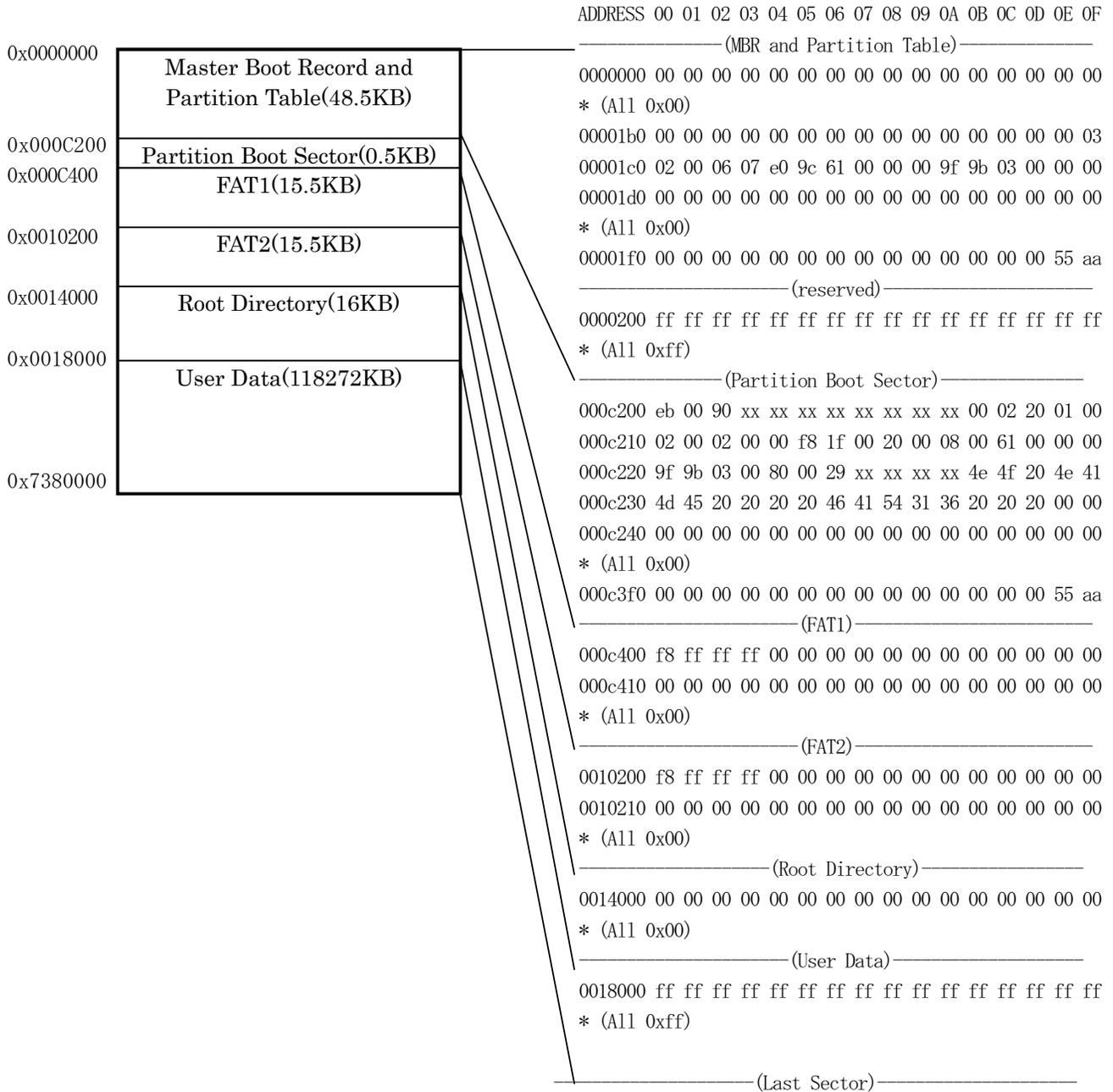


“xx” depends on SD card.

Appendix 3-2 : Memory Map and Dump Data of User Data Area

Last address of this memory map indicates “actual last address + 1”.

(2)128MB Card

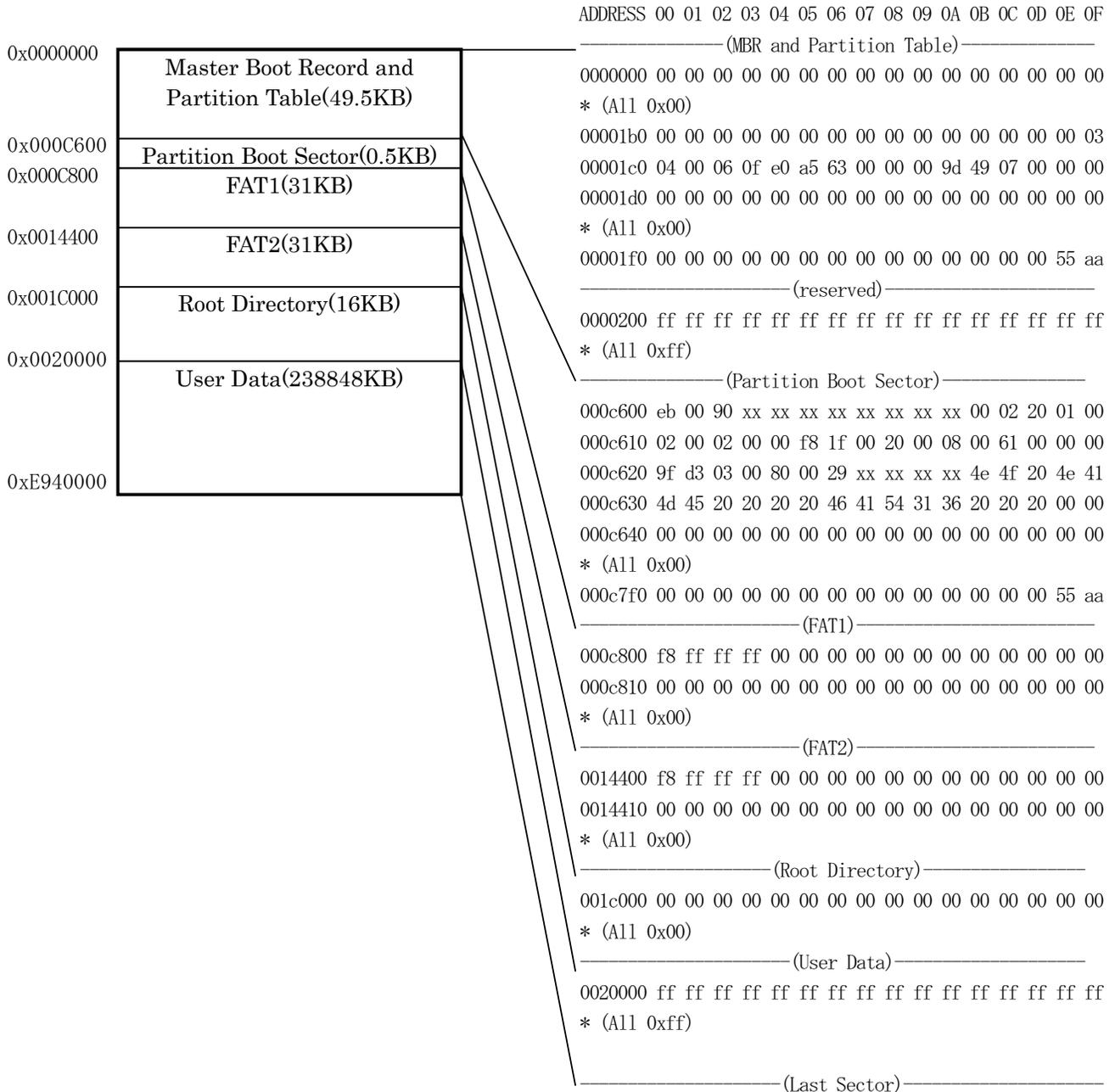


“xx” depends on SD card.

Appendix3-3 : Memory Map and Dump Data of User Data Area

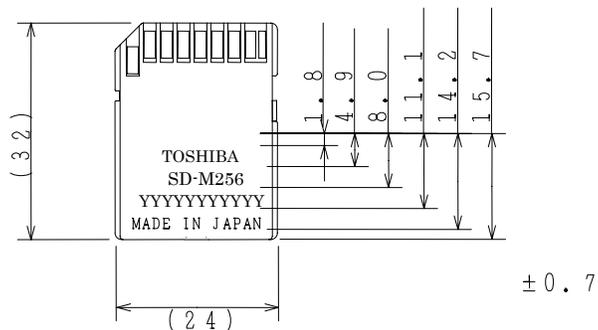
Last address of this memory map indicates “actual last address + 1”.

(3)256MB Card



“xx” depends on SD card.

Appendix4-1 : Laser marking



1 LINE : SPACE

2 LINE : TOSHIBA

3 LINE :

CAPACITY	MODEL NAME	LASER MARKING
256MB	SD-M2564B1	SD-M256

4 LINE : LOT NUMBER
11LETTERS

5 LINE : MADE IN JAPAN

Appendix4-2 : For Instruction Manual

Please comment and inform this prohibition to the end users in proper way. (Manual or Instructions).

Notes on usage

- (1)The SD memory card includes a built-in non-volatile semiconductor memory (NAND type Flash EEPROM). Under normal circumstances data stored on the SD memory card cannot be corrupted or lost. If the card is used in ways other than described in these instruction manual, however, data could be corrupted or lost. Please note that **** Corporation accepts no responsibility for corruption or loss of data stored on the SD memory card, regardless of the type or cause of the problem or damage.
- (2)The SD memory card is a storage medium that conforms to SDMI (Secure Digital Music Initiative) standards for protecting the rights of copyright holders. Based on SD memory card specifications, part of the memory is used as the system area, so the actually usable memory capacity is lower than the indicated capacity.
- (3)The SD memory card is already formatted. If you should want to reformat it, however, do so on a device including the SD logo mark and equipped with an SD memory card formatting function. Formatting the SD memory card on other devices (computers, etc.) may result in problems, such as the inability to read or write data.
- (4)Routine performance of backing-up data is strongly recommended.

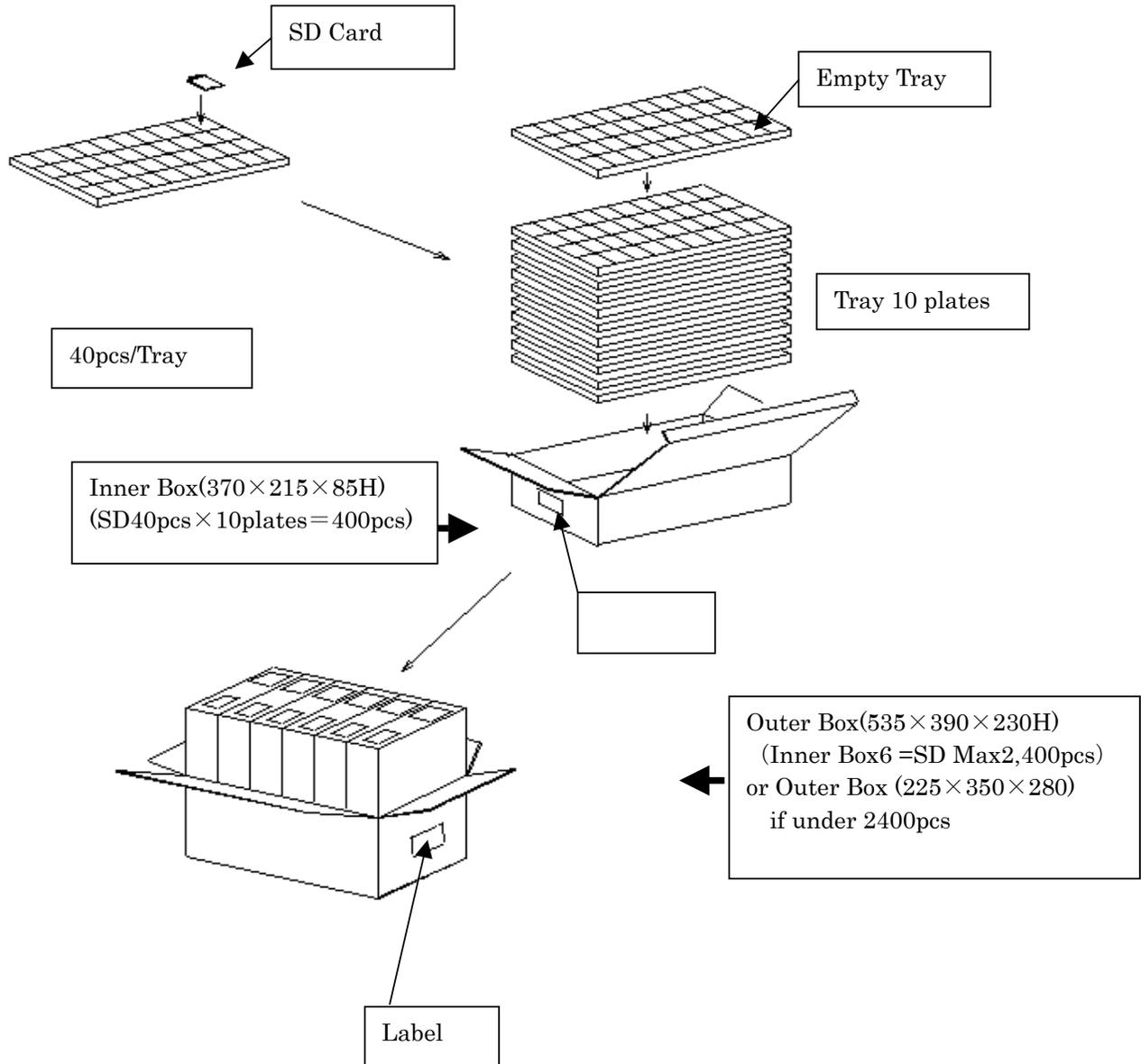
Exemption Clauses

- (1)**** Corporation bears no responsibility in the case of damages arising from earthquakes, fire not liable to Toshiba Corporation, operation by third parties, other accidents, or use under abnormal conditions including erroneous or improper operation and other problems.
- (2)****Corporation bears no responsibility for incidental damages (lost profit, work interruption, corruption or loss of the memory contents, etc.) arising from the use of or the inability to use this unit.
- (3)**** Corporation accepts no liability whatsoever for any damages arising from not having followed the descriptions in this Instruction Manual.
- (4)**** Corporation accepts no liability whatsoever for any damages arising from malfunctions arising from combination with equipment or software that is not related to **** Corporation.

Cautions

- (1)Keep out of reach of small children.
- (2)Do not touch or have metal objects touch the terminals or connectors. Static electricity may cause malfunction, and/or loss of data.
- (3)Do not bend or force the SD Card into the slot. Do not drop the SD Card onto hard surface. Doing so may cause malfunction, and/or loss of data.
- (4)Do not disassemble, transform and/or alter the SD Card.
- (5)Keep away from dampness.
- (6)Do not turn off the power or remove the SD Memory Card from the slot before read/write operation is complete. Avoid using the SD Memory Card when the battery is low. Power shortage, power failure and/or removal of the SD Memory Card from the slot before read/write operation is complete will cause malfunction of the SD Memory Card, loss of data and/or damage to data.
- (7)The SD Memory Card is already formatted. However, if you should want to reformat it, make a back-up copy of the data stored on the SD Card prior to reformatting. **WARNING:** Reformatting clears all the data on the SD Card.

Appendix5-1 : Package



Appendix5-2 : LABEL DETAIL (400pcs BOX、 2,400pcs BOX)

MODEL NAME : SD-M2564B1 2002/30WEEK 2400pcs

TYPE	SD-M2564B1		
ADD.C		Q'TY	2400PCS
NOTE	0230KAZ - 2400		
TD0001			

Week CODE+ 3 LETTERS+ Q'TY

Key No

*Y20+*****



TOSHIBA



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more than 3mm SPACE
at right and left

1) Model Name, Production Code

Model Name	Production Code	Capacity
SD-M2564B1	20533815	128MB

2) LOT

For the control of production or shipment
Different by production and shipment

3) Quantity

* Inner Box

Max 400pcs
(including dummy tray according to circumstances)

* Outer Box

Max 2,400pcs
(including empty box or buffer materials according to circumstances)