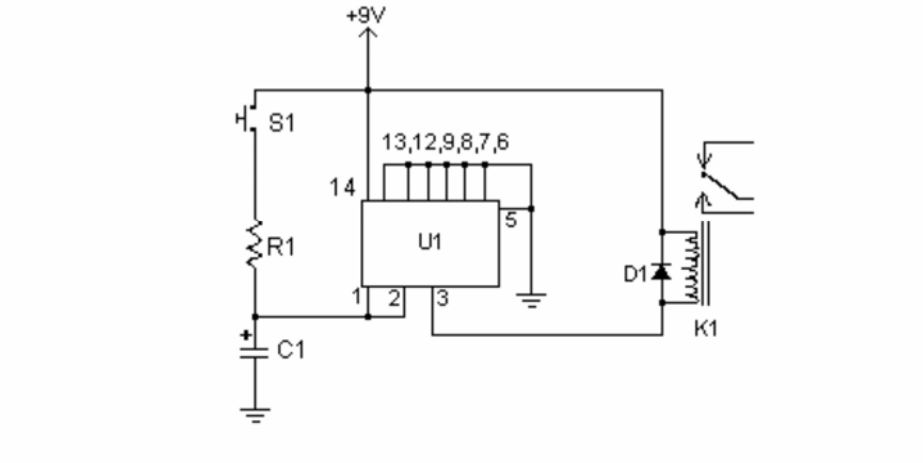
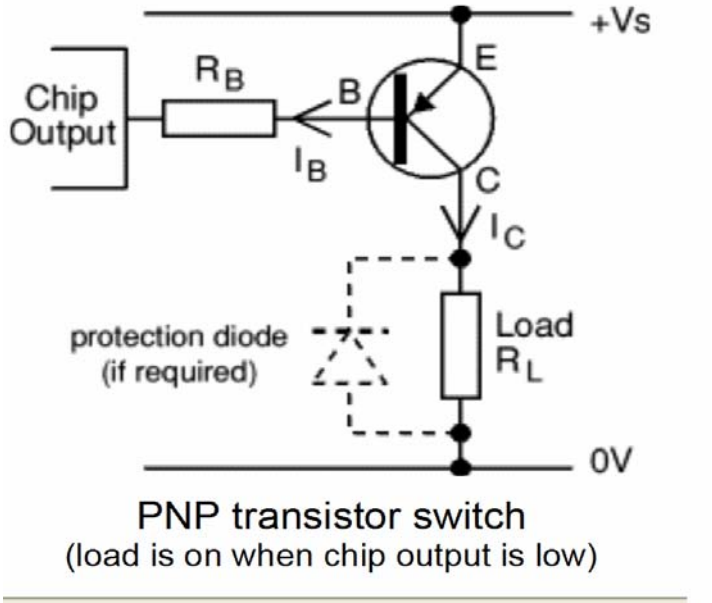
DELAYED TURN ON RELAY FOR CONTROLL UNIT



U1 =4001/4011

When activated by pressing a button, this time delay relay will activate a load after a specified amount of time. This time is adjustable to whatever you want simply by changing the value of a resistor and/or capacitor. The current capacity of the circuit is only limited by what kind of relay you decide to use..you can use any PNP transistor with out from pin 3or



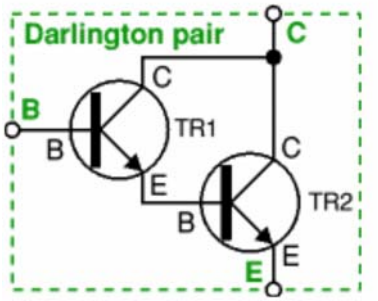
Darlington pair(after one more inversion using any of the free gate in same ic,I used pin 5&6 and out from pin 4) to drive practically any relay using the out from pin 4 of 4011/4001.

To calculate the time delay, use the equation R1 * C1 * 0.85=T, where R1 is the value of R1 in Ohms, C1 is the value of C1 in uF, and T is the time delay in seconds.

D1 =1N4007 or equivalent diodes to protect transistors from back emf in relay coil.

Darlington pair

This is two transistors connected together so that the amplified current from the first is amplified further by the second transistor. This gives the Darlington pair a very high current gain such as 10000. Darlington pairs are sold as complete packages containing the two transistors. They have three leads (B , C and E) which are equivalent to the leads of a standard individual transistor. You can make up your own Darlington pair from two transistors. For example: For TR1 use BC548B with h FE1 = 220. For TR2 use BC639 with h FE2 = 40. The overall gain of this pair is h FE1 × h FE2 = 220 × 40 = 8800. The pair's maximum collector current I



(max) is the same as TR2.

INPUT TO LOGIC GATES FROM SENSOR PROBES

The input to logic gate are either from a float switch or as in my use through conducting probes. The signal from probes(positive voltage from power supply unit of the circuit approximately 9 volt) is fed through the digital amplifier(common collector).to CMOS IN4011/4001 inputs. In figure 2 input from probes is fed through RS (150kohm trim pot to increase or decrease sensitivity).Rl can be avoided. Vout fed into CMOS input.

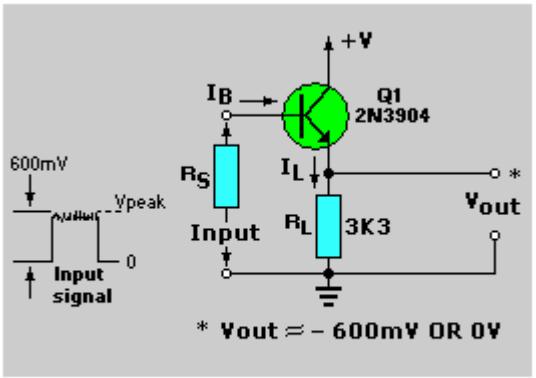
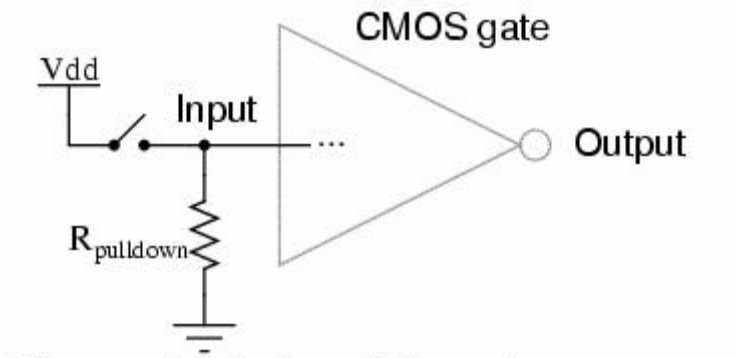


Fig. 2 -- Common-Collector digital amplifier.

The input to logic gates should never be left floating they should be pulled down (for my circuit as I am using Vdd as sensing current) using resistors as shown below . This resistor's value is not critical: 10 kΩ is usually sufficient.



When switch is closed, the gate sees a definite "high" (1) input. When the switch is open, $R_{pulldown}$ will provide the connection to ground needed to secure a reliable "low" logic level for the CMOS gate input.