Ultralow Power, Fully Autonomous Boost Rectifier for Electromagnetic Energy Harvesters

Gyorgy D. Szarka, Stephen G. Burrow, and Bernard H. Stark

***Abstract*—In this paper, a complete power conditioning system for a vibration energy harvester is presented that operates at ultralow power levels. The power conditioning system, implemented with discrete components, is self-starting and fully autonomous, and based upon a full-wave boost rectifier topology. The design utilizes the stray inductance of the harvester's coil, eliminating the need for separate inductors, and employs open-loop control that reduces the quiescent power overhead to just 21 μW, while still extracting 84% of the maximum available power from the harvester. The design of the subsystems, including self-start circuitry, is described in detail, and it is shown that careful active device selection is required to minimize losses. It is experimentally demonstrated that the power converter achieves conversion efficiencies of up to 76% at submilliwatt power levels, including quiescent losses. The overall system efficiency peaks at 65% at 0.9 mW, while still achieving 51% at 200 μW. The ability of this system to operate efficiently at ultralow average power levels opens up new possibilities to further miniaturize vibration harvesters and deploy them into environments with lower vibration levels than is currently possible.**

***Index Terms*—AC–DC power converters, boost converter, energy harvesting, low-power electronics, rectifiers.**

I. Introduction

SMALL-SCALE electromagnetic vibration energy harvesters generate alternating currents at low voltages: typically below 1 V [1]. Rectification and voltage level boosting are required to meet the power supply requirements of typical electronic circuits, while the load seen by the harvester must also be controlled to maximize the harvested power.

Although the power generated by a particular harvester is highly application dependent, it is common for the power output to be roughly constant over time. Many low-power loads, by contrast, exploit burst operation and sleep modes, yielding exceedingly low average power consumption but with short duration high power demands. An extra challenge for the power conditioning system is thus to match the steady power output of the harvester to the power of a load with high peak-to-mean demand.

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Most published power electronics topologies [2] for interfacing with electromagnetic energy harvesters are based on two stages: a rectification stage followed by a dc–dc power converter architecture [3]–[5]. More recently, single-stage ac–dc power converters [6], [7] have been reported in the literature that can overcome some of the challenges associated with passive rectifier topologies [8]. Using single-stage boost rectifiers, the inductance is on the ac side, which allows the inductance to be formed by the parasitic stray inductance of the coil windings in electromagnetic generator systems. This is common practice in high-power drives, and has also been proven to be feasible in low-power energy harvesting systems at milliwatt [9], and at hundred microwatt [10] power levels. A comprehensive overview of boost rectifier topologies can be found in [11].

In a recent review paper by the authors [2], it was ascertained that many of the published low-power conditioning circuits for electromagnetic energy harvesters operate at power levels of several milliwatts and up and achieve efficiencies in the region of 60% [7]. By contrast, many papers report small-scale ($<$10 cm^3) harvesters with output powers in the region of 0.3–200 μW [1], [12]. Addressing this disparity by designing power conditioning circuits that can operate at the low power levels of practical energy harvesting devices is a significant research challenge. Some authors have produced designs for subsystems that can operate efficiently at very low powers, e.g., in [13] an integrated switched-capacitor dc–dc converter that operates down to 40 μW generated power at 0.8 V_{pk} is described.

In this paper, the design and discrete implementation of a fully autonomous power conditioning system based on a nonsynchronous full-wave boost rectifier topology is presented. The power conditioning is capable of self-start, extracts energy efficiently from a microscale generator source producing less than 0.5 V_{pk} output at 135 μW, and can satisfy the power demand of load electronics that draws short pulses in excess of 40 mW. In order to constrain the design of the power conditioning system to within realistic bounds, an energy harvester and load electronics have been realized; these are described in Section II. Section III describes the detailed design and operation of the boost rectifier; Section IV presents the implementation of the self-powered gate drive circuitry; Section V introduces key design concepts associated with the passive self-start circuit; Section VI presents experimental results, and discusses the findings. Finally, the paper concludes with a review of the main achievements.

II. Power Conditioning System Overview

A. Architecture and Power Definitions

The system architecture is shown in Fig. 1. The main power system consists of a boost rectifier feeding a supercapacitor

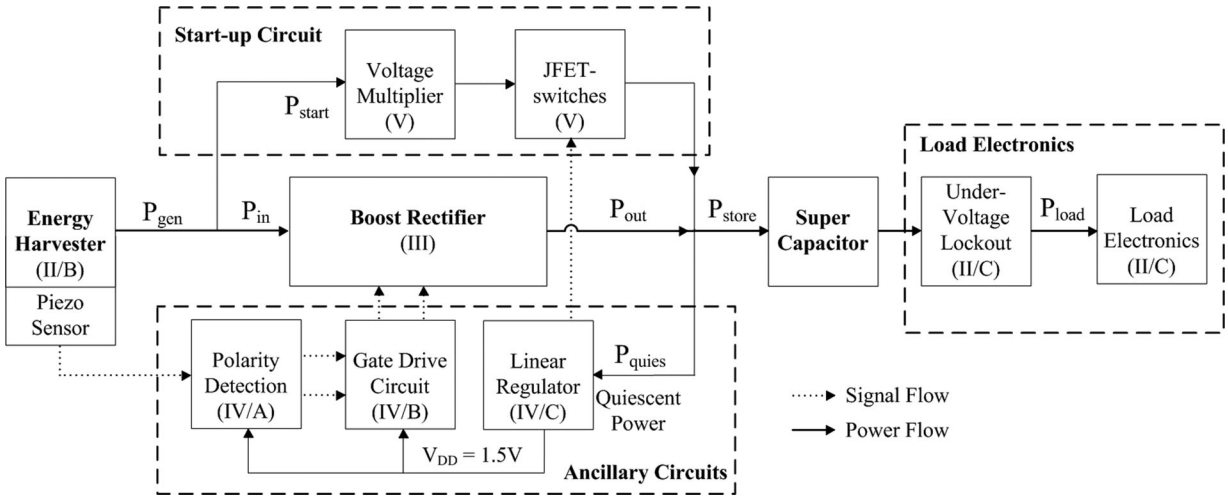


Fig. 1. System block diagram illustrating the main circuit blocks of the power conditioning system and their connections. The relevant section describing a particular system block is indicated under the block titles.

energy storage element. The load is connected via an undervoltage lockout (UVLO) circuit. A passive voltage multiplier (VM) provides start-up. Ancillary circuits are designed to generate the gate driving signals for the active switches of the boost rectifier. The system is designed such that the voltage across the supercapacitor varies within the allowable operating voltage range of the load.

The minimum operating power (MOP) of the system is equal to the maximum of the combined losses within the system over the operating conditions. For a generator that produces $P_{\max}$ at optimum load conditions, the overall power balance is given as

$$P_{\text{store}} = \eta_{\text{con}} \cdot (\eta_{\text{uti}} \cdot P_{\max} - P_{\text{start}}) - P_{\text{quies}} + P_{\text{leak}} \quad (1)$$

where η_{uti} is the utilization factor, defined as

$$\eta_{\text{uti}} = \frac{P_{\text{gen}}}{P_{\max}} \quad (2)$$

and η_{con} is the conversion efficiency

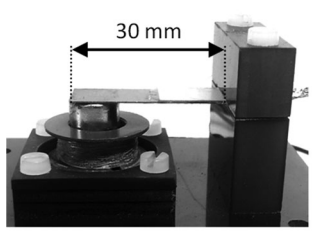
$$\eta_{\text{con}} = \frac{P_{\text{out}}}{P_{\text{in}}}. \quad (3)$$

The overall system efficiency is derived as

$$\eta_{\text{overall}} = \frac{P_{\text{store}}}{P_{\max}}. \quad (4)$$

B. Energy Harvester

Approximating the output of a resonant harvester with a voltage or current source neglects dynamic effects and thus it is important to test the power conditioning system with a real harvester. To this end, a moving magnet harvester embodying many of the characteristics common to small harvesters has been used to constrain the design and test the power conditioning system (see Fig. 2). A NdFeB magnet of 3.4 g is attached to a compliant BeCu beam, resonating at an arbitrary 44 Hz. A coil of copper wire wound on a plastic former completes the transduction mechanism. A piezoelectric element is bonded to the beam and this produces an output voltage proportional to displacement



Damping Coefficient, c_m	0.018 N·s·m^{-1}
Coupling, θ	2.4 V·s·m^{-1}
Spring Constant, k	257.5 N·m^{-1}
Mass, m	3.4 g
Coil Inductance	5.35 mH
Coil Resistance	80 Ω

Fig. 2. Photograph of the energy harvester used as a test source for the power conditioning system, along with lumped-element equivalent parameters (measured). Piezoelectric film used for displacement monitoring can be seen bonded to the top surface of the cantilever beam. The coil is wound using 600 turns of 100 μm copper wire.

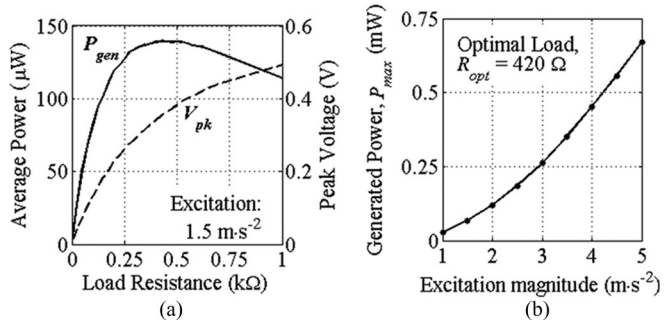


Fig. 3. (a) Measured generated power and voltage versus load resistance of the electromagnetic energy harvester at its resonance frequency of 44 Hz at an excitation magnitude of 1.5 m·s^{-2}. (b) Measured maximum generated power under optimum resistive ac load against excitation magnitude.

that is used to commutate switching in the power converter. The mechanical parameters of the generator are given in Fig. 2.

Fig. 3(a) shows measured output power and voltage against load resistance, and b) shows the maximum power at various levels of excitation. At 44 Hz, the coil impedance is dominated by its resistance and therefore the values of power in Fig. 3 can be considered the maximum possible power that can be extracted with any load and are used in this paper to determine the utilization η_{uti}.

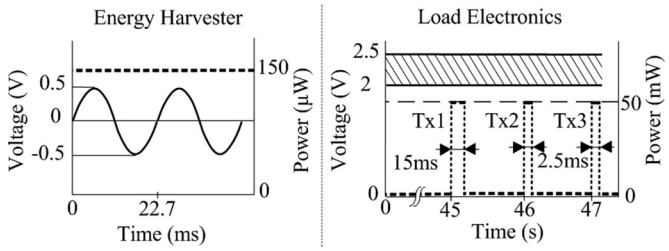


Fig. 4. Conceptual diagram to illustrate the comparison of the harvester voltage and power profiles with those of the wireless sensor load electronics.

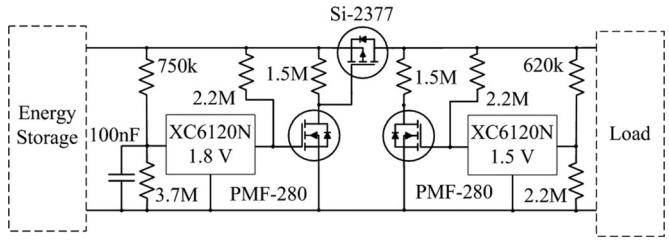


Fig. 5. UVLO circuit: the turn-on and turn-off voltage thresholds can be tuned by the potential dividers connected to the open-drain voltage detectors (XC6120Nxx). The circuit shown earlier is tuned to turn the PMOS on at an input of 2.5 V, and to open the switch at 2.1 V.

C. Burst Powering of Load Electronics

In this paper, a wireless sensor node is used as an example load. TI eZ430-RF2500 has a highly dynamic power consumption that can exceed 45 mW; a typical waveform of the supply current during a single transmission is presented in [14]. The average power consumption during periodic transmissions of 1-s intervals is approximately 80 μW. The node has a wide operating supply voltage range of 2–3.6 V that can be exploited in low-power systems by allowing the voltage across a supercapacitor to drop within this range while the node is active. The challenge for the power conditioning electronics system is thus illustrated by Fig. 4: Low voltage ac must be rectified and boosted to within the allowable dc supply range for the load, and energy storage must be provided to allow the high peak-to-mean power demand of the load to be supplied from a source providing a steady and low power.

During start-up and when the voltage on the storage element falls below the minimum required by the load, the load should be disconnected. This prevents the load holding the harvester and power conditioning system at an equilibrium below the minimum operating voltage [15]. To this end, an UVLO circuit, shown in Fig. 5, is employed.

The circuit connects the load electronics to the energy-storage element via a power-gating transistor when the voltage across the supercapacitor exceeds the threshold voltage set by the potential divider circuit connected to the 1.8-V voltage detector. The load is disconnected when the capacitor voltage drops below the minimum voltage threshold signaled by the 1.5-V voltage detector.

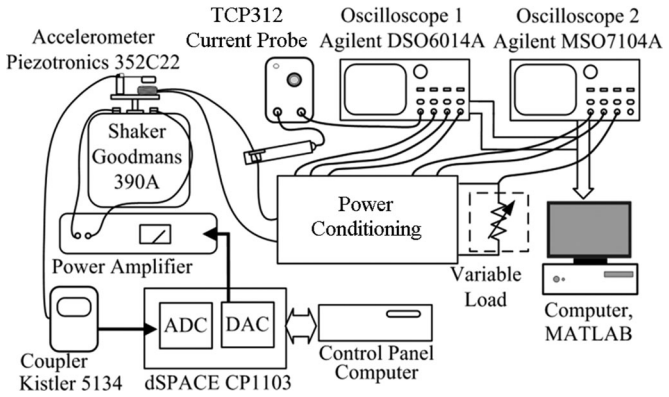


Fig. 6. Experimental setup including a mechanical shaker to excite the energy harvester, controlled by a dSPACE CP1103 platform, keeping the acceleration magnitude constant. The current and voltage waveforms are recorded using two oscilloscopes, and then data are sent to a PC to be processed using MATLAB.

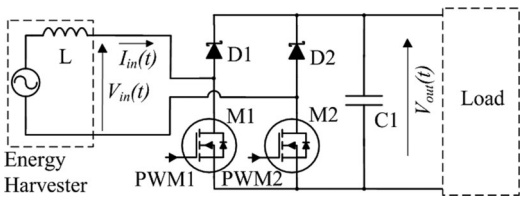


Fig. 7. Circuit schematics of a nonsynchronous full-wave boost rectifier.

D. Experimental Setup

The experimental setup (see Fig. 6) provides a controlled source excitation and records and analyzes the performance parameters of the circuit under test.

A sinusoidal source excitation with a constant acceleration magnitude is provided by the shaker. The output of an accelerometer measuring base excitation is monitored by a dSPACE platform that provides a closed-loop control to maintain a constant excitation magnitude under varying load conditions. Data are acquired at 10-MHz sampling frequency by multiple digital oscilloscopes and streamed via USB to a PC running MATLAB. This permits the processing of high-frequency switching waveforms over many displacement cycles. The variable load is computer controlled.

III. Full-Wave, Nonsynchronous Boost Rectifier Circuit

A. Single-Stage AC–DC Power Converter

A nonsynchronous, full-wave boost rectifier circuit (see Fig. 7) consists of two force-commutated, low-side switches and two passive high-side rectifying devices. The switching frequency is several orders of magnitude higher than the source excitation frequency, which means that the input voltage can be considered constant during a switching cycle. The topology is selected to be able to exploit the parasitic inductance of the coil, circumventing the need for an additional inductor.

During the positive input voltage half-cycle, $M1$ is the primary switching device, complemented by $D1$, a rectifying Schottky diode, while the other low-side transistor, $M2$ can

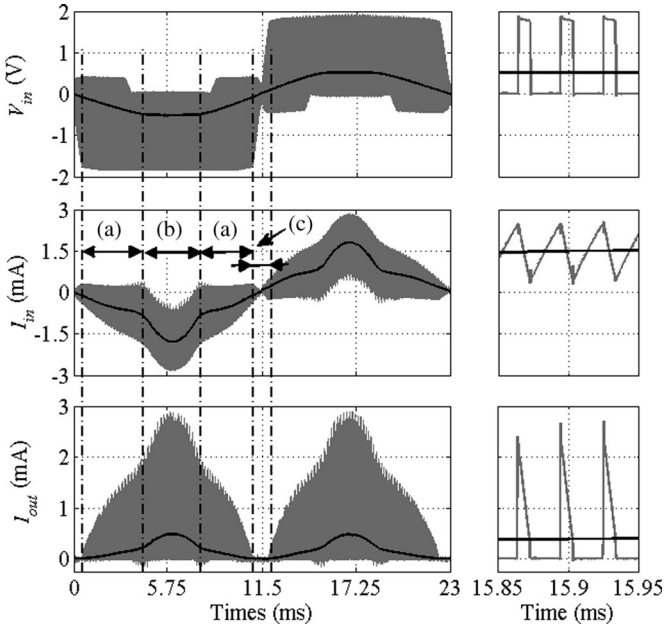


Fig. 8. Measured (gray) instantaneous input voltage, input current, and output current waveforms for a complete displacement cycle at 1.5 m·s^{-2}, 43.6-Hz excitation. Black solid lines represent the switching-cycle-averaged waveforms. Three modes are delineated: (a) DCM, (b) CCM, and (c) no output current region. Figures on the right show the waveforms expanded to 50 μs/div during CCM.

be considered as a secondary switch that is continuously ON, maintaining a return path for the current. Initially, the primary switching device turns ON, shorting the output of the harvester. Current ramps up linearly, transferring energy to the parasitic inductance of the coil. As $M1$ turns OFF, its drain-source voltage increases rapidly until the rectifying diode becomes forward biased, enabling the transfer of the built-up energy from the coil to the output capacitor. $D2$ does not conduct during this half-cycle. During the negative input voltage half-cycle, the roles of the converter legs are swapped.

The operation during a single-input voltage half-cycle can be divided into three modes based on the current conduction: 1) discontinuous current conduction mode (DCM); 2) continuous current conduction mode (CCM); and 3) no output current. Fig. 8 shows the operation of the circuit for a fixed duty ratio δ, and at a fixed load condition during a complete displacement cycle. The measured input current and voltage, and output current waveforms of the power converter have been piecewise averaged over each switching cycle. The switching-cycle averaged current shows the transitions from discontinuous to continuous conduction in the inductance. The transition points depend on the input and output voltage levels, as well as the output current of the converter.

B. Device Selection

The semiconductor device selection is an important part of the design to enable efficient operation down to very low power levels. The main contributors to the power loss within the circuit are briefly discussed in [10]; the measured diode conduction loss and the MOSFET gate charge loss dominate. In this study, semiconductor devices are chosen to minimize these losses without a significant increase in other loss parameters.

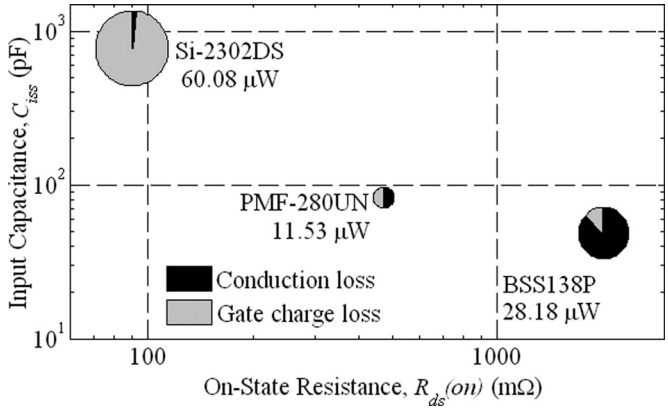


Fig. 9. Calculated gate charge and conduction losses (shown as an area) of three n-type MOSFETs with threshold voltages below 1.5 V at 2.5-mA rms drain-source current. Device parameters quoted in the data sheets are used. The switching frequency is 32.768 kHz and the gate voltage is 1.5 V.

The gate charge loss of a MOSFET can be approximated according to [16]

$$P_{\text{charge}} = f_{\text{sw}} \cdot C_{\text{iss}} \cdot V_{\text{gs}}^2 \tag{5}$$

where C_{iss} is the input capacitance, the sum of C_{gd} and C_{gs}, and V_{gs} is the gate voltage. This equation describes the energy lost as the gate's parasitic capacitances charged via a resistive path to V_{gs} in every switching cycle. This loss is the average value for the two low-side switches over a displacement cycle as there is only a single commutated transistor at any given time. In order to minimize this power loss, devices with low parasitic capacitance and low threshold voltage should be chosen. Typically, a lower gate capacitance value means a higher on-state resistance as it corresponds to smaller gate area and therefore, smaller channel. This is why the conduction loss and the gate charge loss should be considered together, as shown in Fig. 9. The conduction losses are calculated for a typical conducted current level in two switches as

$$P_{\text{cond}} = 2 \cdot R_{\text{ds(on)}} \cdot (I_{\text{ds(RMS)}})^2. \tag{6}$$

PMF-280UN, a vertical device (μTrenchMOS), is selected as it offers a low ratio of parasitic gate capacitance to on-state resistance, resulting in balanced gate charge and conduction losses, and the lowest overall power penalty.

The conduction losses in the diodes are due to the diode's forward voltage drop and are approximated according to

$$P_{\text{cond\_diode}} = V_f \cdot I_{f\text{ave}} \tag{7}$$

where V_f is the diode forward voltage drop that is a function of the forward current I_f, which in turn is determined by the output power and the output voltage. At low output power levels, as the output current decreases, the switching losses due to the diode's junction capacitance become of increasing significance. These losses are calculated as

$$P_{\text{sw\_diode}} = f_{\text{sw}} \cdot C_{\text{jt}} \cdot V_{\text{rr}}^2 \tag{8}$$

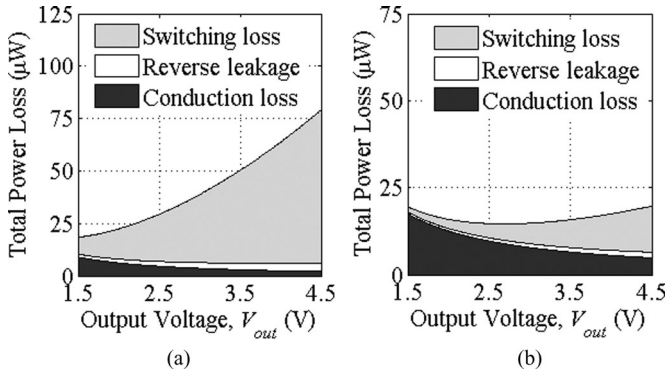


Fig. 10. Total calculated diode power losses, including losses due to conduction, reverse leakage current, and the charging of the parasitic junction capacitance, compared for two Schottky diodes: (a) 1N5817 and (b) 1PS79SB30. The losses are calculated for an average output power of 150 μW.

TABLE I
IMPORTANT DEVICE PARAMETERS

Component	Parameters	Value
PMF-280UN (M1, M2)	Gate capacitance (C_{iss})	45 pF
	Threshold voltage (typical)	0.7 V
	On-state resistance (V_{GS} = 1.8 V)	460 mΩ
1PS79SB30 (D1, D2)	Forward voltage drop (I_f = 1.5 mA)	252 mV
	Reverse leakage current (V_R < 5 V)	< 200 nA
	Junction Capacitance	20 pF
BZ094B15 (C1)	Capacitance	11.5 mF
	Maximum voltage	4.5 V

The values quoted here are based on the datasheet values under typical operating conditions. The capacitance of the supercapacitor is based on measurement. The component identifiers are referring to Fig. 7.

where $C_{\rm jt}$ is the junction capacitance, which is a function of the reverse voltage $V_{\rm rr}$, the output voltage of the converter in this case. Finally, the reverse leakage loss in both diodes combined is

$$P_{\rm leak} = (1+\delta)\cdot I_{\rm rr}\cdot V_{\rm rr}. \tag{9}$$

Fig. 10(a) and (b) shows calculated losses for two power Schottky diodes, 1N5817 and 1PS79SB30, against output voltage, at an average output power level of 150 μW. Despite a lower forward voltage drop and consequently lower conduction losses, the 1N5817 contributes to higher total losses due to its relatively large junction capacitance. These results depend strongly on the operating power, as with increasing output power and output current the conduction losses become more significant. The key electrical parameters of the components used in the implementation of the boost rectifier circuit are shown in Table I.

C. Effects of Pulsewidth Modulation (PWM)

An ideal control circuit would operate the power converter at the duty ratio that results in the maximum output power, as the load voltage varies. This optimization comes at the cost of increased quiescent power consumption that should be weighed against the benefits of continuously optimizing the operating conditions. At low excitation magnitudes, and consequently at very low power, open-loop control is found to offer better performance due to two underlying factors: 1) more significant quiescent power overheads as they represent a higher percentage of the total available power and 2) reduced sensitivity of the output power to the duty ratio, which is explained by the underlying effects of the control parameter variation.

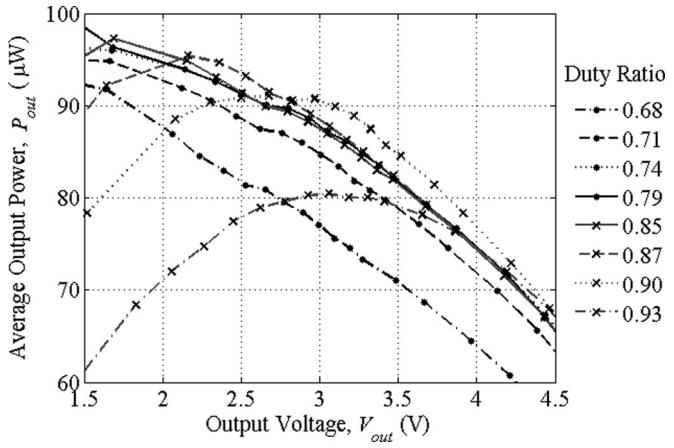


Fig. 11. Output power against output voltage for various duty ratios under steady-state conditions. Source excitation is of fixed at 44 Hz and 1.5 m·s^{-2}.

An in-depth analysis of the effects of PWM for a full-wave boost rectifier is presented in [17]. By varying the duty ratio, the extracted current magnitude and ripple can be controlled that affects the damping of the electromagnetic generator and the conduction loss within the parasitic coil resistance, consequently determining the actual extracted power $P_{\rm gen}$. The apparent input resistance of the rectifier, which is a strong function of the duty ratio, is one of the key parameters that influence the harvester utilization, similarly to the effects of varying ac load resistance as presented in Fig. 3(a). In contrast with the harvester utilization, the power conversion efficiency is shown to be fairly constant over the investigated duty ratio range, thus resulting in a strong correlation between the output power $P_{\rm out}$ of the converter and the extracted power. At low excitation amplitudes, the range of load resistances that can extract close to the optimum power level is increased; at 1.5 m·s^{-2} an ac load between 250 and 680 Ω extracts over 95% of the maximum potential power, while at 4 m·s^{-2} excitation, this range is reduced to between 300 and 550 Ω. Furthermore, the input resistance of the power converter is near independent of the output voltage and current conditions as a result of the combination of low input power and voltage levels that force the converter to operate in DCM only with a high voltage gain. Overall, these effects translate to an increased range of duty ratios that correspond to near optimum conditions for the energy harvesting system.

This is confirmed by the steady-state measurements presented in Fig. 11: The output power of the boost rectifier is measured as a function of the output voltage for different fixed duty ratios, connected to the energy harvester and using external power

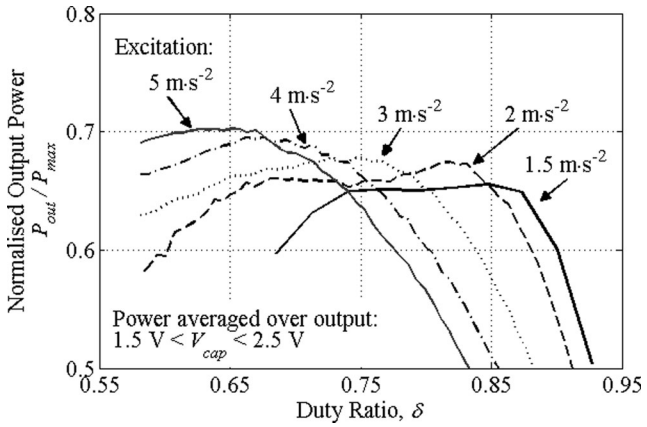


Fig. 12 Average output power over the range of 1.5 V $< V_{\rm cap} <$ 2.5 V normalized to the maximum potential extractable power, under steady-state conditions at different excitation magnitudes.

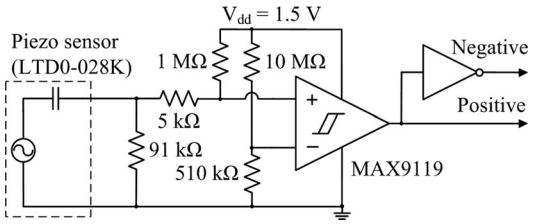


Fig. 13. Polarity detector circuit: a piezoelectric sensor on the cantilever beam provides the input to a level-crossing-detecting comparator circuit.

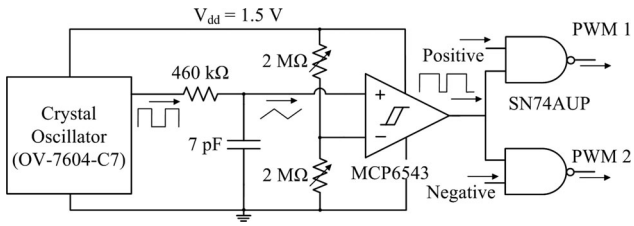


Fig. 14. Gate drive circuitry that produces a variable PWM gate signal of a frequency of 32.768 kHz.

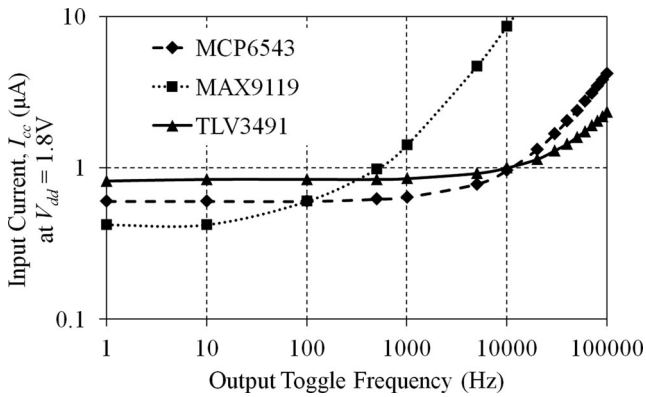


Fig. 15. Measured current consumption of selected COTS micropower comparators as a function of output toggle frequency.

source for the gate drive circuit. The load of the power conditioning system is an 11.5-mF supercapacitor and a controllable resistor varied between 20 and 350 kΩ. The results show that the output power remains within 5% of the optimum for duty ratios between 74% and 85% for the entire output voltage range.

These results for 1.5-m·s^{-2} excitation (corresponding to a maximum available power of 135 μW) show that the maximum output power of the converter is 97 μW in the region of a 1.5–1.7-V output. The power drops as the output voltage increases, as the switching losses, particularly the parasitic drain-source capacitances and the diodes' junction capacitance charge-up losses, become more significant, resulting in a reduced conversion efficiency.

Using the data of Fig. 11, the output-power measurements recorded between 1.5 and 2.5 V for a given duty ratio are averaged, these values are shown in Fig. 12 normalized to the maximum extractable power. Similarly, measured data for higher excitation levels are also included in the diagram to present how the relationship between the mean output power over the output voltage range and the duty ratio changes with excitation.

The plateau observed at 1.5-m·s^{-2} excitation, representing the wide range of duty ratios that can extract close to the maximum power level, is gradually reduced and the optimum point is shifted to lower duty ratios as the excitation amplitude and the input power increases. Therefore, a fixed duty ratio of 71% to the left-hand side of the plateau is chosen for an open-loop operation. This offers optimum performance at low power, where avoiding the power penalty of a practical control circuit is most important, at the expense of providing only near-optimum performance at higher power.

IV. Ancillary Circuits

A. Input-Voltage Polarity Detection

The operation of the boost rectifier depends on the polarity of the input voltage. A passive piezoelectric film sensor on the cantilever beam provides the input signal for a low-power comparator-based (MAX9119) level-crossing detector circuit (see Fig. 13). The output of the comparator and its inverted signal are used to select the primary switching transistor for the particular half-cycle. The power consumption of the polarity detector circuit is measured to be 3 μW at 1.5 V.

B. Gate Drive Circuit

The gate drive circuitry consists of two parts; a crystal oscillator-based triangular waveform generator, and a comparator that generates the PWM signal. The gates of the transistors are driven directly from the output of two low-power NAND gates (SN74AUP1G). A low-power crystal oscillator (OV-7604-C7) is used to provide a 32.768-kHz square wave, which is transformed into a triangular waveform using an *RC* filter as shown in Fig. 14. The reference voltage for the low-power comparator (MCP6543) is set by two multiturn 2-MΩ potentiometers, resulting in a fixed duty ratio square wave output.

The quiescent current consumption of micropower comparators increases significantly with toggle rate [18], due to shoot-through current in the push–pull output stage during transitions, as exemplified by the measured current consumption of selected micropower comparators, shown in Fig. 15. At low toggle

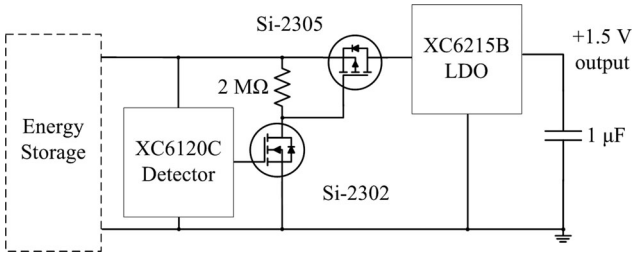


Fig. 16. Fully autonomous 1.5-V linear regulator with under voltage lockout.

frequencies, sub-100 Hz, the MAX9119 presents the lowest input current at 0.34 μA; however, at the switching frequency of 32.768 kHz, the MCP6543 draws significantly less current. The TLV3491 has a higher minimum operating voltage than the MCP6543 that would increase the minimum power consumption of the gate drive circuitry.

The overall power consumption of the gate drive circuit is 6.7 μW at 1.5 V, with no load connected to the output. The rise and fall times are approximately 50 ns when connected to the gate of a single PMF-280UN transistor. The maximum duty ratio δ that the gate drive circuit provides at 32.768 kHz is around 97%.

C. Power Supply to the Ancillary Circuits

A 1.5-V low dropout (LDO) linear regulator (Torex XC6215B) with low quiescent current consumption (0.8-μA typ.) is used to supply the polarity detect and gate drive circuitry. The minimum input voltage of the linear regulator places a lower bound on the capacitor voltage $V_{\rm out}$ range, which is now 1.5–4.5 V. Below 1.5 V, the input of the linear regulator is disconnected from the supercapacitor by a p-type MOSFET (see Fig. 16), in order to avoid leakage current. An XC6120C voltage detector turns the low-side switch on when 1.5 V is reached across the storage element.

The measured power consumption of all the ancillary circuits together, including quiescent losses of the linear regulator and gate charge-up losses, goes from a minimum of 22.8 μW at $V_{\rm out} = 1.5$ V ($I_{\rm ss} = 15.2$ μA, $V_{\rm out} = 1.5$ V, $f_{\rm switching} = 32.768$ kHz, $\delta = 0.809$), up to 72.5 μW at $V_{\rm out} = 4.5$ V.

V. Passive Start-Up Circuit

The capability to operate when no stored energy is available is not only essential to "jump start" the circuit but also to recover after energy lulls when the source excitation is too small for power generation. Different techniques have been proposed in the literature to solve this issue [2]; in this study, two of these techniques are combined: passive operation of the main power conditioning topology, and additional parallel passive power extraction.

The boost rectifier circuit, when not actively commutated behaves as a passive full-wave diode bridge rectifier using the two Schottky diodes as the high-side rectifiers and the parasitic body diode of the NMOS switches as the low-side devices (see Fig. 17). This rectifier cannot, however, operate below an input voltage of less than the forward voltage drop of the diodes. Also,

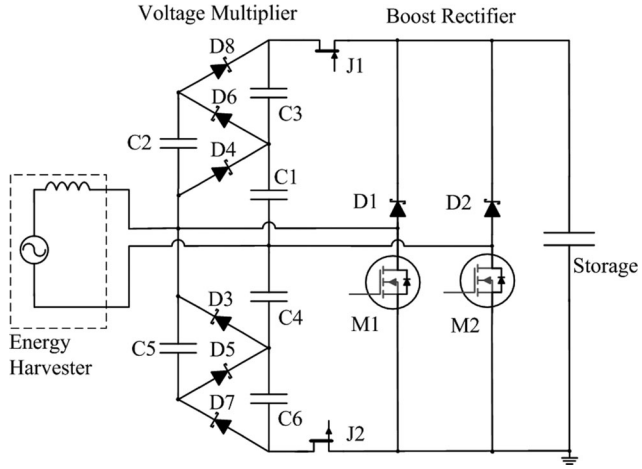


Fig. 17. Passive full-wave voltage multiplier circuit (sextupler) in parallel with the boost rectifier circuit that forms a full-bridge diode rectifier when not active. Diodes are 1PS79SB30, and the capacitors are 47-μF ceramic components.

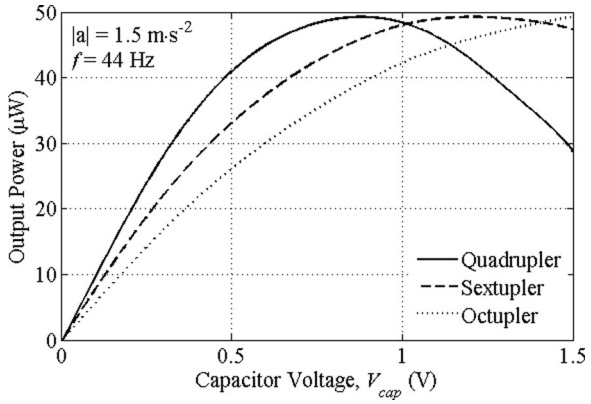


Fig. 18. Measured output power of 4-, 6-, and 8-stage voltage multipliers during cold start as a function of the output voltage.

it cannot boost the output voltage. Therefore, a secondary circuitry is connected in parallel with the primary power converter to aid the zero-energy start-up and charge the output voltage to above 1.5 V from low input voltages.

Passive voltage multiplier circuits are commonly used for electromagnetic energy harvesters as the main power extraction circuit [19], and therefore are optimized for power extraction under specific load conditions. This entails the selection of diodes and capacitor sizes to minimize the output impedance of the voltage multiplier at the excitation frequency [20], and choosing a number of multiplication stages to offer an output voltage which is close to the optimum loading conditions for the generator. By contrast, the principal purpose of the circuit in this system is to minimize the start-up time, which is the time it takes the supercapacitor to charge from 0 to 1.5 V. The charging of a total capacitance of 12.8 mF to 1.5 V is compared experimentally for 4-, 6-, and 8-stage passive full-wave voltage multiplier circuits. During the test, the start-up circuit is connected to the rest of the power conditioning circuitry. The measured results are shown in Fig. 18:The output power of the voltage multiplier circuit varies over the charge-up period. The quadrupler's output voltage peaks around 0.85 V, the sextupler reaches its maximum

TABLE II
PASSIVE VOLTAGE MULTIPLIER COMPARISON

Voltage Multiplier	Charge-up Time	Output Power Penalty (V_{cap} = 2.5V)
Quadrupler	498.1 s	2.39 μW
Sextupler	378.5 s	4.57 μW
Octupler	466.5 s	6.73 μW

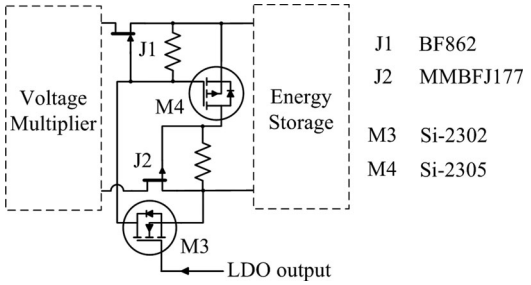


Fig. 19. Voltage multiplier disconnect circuit, using normally on JFET devices. The pull-up and pull-down resistors are 2 MΩ.

output power at 1.2 V, while the octupler topology approaches its maximum at 1.5 V. These charge-up curves result in different start-up times for the three topologies as listed in Table II. The results show that the six-stage full-wave voltage multiplier circuit is the best at 1.5-m·s^{-2} excitation when the start-up time is considered.

The passive voltage multiplier must be disconnected during the active operation of the boost rectifier circuit, to prevent unwanted discharge of the output capacitors. The normally-on JFET circuit shown in Fig. 19 is designed to disconnect the output of the sextupler circuit from the energy storage in both the ground and the voltage rails (see indicated in Fig. 17) when the linear regulator's output voltage is enabled.

The 1.5-V output from the LDO turns M3 ON, which pulls the gate of J1 low, turning the n-type JFET off. M3 also turns M4 ON that pulls the gate of J2 high, opening the p-type JFET that is used to maintain the ground connection. This effectively open circuits the output of the passive voltage multiplier. During the active operation of the boost rectifier, the output voltage before the JFET switches can reach up to 25 V as the input of the voltage multiplier sees the stepped-up voltage levels. As the voltage multiplier remains connected to the energy harvester, it continues to draw current and thus reduces the maximum power that can be extracted by the power converter. This results in a measured power penalty deducted from the useful output power that is dependent on the number of stages of the voltage multiplier as shown in Table II for $V_{\rm cap} = 2.5$ V.

VI. EXPERIMENTAL RESULTS AND DISCUSSION

The charging of a 12.8-mF supercapacitor from zero stored energy to the turn-on point of the load electronics' UVLO at 1100 s is shown in Fig. 20, alongside the utilization factor, the

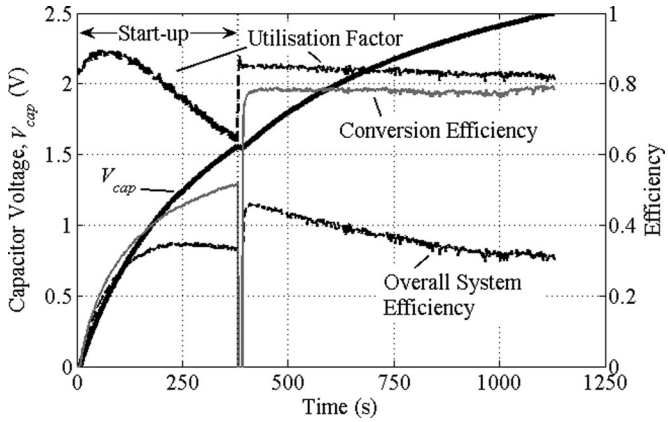


Fig. 20. Complete charge-up cycle in fully autonomous operation. During the start-up phase (capacitor voltage $<$ 1.5 V), the passive voltage multiplier charges the storage element until the active boost rectifier takes over. Excitation is set to 44 Hz at 1.5 m·s^{-2}, and duty ratio is fixed at 71%.

conversion efficiency, and system efficiency. After a 340-s start-up phase, the voltage multiplier has successfully cold started the active converter. The overall system efficiency achieved during start-up is limited by the low conversion efficiency of the passive circuit, a result of the low 350-mV$_{\rm rms}$ input voltage. At the start-up point, there is a brief lull in the output power during which the output capacitors of the voltage multipliers are charged to approximately ±4.5 V. The storage element must be sized to store enough energy to be able to supply the gate drive circuit's power during this period without dipping below the cutoff threshold. The start-up is a series of events that consists of the following: 1) the 1.5-V linear regulator is enabled; 2) the VM is disconnected from the supercapacitor by opening the JFET switches; 3) the gate drive circuit is powered up; 4) the low-side transistors are switched at the high switching frequency, 5) which lead to the step-up of the input voltage; 6) the input voltage is initially capped by the output capacitors of the open-circuited voltage multipliers while they are charged; and finally 7) the input voltage is boosted high enough to forward bias the rectifying diodes of the boost rectifier so that output current can flow to the storage capacitor.

As the active circuitry starts up, the power extracted from the harvester is increased by 33.5%, from 85.2 to 113.7 μW, and the conversion efficiency by 50%, from 52% to 77.8%, resulting in almost doubling of the converter output power $P_{\rm out}$. However, this increase in the output power does not translate equally to the transferred power $P_{\rm store}$ due to the onset of quiescent power overheads $P_{\rm quies}$ of the gate drive circuit. Therefore, the overall system efficiency is increased by 39%, from 32.8% to 45.7%. In an active conversion mode, the utilization factor and conversion efficiency remain reasonably constant, an expression of the system's lack of sensitivity to the duty ratio over this voltage range at very low excitation levels. At higher excitation magnitudes, i.e., at higher generated power levels, this relationship no longer holds, thus rendering the fixed duty ratio regime suboptimal.

The voltage and current waveforms of the wireless transmitter are shown in Fig. 21 under periodic operation. The energy storage is reduced to 1 mF for this test to facilitate the real-time capture of the long charge-discharge period. The average power

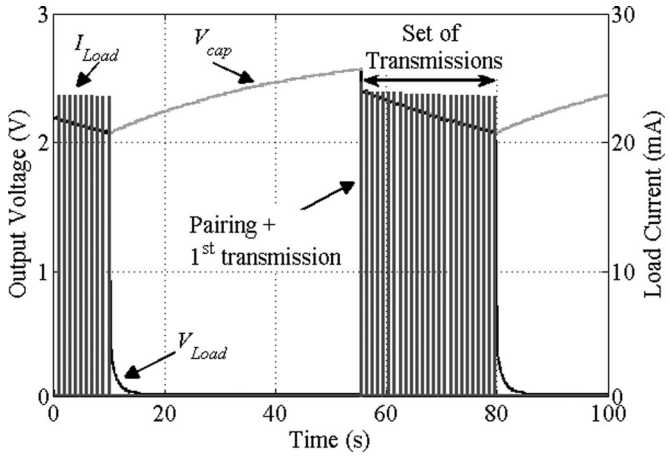


Fig. 21. Storage voltage $V_{\rm cap}$ ($C = 1$ mF), load supply voltage $V_{\rm Load}$, and current $I_{\rm load}$ against time for a complete charge-discharge cycle. The current pulses drawn by the node are individual transmission.

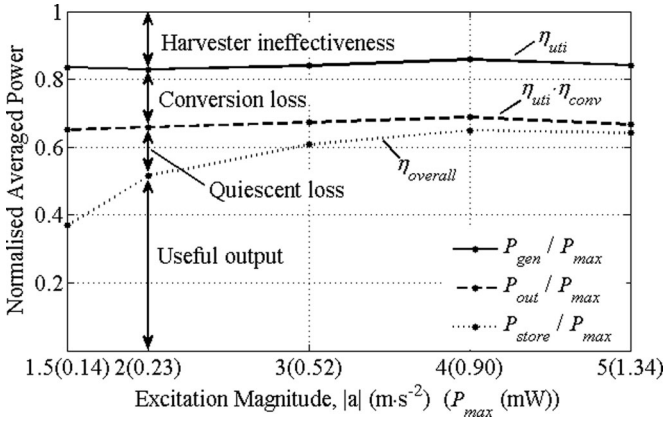


Fig. 22. Measured power (generated, output, and useful) averaged over a charge-up cycle of 1.5–2.5 V and normalized to the maximum generated power at five excitations spanning an order of magnitude of available power.

drawn by the transmitter is approximately 80 μW during the transmissions, which exceeds the average output power of the converter, resulting in a decreasing output voltage as the capacitor is discharged during the operation of the transmitter. The output voltage range of 2.5–2.1 V set by the UVLO circuit (see Fig. 5) allows for a pairing with the access point plus 25 sense-and-transmit operations at 1-s intervals. The storage element is recharged to 2.5 V in 45 s after the load has been disconnected, which means that the transmitter operates only for 35.7% of the time. The overall average power consumption of load is reduced by the duty cycled operation to below the average output power of the boost rectifier.

The minimum excitation magnitude at which the power conditioning system successfully starts up and charges the supercapacitor to 2.5 V is 1.25 m·s^{-2}, this corresponds to a maximum generated power $P_{\rm gen}$ under optimum resistive load conditions of 89 μW. This also determines a MOP of the system of 66.3 μW, which is the maximum input power $P_{\rm in}$ during a charge cycle at minimum excitation. This maximum occurs at $V_{\rm out} = 2.5$ V, where the power overheads are at their maximum.

The power conditioning system is tested over a range of excitation magnitudes, corresponding to an input power range of over a magnitude. Fig. 22 shows the important system performance metrics averaged over the maximum output voltage swing of 1.5–2.5 V when charging the 12.8-mF supercapacitor, and normalized to the maximum generated power under optimum resistive load conditions. The average utilization factor appears constant over the entire range; however, this conceals the fact that at high excitation levels, above 3 m·s^{-2}, the variation in the utilization can exceed $\pm 5\%$ over the 1.5–2.5 V output voltage range. The conversion efficiency is also constant around 80% over this range, however, it tails off at very low power due to quiescent loss, and at high power levels due to suboptimal control.

At very low power levels the parasitic capacitance charge-up losses within the converter become increasingly more significant, indicating that smaller devices (e.g., BSS138P) could increase the efficiency. At high power levels, the conduction losses are the dominant contributors to the power losses, in particular the diode's forward voltage drop. At these power levels, the lower forward voltage drop of, for example, the Schottky diode 1N5817 could potentially increase the power conversion efficiency.

The overall system efficiency, after accounting for the power consumption of the gate drive circuit and other quiescent losses within the system, is 50% at 200 μW maximum generated power levels and reaches 65% at 900 μW. The suboptimal loading of the harvester results in a reduced generated power compared to the maximum extractable power by 34.2 μW and by 127.8 μW at 200- and 900-μW power levels, respectively. The rest of the overall system efficiency penalty is down to power lost within the power converter due to lossy conversion process and the quiescent overheads. At 900 μW, these losses are 153 and 34.2 μW, respectively.

VII. Conclusion

This paper presents and discusses the design of a full-wave boost rectifier circuit that is capable of fully autonomous operation down to sub-100-μW power levels. The power conditioning system is shown to be capable of cold start, and of burst powering a wireless sensor node whose power demand exceeds the generated power by over 2 orders of magnitude.

Open-loop, fixed duty-ratio operation of the switching converter is shown to provide close to optimal performance at very low excitation and power levels, where the power budget of any practical maximum power point tracking system can be considered prohibitively large. The selection of the duty ratio is detailed for the example application, including the selection of storage capacity and output voltage range.

An overall system efficiency of 44% is recorded at 100-μW input power, with a utilization of 84%. The conversion efficiency is close to 80%, excluding the quiescent power overheads of the ancillary circuitry.

These important system performance metrics are measured over an order of magnitude of power levels in burst power operation. The average utilization remains over 83% for the

entire range, while the conversion efficiencies are close to 80% on average. An average overall efficiency of 65% is observed at 900-μW maximum generated power, which is a significant improvement compared to reported systems within the energy harvesting literature.

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