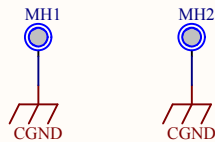
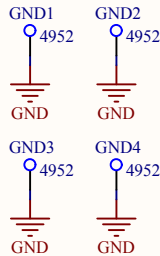


Nixie Tube Supply Test

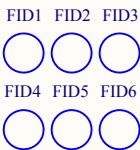
MOUNTING HOLES



GND CLIPS



FIDUCIALS



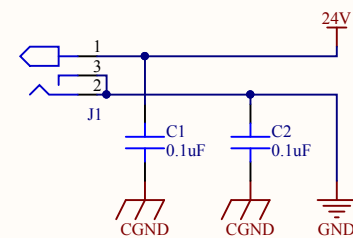
- Test points are not on the schematic, they will be determined by rules in the layout and checked by DRC
- GND test points are Keystone 4952 series, but wires can be populated instead

Title <i>Nixie Test PCB</i>				
Size: B	Drawn By: Brian	Revision: A		
Date: 6/9/2015		Sheet* of *		
File: 01 Title.SchDoc				

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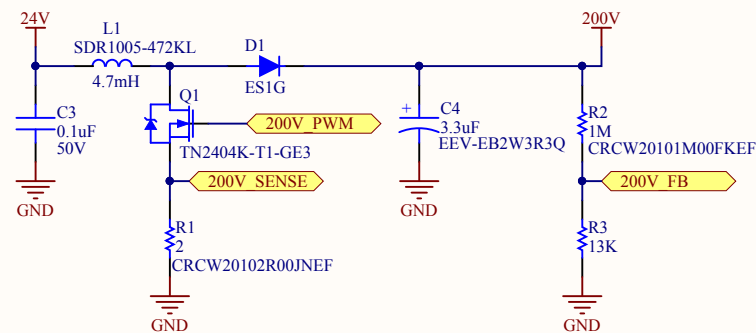
Title <i>Nixie Test PCB</i>				
Size: B	Drawn By: Brian	Revision: A		
Date: 6/9/2015	Sheet* of *			
File: 02 Data.SchDoc				

INPUT POWER

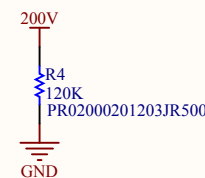


- Barrel connector (J1) can fit both 2.1mm and 2.5mm diameter center pins (5.5mm outer diameter)
- C1, C2 used for rudimentary ESD protection and EMC filtering

HIGH VOLTAGE BOOST (MCU CONTROLLED)

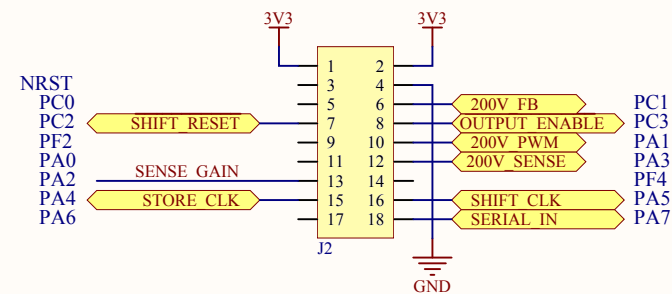


LOAD RESISTOR



- Target Switching frequency for Q1 is 200 kHz
- Target duty cycle: 88% (24 --> 200V)
- Target load current: 6mA
- Calculated:
 - Minimum input capacitance for 50mV ripple: 64nF
 - Minimum inductance: 1056uH
 - Peak inductor current: 62.5mA
 - Minimum output capacitance: 0.3uF
 - Minimum input current for continuous mode: 1.5mA
- Load resistor R4 will be used to keep the power supply in continuous mode by drawing at least 1.5mA (for testing only, depopulated when nixie tubes are used)

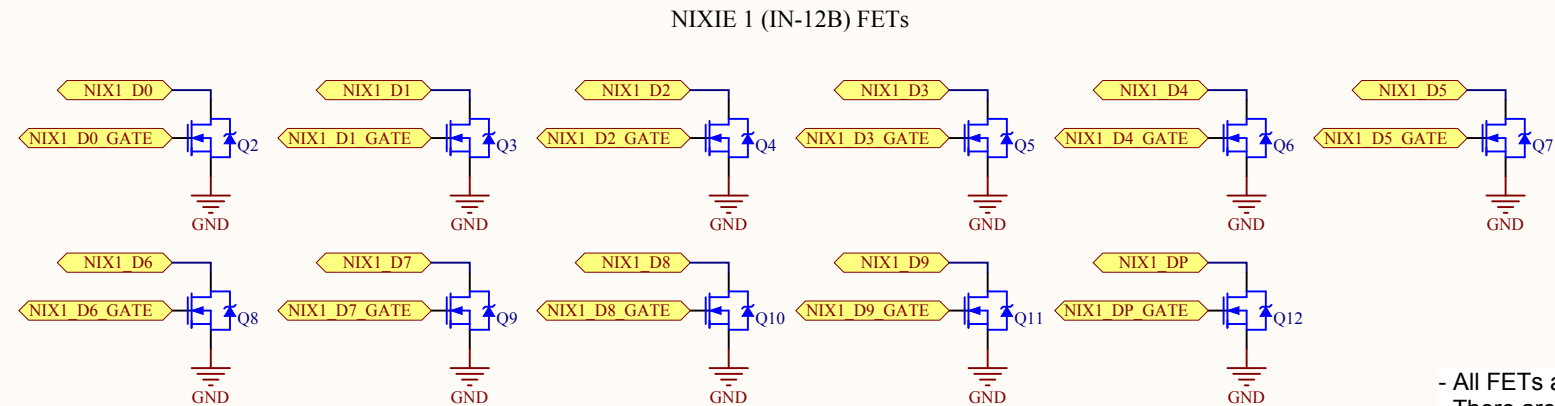
STM32F3 Discovery Header (Partial)



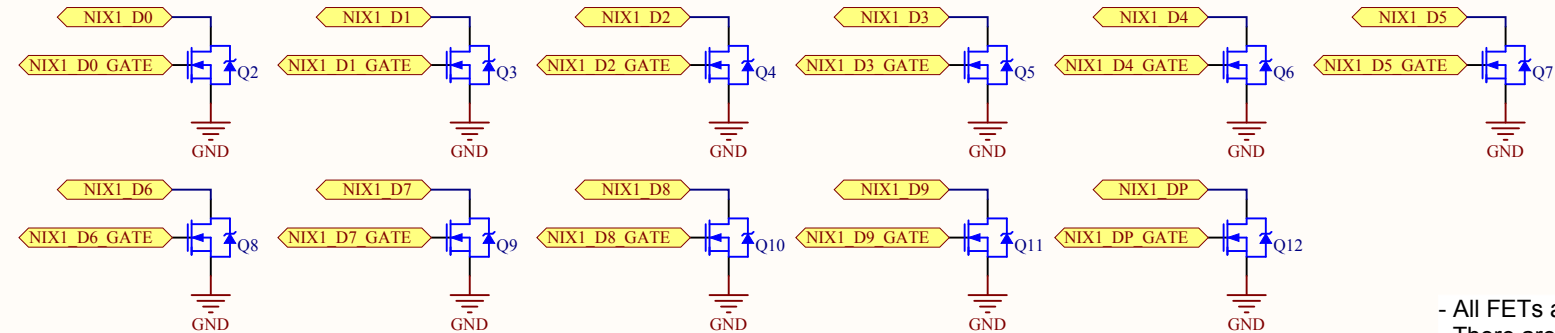
- Header J2 connects to P1 on the STM32F3 Discovery board (STM32F303VCT6)
- 200V_FB (voltage feedback) goes to PC1, which is connected to ADC1 or ADC2 CH 7.
- 200V_PWM (FET gate drive) goes to PA1, which is connected to TIM2_CH2 (32-Bit timer)
- 200V_SENSE (current sense) goes to PA3, which is connected to the non-inverting input of OPAMP1
- The inverting input of OPAMP1 will be the internal gain array, set to 16 (assuming a peak current of 63mA: $0.063A * 2 \text{ ohms} = 0.126V * 16 = 2.016V$ after gain)
- The output of OPAMP1 is on PA2, where the amplified signal can be measured; it is also connected internally to ADC1 CH3 for internal measurement
- SHIFT_CLK, SERIAL_IN, and STORE_CLK are on SPI1_SCK, SPI1_MOSI, SPI1_NSS (PA4, PA7, and PA4) respectively
- OUTPUT_ENABLE and SHIFT_RESET are both on GPIO (PC3 and PC2)
- Pin 3 is the MCU reset pin (NRST)

Title <i>Nixie Test PCB</i>				
Size: B	Drawn By: Brian	Revision: A		
Date: 6/9/2015		Sheet* of *		
File: 03 Power.SchDoc				

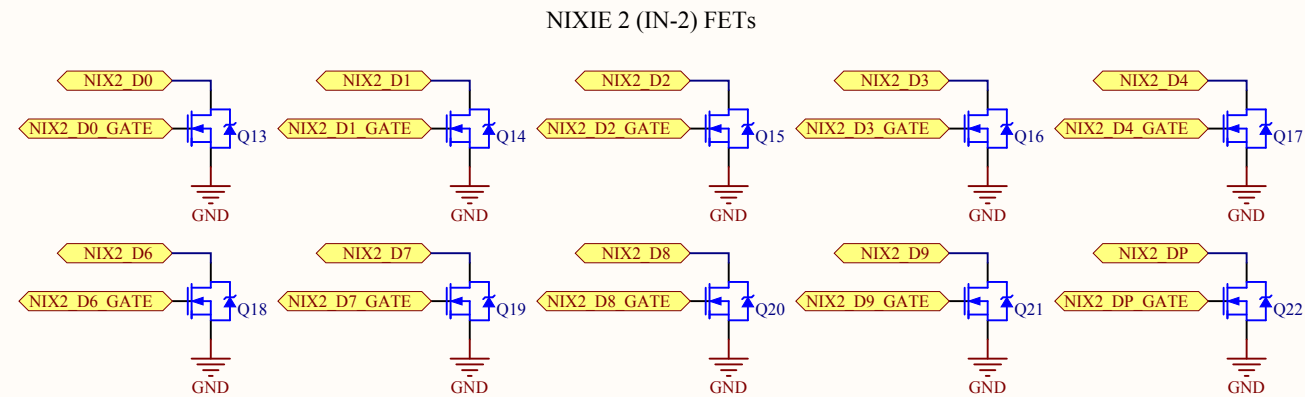
NIXIE 1 (IN-12B)



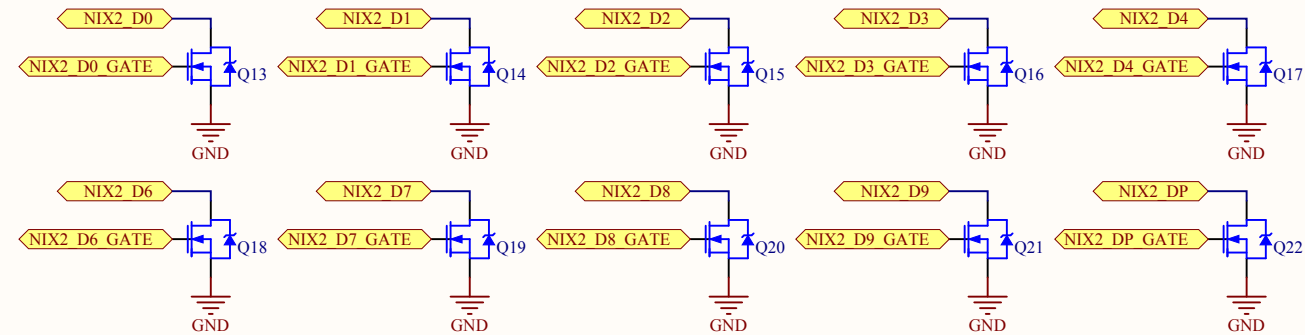
NIXIE 1 (IN-12B) FETs



NIXIE 2 (IN-2)

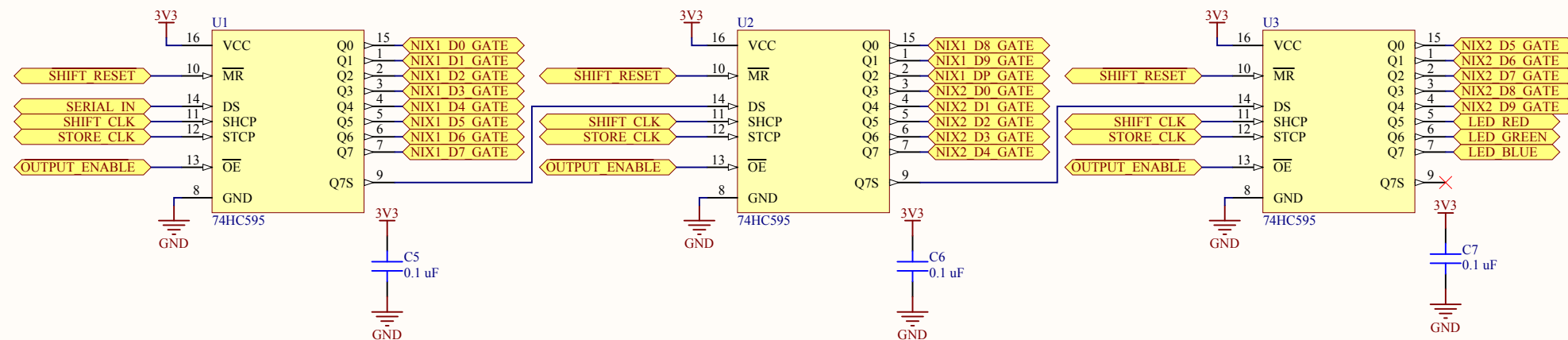


NIXIE 2 (IN-2) FETs



- All FETs are Infineon BSS131
- There are no pull down resistors on the FET gates to ensure the nixie tubes are off. Make sure to set the shift register states BEFORE turning on the HV PSU
- IN-12B current is 2.5mA nominal (3.5 mA max), forward voltage is 145V nominal
- IN-2 current is 1.5mA nominal (2 mA max), forward voltage is 150V nominal
- Assuming 200V supply, and worst case 130 Vf for tubes:
 - IN-12B: $(200-130)/33k = 2.12mA$
 - IN-2: $(200-130)/47k = 1.489mA$
- Current using nominal Vf:
 - IN-12B: $(200-145)/33k = 1.66mA$
 - IN-2: $(200-150)/47k = 1.06mA$
- Running at 230V should bring currents back into range if nominal values are correct
- Values will likely require tuning

SHIFT REGISTERS



BACKLIGHTING LED (NIX1)

