

## MC14584B

### Hex Schmitt Trigger

The MC14584B Hex Schmitt Trigger is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14584B may be used in place of the MC14069UB hex inverter for enhanced noise immunity to "square up" slowly changing waveforms.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Can Be Used to Replace MC14069UB
- For Greater Hysteresis, Use MC14106B which is Pin-for-Pin Replacement for CD40106B and MM74CI4

**MAXIMUM RATINGS\*** (Voltages Referenced to V<sub>SS</sub>)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	− 0.5 to + 18.0	V
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	− 0.5 to V <sub>DD</sub> + 0.5	V
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	± 10	mA
P <sub>D</sub>	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	− 65 to + 150	°C
T <sub>L</sub>	Lead Temperature (8-Second Soldering)	260	°C

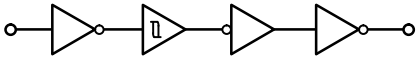
\* Maximum Ratings are those values beyond which damage to the device may occur.

† Temperature Derating:

Plastic "P" and D/DW" Packages: − 7.0 mW/°C From 65°C To 125°C

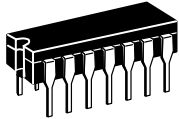
Ceramic "L" Packages: − 12 mW/°C From 100°C To 125°C

**EQUIVALENT CIRCUIT SCHEMATIC**  
(1/6 OF CIRCUIT SHOWN)

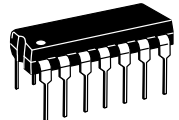


This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range V<sub>SS</sub> ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>DD</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V<sub>SS</sub> or V<sub>DD</sub>). Unused outputs must be left open.



**L SUFFIX**  
CERAMIC  
CASE 632



**P SUFFIX**  
PLASTIC  
CASE 646



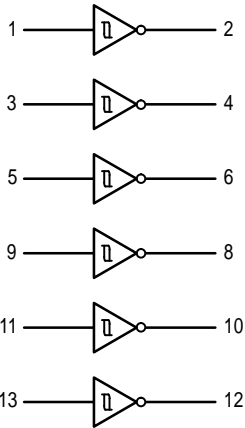
**D SUFFIX**  
SOIC  
CASE 751A

**ORDERING INFORMATION**

MC14XXXBCP Plastic  
MC14XXXBCL Ceramic  
MC14XXXBD SOIC

T<sub>A</sub> = − 55° to 125°C for all packages.

**LOGIC DIAGRAM**



V<sub>DD</sub> = PIN 14  
V<sub>SS</sub> = PIN 7

**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to  $V_{SS}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	– 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage $V_{in} = V_{DD}$  $V_{in} = 0$	“0” Level  $V_{OL}$	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	“1” Level  $V_{OH}$	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Output Drive Current ( $V_{OH} = 2.5$ Vdc) ( $V_{OH} = 4.6$ Vdc) ( $V_{OH} = 9.5$ Vdc) ( $V_{OH} = 13.5$ Vdc)  ( $V_{OL} = 0.4$ Vdc) ( $V_{OL} = 0.5$ Vdc) ( $V_{OL} = 1.5$ Vdc)	Source  $I_{OH}$	5.0	– 3.0	—	– 2.4	– 4.2	—	– 1.7	—	mAdc
		5.0	– 0.64	—	– 0.51	– 0.88	—	– 0.36	—	
		10	– 1.6	—	– 1.3	– 2.25	—	– 0.9	—	
		15	– 4.2	—	– 3.4	– 8.8	—	– 2.4	—	
	Sink  $I_{OL}$	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	$I_{in}$	15	—	$\pm 0.1$	—	$\pm 0.00001$	$\pm 0.1$	—	$\pm 1.0$	$\mu$ Adc
Input Capacitance ( $V_{in} = 0$ )	$C_{in}$	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	$I_{DD}$	5.0	—	0.25	—	0.0005	0.25	—	7.5	$\mu$ Adc
		10	—	0.5	—	0.0010	0.5	—	15	
		15	—	1.0	—	0.0015	1.0	—	30	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) ( $C_L = 50$ pF on all outputs, all buffers switching)	$I_T$	5.0 10 15	$I_T = (1.8 \mu A/kHz) f + I_{DD}$ $I_T = (3.6 \mu A/kHz) f + I_{DD}$ $I_T = (5.4 \mu A/kHz) f + I_{DD}$							$\mu$ Adc
Hysteresis Voltage	$V_{H\ddagger}$	5.0	0.27	1.0	0.25	0.6	1.0	0.21	1.0	Vdc
		10	0.36	1.3	0.3	0.7	1.2	0.25	1.2	
		15	0.77	1.7	0.6	1.1	1.5	0.50	1.4	
Threshold Voltage Positive–Going   Negative–Going	$V_{T+}$	5.0	1.9	3.5	1.8	2.7	3.4	1.7	3.4	Vdc
		10	3.4	7.0	3.3	5.3	6.9	3.2	6.9	
		15	5.2	10.6	5.2	8.0	10.5	5.2	10.5	
	$V_{T-}$	5.0	1.6	3.3	1.6	2.1	3.2	1.5	3.2	Vdc
		10	3.0	6.7	3.0	4.6	6.7	3.0	6.7	
		15	4.5	9.7	4.6	6.9	9.8	4.7	9.9	

#Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

\*\*The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V f k$$

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V = (V_{DD} - V_{SS})$  in volts,  $f$  in kHz is input frequency, and  $k = 0.001$ .

$\ddagger V_H = V_{T+} - V_{T-}$  (But maximum variation of  $V_H$  is specified as less than  $V_{T+} \text{ max} - V_{T-} \text{ min}$ ).

# SWITCHING CHARACTERISTICS ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	Min	Typ #	Max	Unit
Output Rise Time	$t_{TLH}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Output Fall Time	$t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time	$t_{PLH}$ , $t_{PHL}$	5.0 10 15	— — —	125 50 40	250 100 80	ns

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

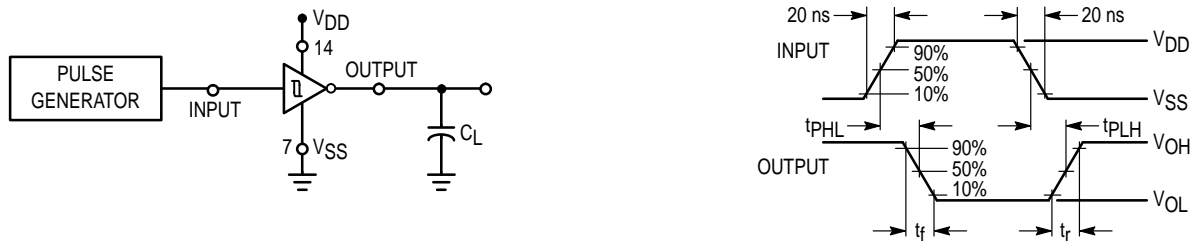
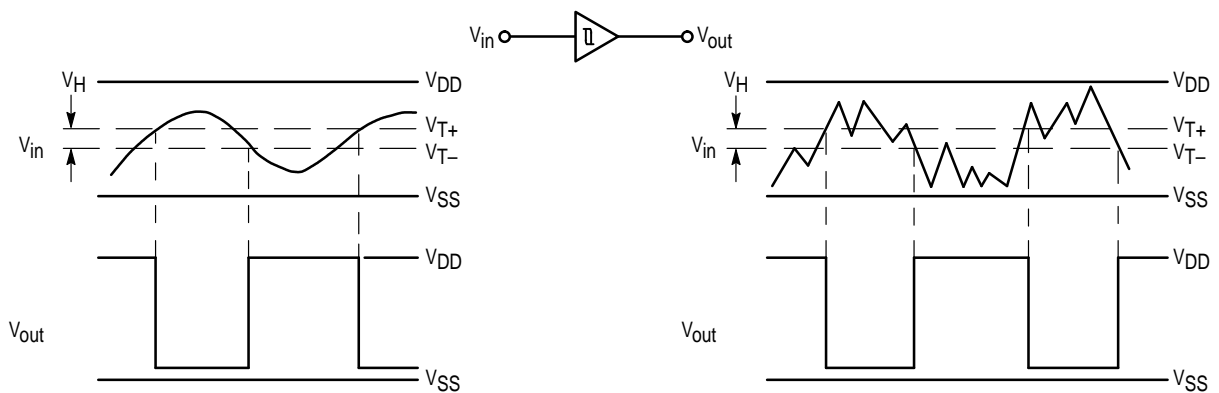


Figure 1. Switching Time Test Circuit and Waveforms



(a) Schmitt Triggers will square up inputs with slow rise and fall times.

(b) A Schmitt trigger offers maximum noise immunity in gate applications.

Figure 2. Typical Schmitt Trigger Applications

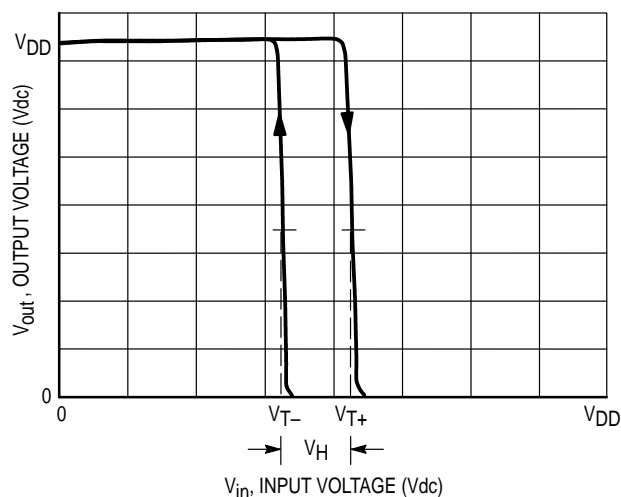


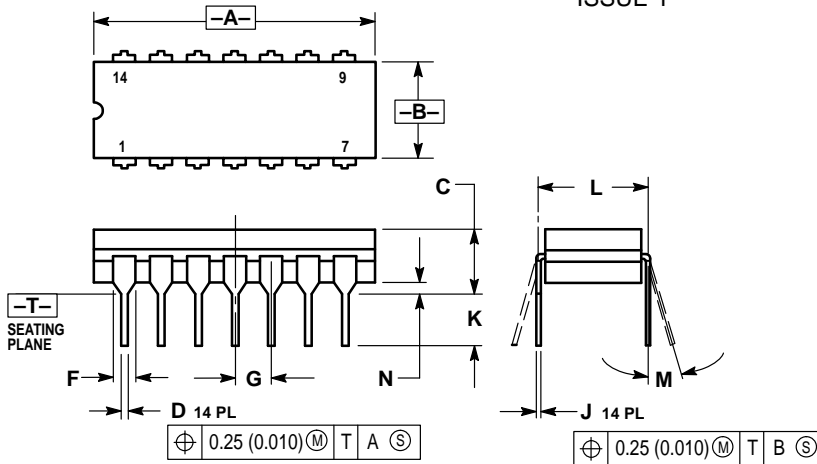
Figure 3. Typical Transfer Characteristics

## PIN ASSIGNMENT

IN 1	1	14	$V_{DD}$
OUT 1	2	13	IN 6
IN 2	3	12	OUT 6
OUT 2	4	11	IN 5
IN 3	5	10	OUT 5
OUT 3	6	9	IN 4
$V_{SS}$	7	8	OUT 4

## OUTLINE DIMENSIONS

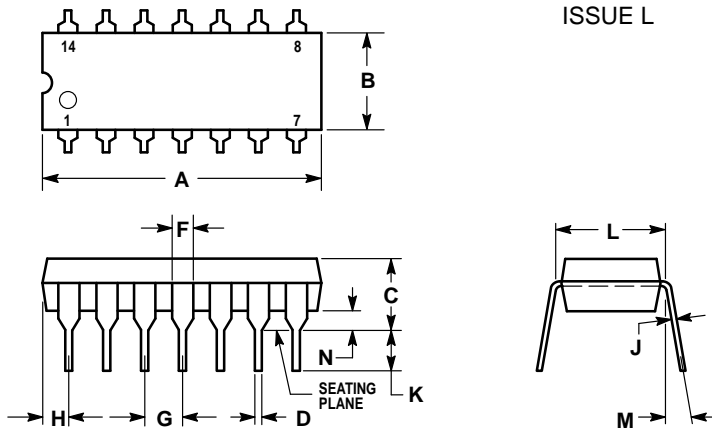
### L SUFFIX CERAMIC DIP PACKAGE CASE 632-08 ISSUE Y



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.94
B	0.245	0.280	6.23	7.11
C	0.155	0.200	3.94	5.08
D	0.015	0.020	0.39	0.50
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

### P SUFFIX PLASTIC DIP PACKAGE CASE 646-06 ISSUE L

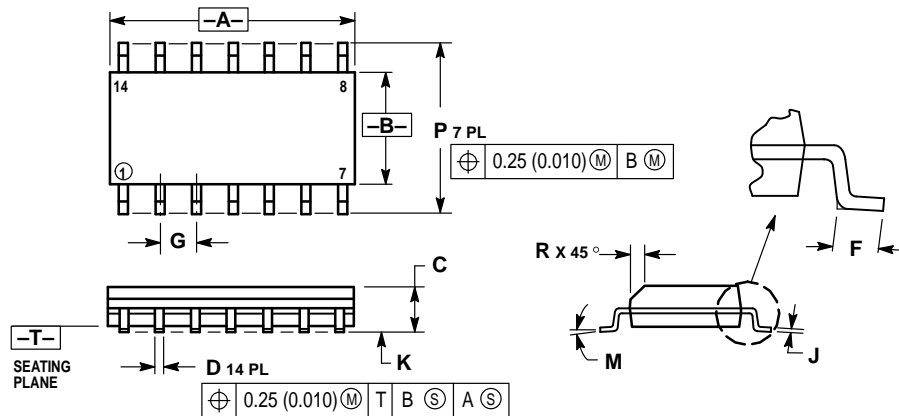


- NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
  2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  4. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

## OUTLINE DIMENSIONS

### D SUFFIX PLASTIC SOIC PACKAGE CASE 751A-03 ISSUE F



#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
E	0.40	1.25	0.016	0.049
F	1.27	BSC	0.050	BSC
G	0.19	0.25	0.008	0.009
H	0.10	0.25	0.004	0.009
I	0°	7°	0°	7°
J	5.80	6.20	0.228	0.244
K	0.25	0.50	0.010	0.019

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MC14584B/D



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