

IRFR220

N-channel enhancement mode field effect transistor

Rev. 01 — 14 August 2001

Product data

1. Description

N-channel enhancement mode field-effect transistor in a plastic package using **TrenchMOS™¹** technology.

Product availability:

IRFR220 in SOT428 (D-PAK).

2. Features

- Fast switching
- Low on-state resistance
- Surface mount package.

3. Applications

- Switched mode power supplies
- DC to DC converters.

4. Pinning information

Table 1: Pinning - SOT428 (D-PAK), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)	<p>Top view MBK091</p> <p>SOT428 (D-PAK)</p>	<p>MBB076</p>
2	drain (d) [1]		
3	source (s)		
mb	mounting base; connected to drain (d)		

[1] It is not possible to make connection to pin 2 of the SOT428 package.

1. TrenchMOS is a trademark of Koninklijke Philips Electronics N.V.



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5. Quick reference data

Table 2: Quick reference data

Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)	$T_j = 25$ to 150 °C	–	200	V
I_D	drain current (DC)	$T_{mb} = 25$ °C; $V_{GS} = 10$ V	–	4.8	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C	–	42	W
T_j	junction temperature		–	150	°C
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 2.9$ A	0.7	0.8	Ω

6. Limiting values

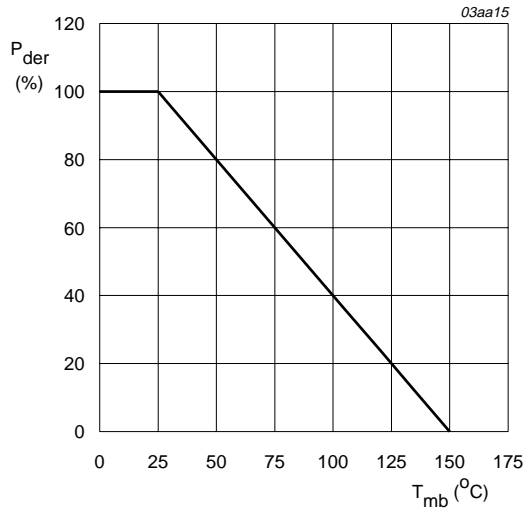
Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$T_j = 25$ to 150 °C	–	200	V
V_{DGR}	drain-gate voltage (DC)	$T_j = 25$ to 150 °C; $R_{GS} = 20$ k Ω	–	200	V
V_{GS}	gate-source voltage (DC)		–	± 20	V
I_D	drain current (DC)	$T_{mb} = 25$ °C; $V_{GS} = 10$ V; Figure 2 and 3	–	4.8	A
		$T_{mb} = 100$ °C; $V_{GS} = 10$ V; Figure 2 and 3	–	3.0	A
I_{DM}	peak drain current	$T_{mb} = 25$ °C; $t_p \leq 10$ μ s	–	19	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; Figure 1	–	42	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C

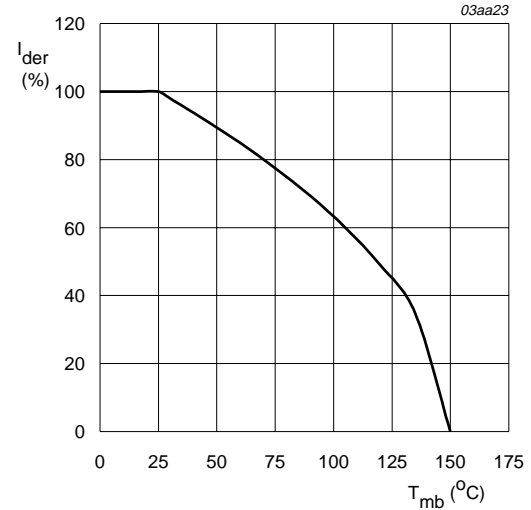
Source-drain (reverse) diode

I_S	source (diode forward) current (DC)	$T_{mb} = 25$ °C	–	4.8	A
I_{SM}	peak (diode forward) source current	$T_{mb} = 25$ °C; $t_p \leq 10$ μ s	–	19	A



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

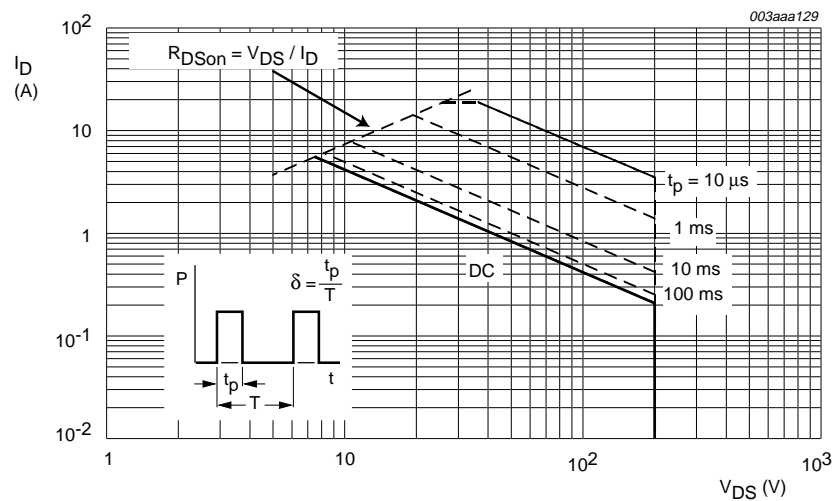
Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

$V_{GS} \geq 10 \text{ V}$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



$T_{mb} = 25^{\circ}C$; I_{DM} is single pulse

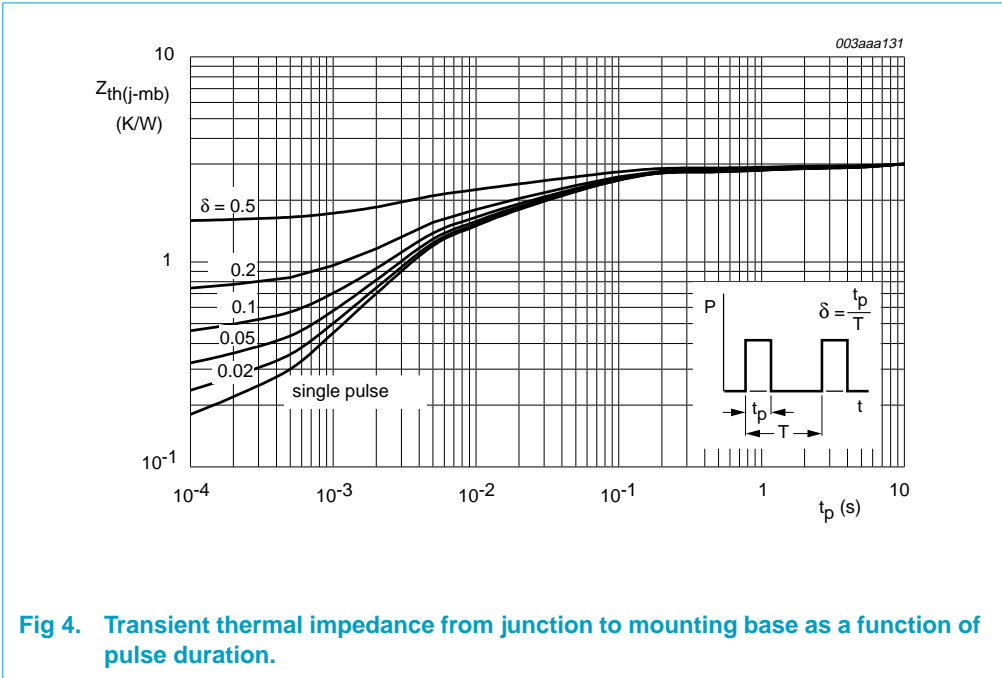
Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	mounted on a metal clad substrate; Figure 4	3	K/W

7.1 Transient thermal impedance

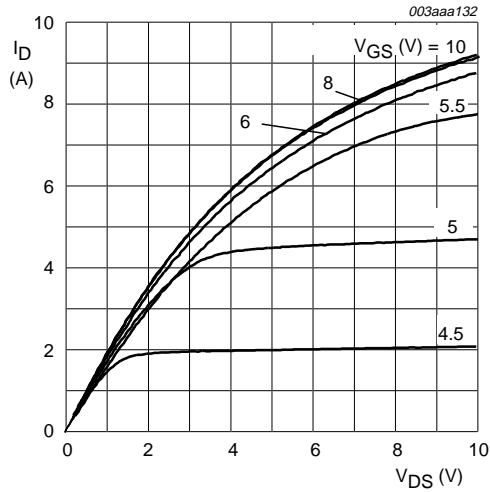


8. Characteristics

Table 5: Characteristics

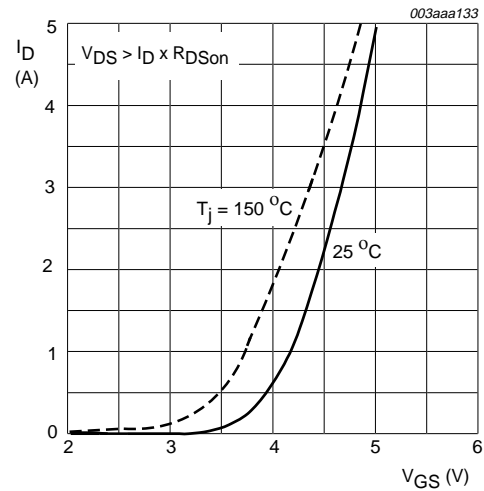
$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V	200	—	—	V
V _{GS(th)}	gate-source threshold voltage	I _D = 250 μA; V _{DS} = V _{GS} ; Figure 9	2	3	4	V
I _{DSS}	drain-source leakage current	V _{DS} = 200 V; V _{GS} = 0 V	—	—	25	μA
		V _{DS} = 160 V; V _{GS} = 0 V; T _j = 125 °C	—	—	250	μA
I _{GSS}	gate-source leakage current	V _{GS} = ±20 V; V _{DS} = 0 V	—	10	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 2.9 A				
		T _j = 25 °C; Figure 7 and 8	—	0.7	0.8	Ω
		T _j = 150 °C; Figure 7 and 8	—	—	1.9	Ω
Dynamic characteristics						
g _{fs}	forward transconductance	V _{DS} = 50 V; I _D = 2.9 A	1.7	—	—	S
Q _{g(tot)}	total gate charge	I _D = 4.8 A; V _{DD} = 160 V; V _{GS} = 10 V; Figure 13	—	10	14	nC
Q _{gs}	gate-source charge		—	1.5	3.0	nC
Q _{gd}	gate-drain (Miller) charge		—	4.0	7.9	nC
C _{iss}	input capacitance		V _{GS} = 0 V; V _{DD} = 25 V; f = 1 MHz; Figure 11	—	280	—
C _{oss}	output capacitance	—		41	—	pF
C _{rss}	reverse transfer capacitance	—		25	—	pF
t _{d(on)}	turn-on delay time	V _{DD} = 100 V; R _D = 20 Ω; V _{GS} = 10 V; R _G = 18 Ω		—	5.0	—
t _r	rise time		—	17	—	ns
t _{d(off)}	turn-off delay time		—	22	—	ns
t _f	fall time		—	18	—	ns
Source-drain (reverse) diode						
V _{SD}	source-drain (diode forward) voltage	I _S = 4.8 A; V _{GS} = 0 V; Figure 12	—	—	1.8	V
t _{rr}	reverse recovery time	I _S = 4.8 A; dI _S /dt = −100 A/μs;	—	85	170	ns
Q _r	recovered charge	V _{GS} = 0 V; V _{DS} = 30 V	—	0.2	1.8	μC



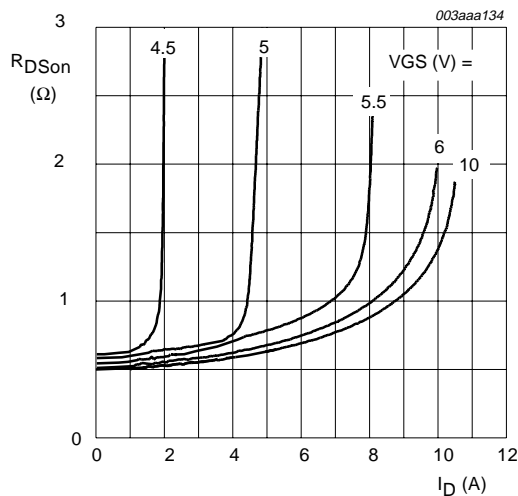
$T_j = 25^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



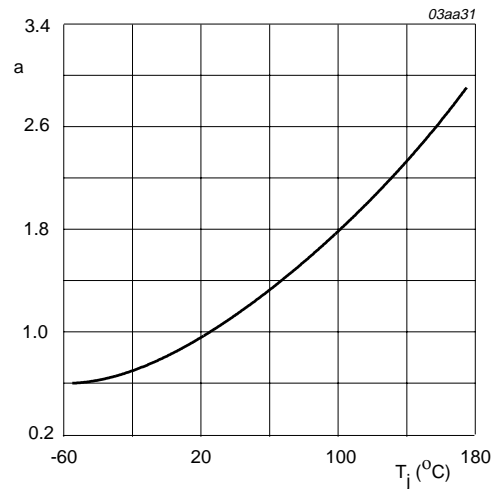
$T_j = 25^\circ\text{C}$ and 150°C ; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



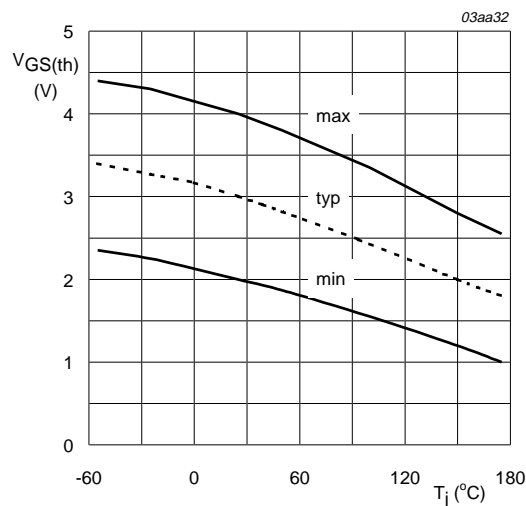
$T_j = 25^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



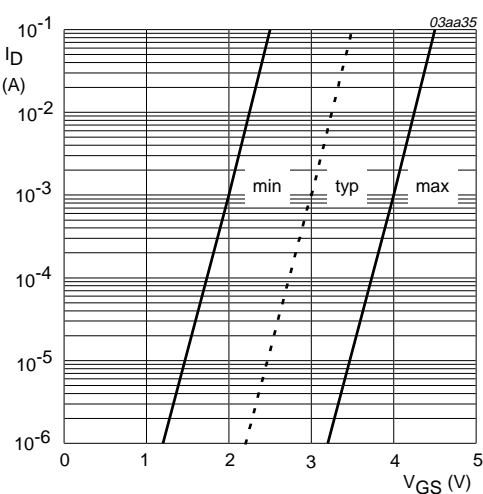
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig 8. Normalized drain source on-state resistance factor as a function of junction temperature.



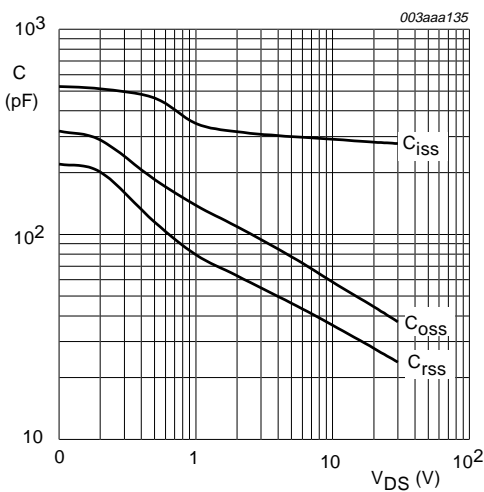
$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



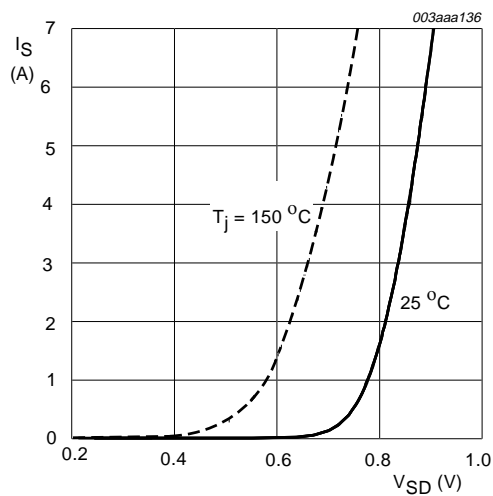
$T_j = 25 \text{ }^\circ\text{C}$; $V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



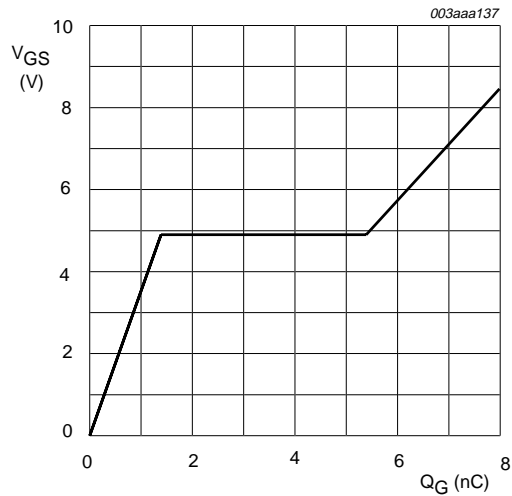
$V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25\text{ }^{\circ}\text{C}$ and $150\text{ }^{\circ}\text{C}$; $V_{GS} = 0\text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$I_D = 4.8\text{ A}$; $V_{DD} = 160\text{ V}$

Fig 13. Gate-source voltage as a function of gate charge; typical values.

9. Package outline

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads
(one lead cropped)

SOT428

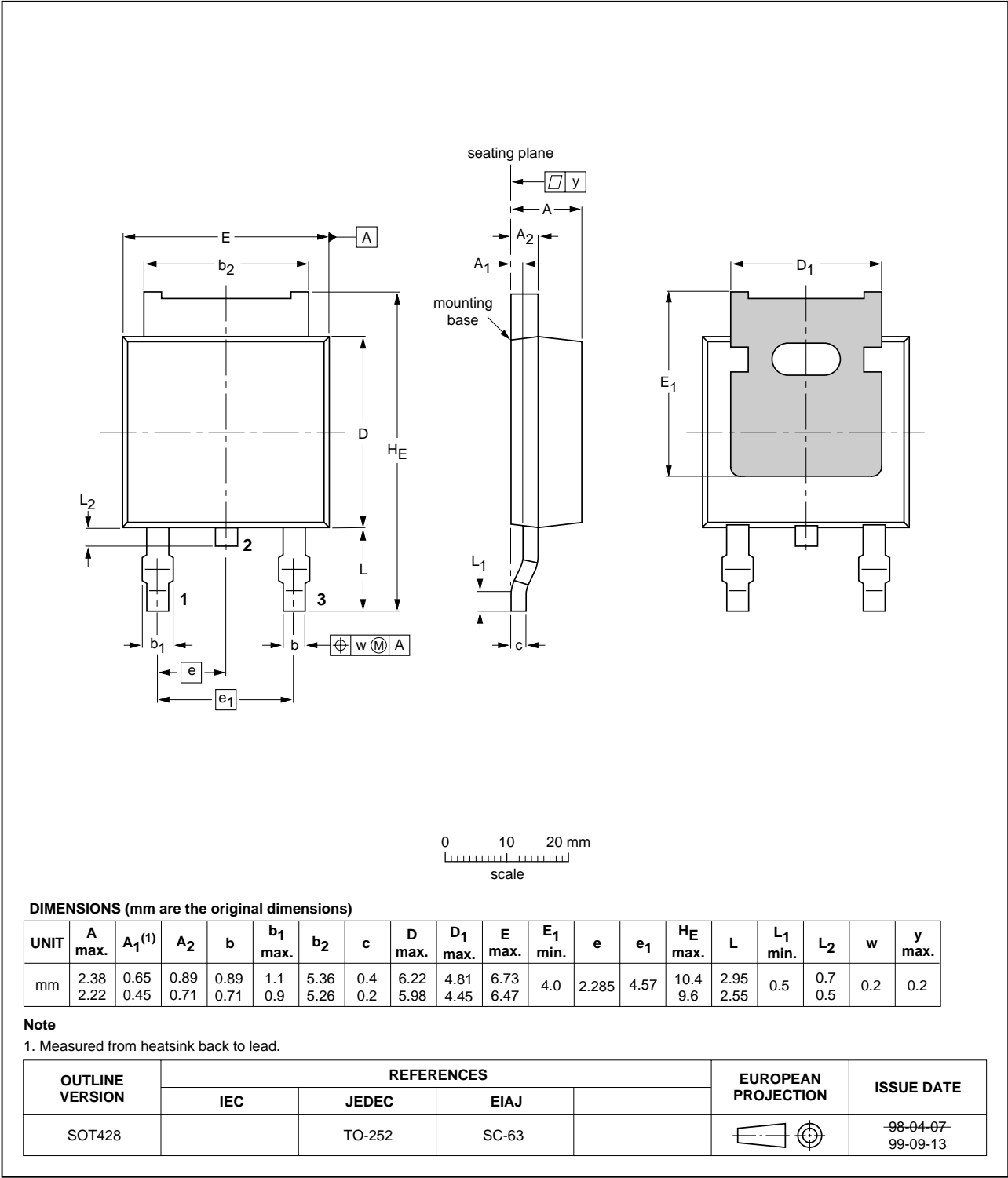


Fig 14. SOT428.

10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20010814	-	Product data; initial version

11. Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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Contents

1 Description 1

2 Features 1

3 Applications 1

4 Pinning information 1

5 Quick reference data 2

6 Limiting values 2

7 Thermal characteristics 4

7.1 Transient thermal impedance 4

8 Characteristics 5

9 Package outline 9

10 Revision history 10

11 Data sheet status 11

12 Definitions 11

13 Disclaimers 11

