Adding hysteresis to comparators

My last column ("Designing with comparators," *EDN*, March 29, 2001, pg 56) discussed basic comparator theory, and this column adds hysteresis to comparators to eliminate multiple switching on the output. Comparators have very high open-loop gain, and, without some type of positive feedback, they have no noise immunity. A slow or dc input signal spends too much time in the comparator threshold, where noise immunity is zero, so any noise on the input signal causes the output voltage to switch almost randomly. Hysteresis is positive feedback that pulls the input signal through the threshold when the output switches, thus preventing multiple switching.

In the circuit in **Figure 1**, R_L (the load resistor) forms a voltage divider with the pullup resistor, R_3; hence, R_L's value must be much greater than R_3 to keep the output voltage high. R_1 and R_2 are the hysteresis components. When V_{IN} transitions from some value greater than V_+ toward some value less than V_+, the output voltage switches from $V_{OUT}=V_{CE}\approx 0$ to $V_{OUT}=V_{CC}-I_LR_3\approx V_{CC}$. The change in the output voltage establishes a current through R_1, and the voltage drop across R_1 increases, causing V_+ to increase. The increase in V_+ pulls the threshold voltage above the input voltage, preventing multiple switching. The following switching equations assume that $R_2>>R_3<<R_L$.

When $V_{IN}>V_{REF}$,

$$V_+=\frac{V_{REF}R_2}{R_1+R_2}+\frac{V_{CES}R_1}{R_1+R_2}.$$

When $V_{IN}<V_{REF}$,

$$V_+=\frac{V_{REF}R_2}{R_1+R_2}+\frac{V_{CC}R_1}{R_1+R_2}.$$

The hysteresis voltage is the difference voltage between the equations, or

$$\Delta V_+=\frac{(V_{CC}-V_{CES})R_1}{R_1+R_2}.$$

HYSTERESIS IS POSITIVE FEEDBACK THAT PULLS THE INPUT SIGNAL THROUGH THE THRESHOLD WHEN THE OUTPUT SWITCHES, THUS PREVENTING MULTIPLE SWITCHING.

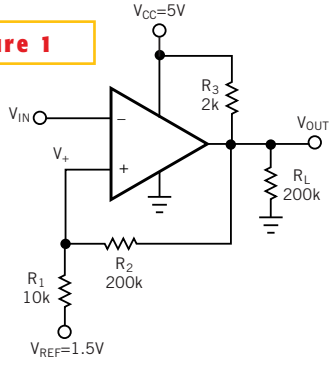
And, when $V_{CES}\approx 0$ and $R_2>>R_1$, you can approximate the hysteresis voltage by

$$\Delta V_+=\frac{V_{CC}R_1}{R_2}.$$

Selecting R_1=10 kΩ, R_2=200 kΩ, R_3=2 kΩ, R_L=200 kΩ, and a TLC-339 comparator yields V_{OUT}=4.95V, V_{CES}=0.2V, and a hysteresis voltage of ΔV_+=0.226V. This hysteresis voltage is unusually large for illustrative purposes. Normally, the amplitude of the noise on the signal determines the hysteresis voltage. A more normal hysteresis voltage is closer to 22.6 mV, and when you increase the value of R_2 to 2 MΩ to reduce the hysteresis, the approximate equation now yields an adequate solution.

Hysteresis prevents multiple switching, but there is no free lunch, because hysteresis introduces a "dead zone" in which the comparator cannot sense an input voltage. The dead zone is the range of voltages within ΔV_+. It is equal to the hysteresis voltage, and it limits the accuracy of the comparator. If the application is unidirectional (the input-voltage direction to the trip point is always from the same direction), the dead zone does not matter, but, in bidirectional applications, such as ADCs, the dead zone limits the converter's ultimate accuracy. When you want to use a string of comparators as an ADC (a flash converter), the dead zone limits the best accuracy the ADC can have. A 9-bit ADC referenced to 10V full-scale has a least significant bit of 19.5 mV. The hysteresis voltage is 22.6 mV, and this dead zone equates to more than a least significant bit for a 9-bit ADC, so the best ADC this comparator circuit can make has 8-bit accuracy.□

Figure 1



R_2 and R_1 add hysteresis to the comparator to prevent multiple switching.

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