Issue date	**: 2005.06.27**
Revision NO.	**: 1.0**

Module:HTG1603A

The instruction of the Module

Design: :

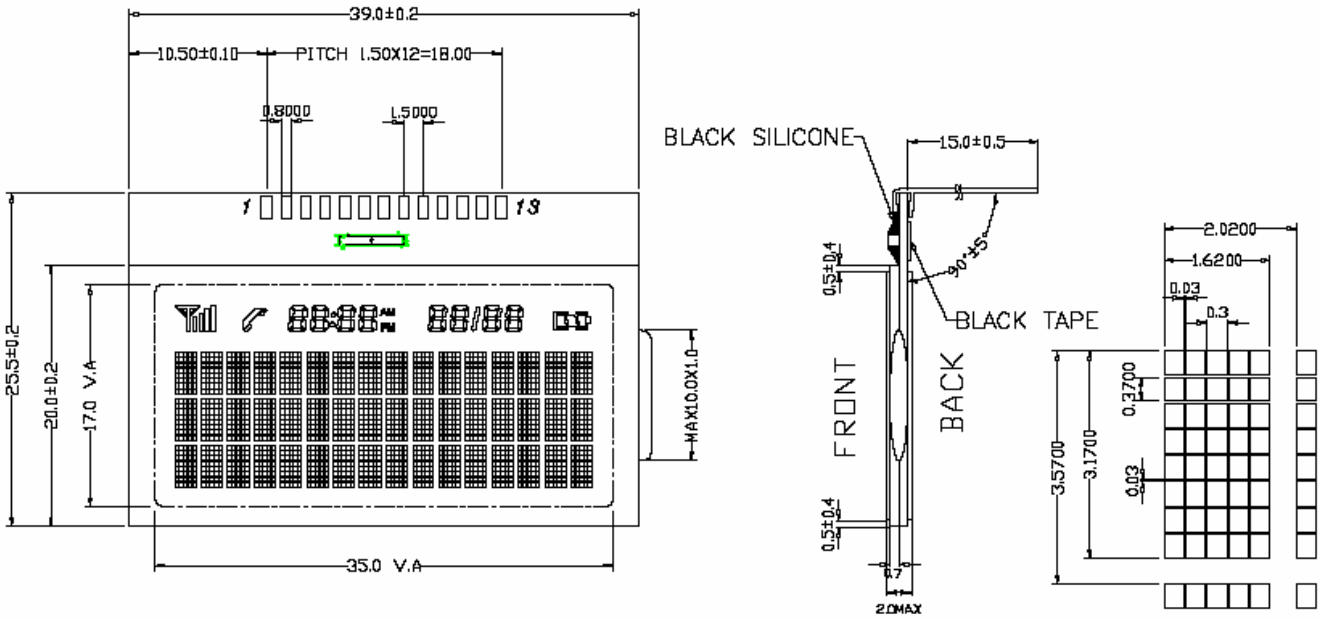
Checkl:

Approval:

Customer:

Customer Approval:

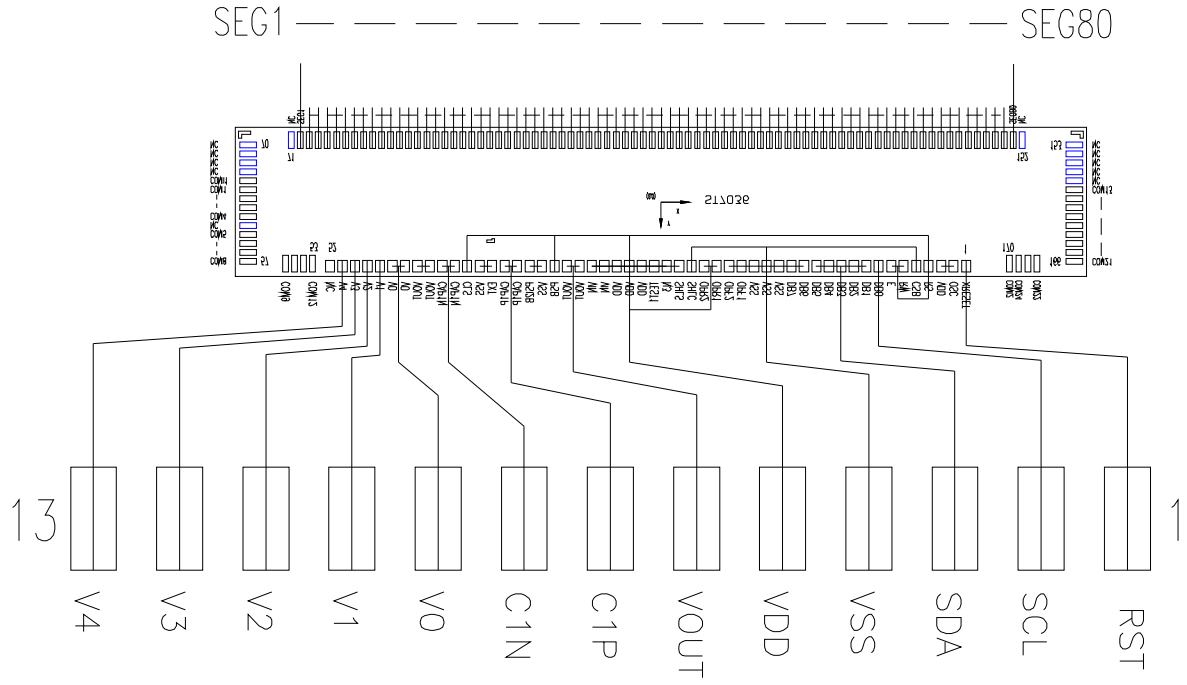
1.GLASS INDTRUCTION



PIN	1	2	3	4	5	6	7
CONNECTION	RST	SCL	SDA	VSS	VDD	VOUT	C1P
PIN	8	9	10	11	12	13	
CONNECTION	C1N	V0	V1	V2	V3	V4	

LCD type:	*STN-YELLOW*	*Drive voltage:*	*3.3V*
Display mode:	*Positive*	*Duty: 1/25*	*Bias: 1/5*
Polarizer type:	*T/H*	*Operating Temp:*	*0°C~60°C*
Viewing Angle:	*6:00*	*Storage Temp:*	*-10°C~60°C*
Connector :	*COG(ST7036)+PIN*		

2.DEFINIENS OF CHIP PIN



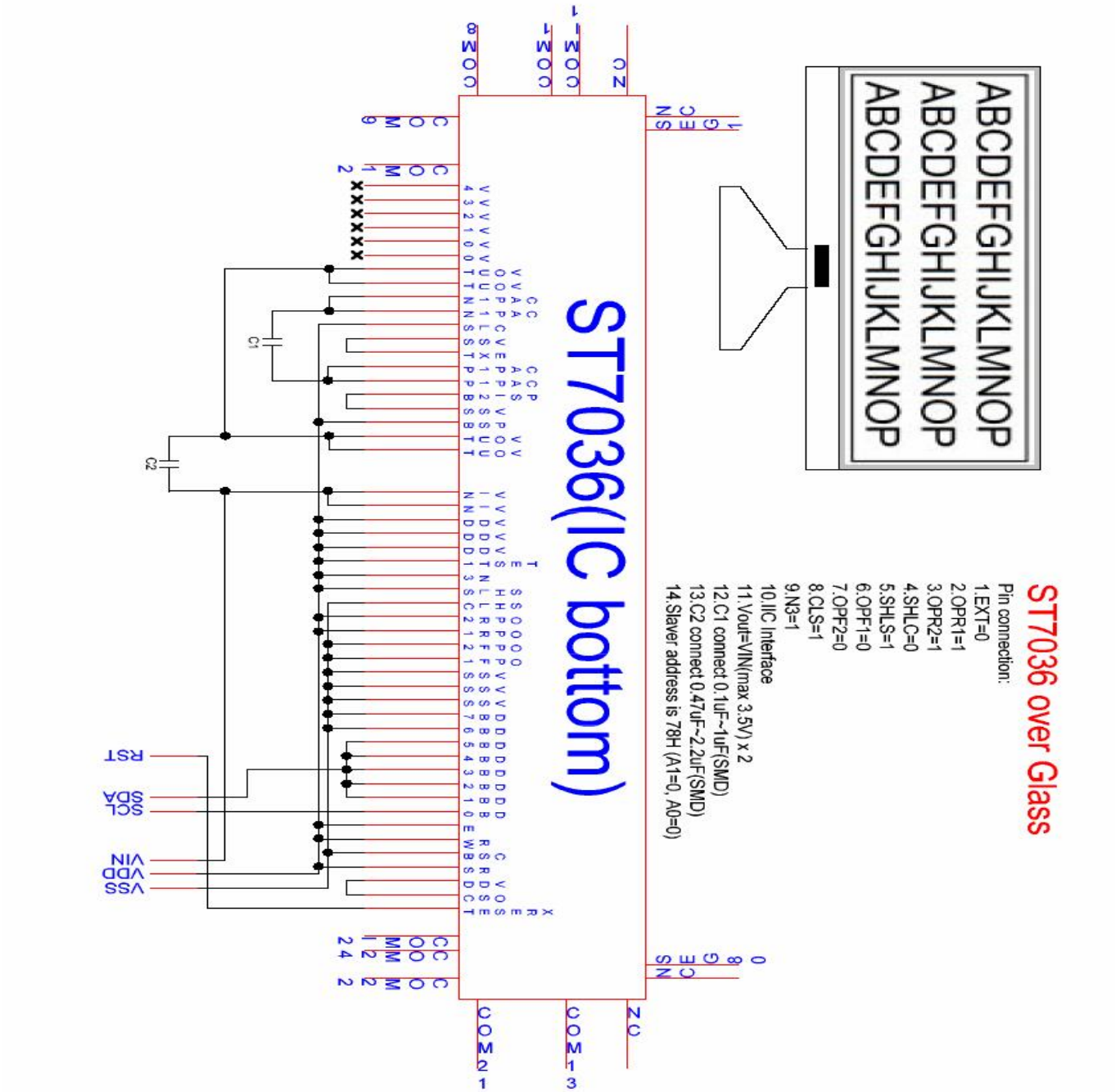
PIN	1	2	3	4	5	6	7
CONNECTION	RST	SCL	SDA	VSS	VDD	VOUT	C1P
PIN	8	9	10	11	12	13	
CONNECTION	C1N	V0	V1	V2	V3	V4	

PIN	CONNECTION	I/O	INTERFACED WITH	FUNCTION
1	RET	I	MPU	EXTERMAL RET PIN
2	SCL	I	MPU	SERIAL CLOCK
3	SDA	I	MPU	INPUT DATA
4	VSS	-	POWER	0V
5	VDD	-	POWER	2.7V TO 5.5V
6	VOUT	-	POWER	DC/DC VOLTAGE CONVERTER
7	C1P	-	POWER	FOR VOLTAGE BOOSTER CIRCLE
8	C1N	-	POWER	EXTEMAL CAP ABOUT 0.1~4.7uF
9~13	VO~V4	-	POWER	POWER SUPPLY FOR LCD DRIVER

3. APPLICATION CIRCUIT

- ***ST7036 over Glass, I²C interface, with booster and follower circuit on***

In I2C application, note that the impedence of SDAs and GNDs should be keep in the POWER PIN LEVEL.



4.FUNCTION DESCRIPTION

- **System Interface**

This chip has all four kinds of interface type with MPU: 4-bit bus, 8-bit bus, serial and fast I^2C interface. 4-bit bus or 8-bit bus is selected by DL bit in the instruction register.

During read or write operation, two 8-bit registers are used. One is data register (DR), the other is instruction register(IR).

The data register(DR) is used as temporary data storage place for being written into or read from DDRAM/CGRAM/ICON RAM, target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically. So to speak, after MPU reads DR data, the data in the next DDRAM/CGRAM/ICON RAM address is transferred into DR automatically. Also after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM/ICON RAM automatically.

The Instruction register(IR) is used only to store instruction code transferred from MPU. MPU cannot use it to read instruction data.

To select register, use RS input pin in 4-bit/8-bit bus mode.

RS	R/W	Operation
L	L	Instruction Write operation (MPU writes Instruction code into IR)
L	H	Read Busy Flag(DB7) and address counter (DB0 ~ DB6)
H	L	Data Write operation (MPU writes data into DR)
H	H	Data Read operation (MPU reads data from DR)

Table 1. Various kinds of operations according to RS and R/W bits.

I^2C interface

It just only could write Data or Instruction to ST7036 by the IIC Interface.
It could not read Data or Instruction from ST7036 (except Acknowledge signal).

SCL: serial clock input
SDA_IN: serial data input
SDA_OUT: acknowledge response output
Slaver address could set from "0111100" to "0111111".

The I^2C interface send RAM data and executes the commands sent via the I^2C Interface. It could send data in to the RAM. The I^2C Interface is two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

BIT TRANSFER
One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Fig.1.

START AND STOP CONDITIONS
Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig.2.

SYSTEM CONFIGURATION
The system configuration is illustrated in Fig.3.
· Transmitter: the device, which sends the data to the bus
· Master: the device, which initiates a transfer, generates clock signals and terminates a transfer
· Slave: the device addressed by a master
· Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message

· Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
· Synchronization: procedure to synchronize the clock signals of two or more devices.

ACKNOWLEDGE

Acknowledge signal (ACK) is not BF signal in parallel interface.
Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. A master receiver must also generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the I^2C Interface is illustrated in Fig.4.

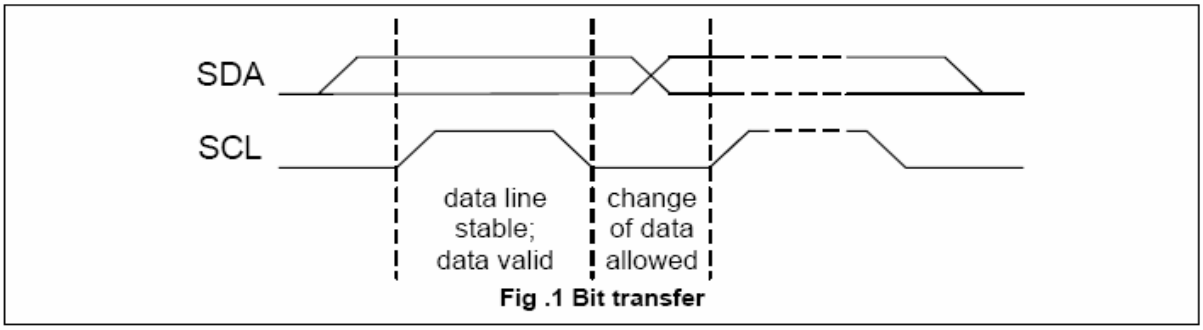


Fig .1 Bit transfer

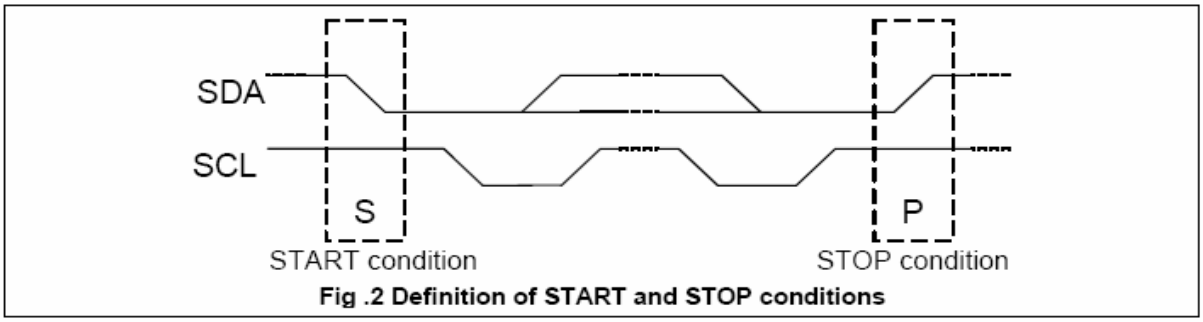


Fig .2 Definition of START and STOP conditions

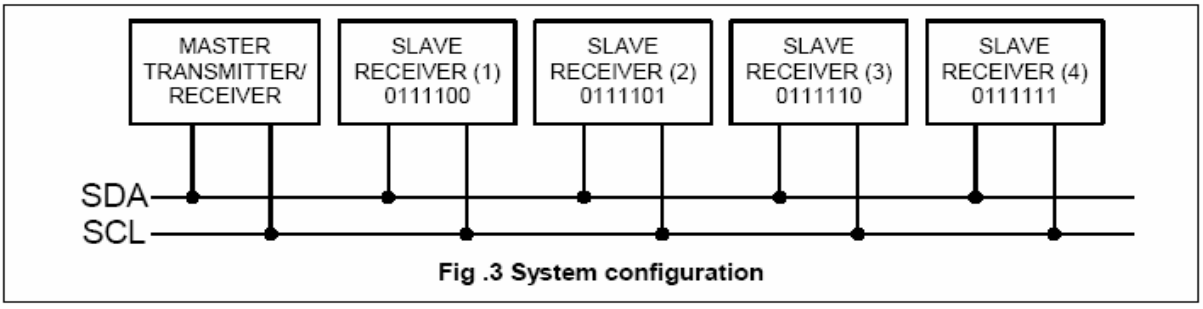


Fig .3 System configuration

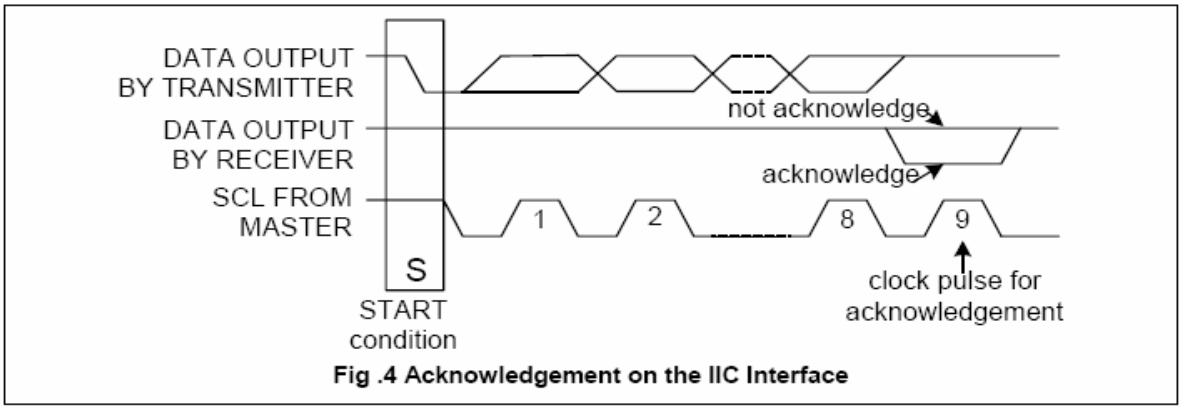


Fig .4 Acknowledgement on the IIC Interface

I²C Interface protocol

The ST7036 supports command, data write addressed slaves on the bus.
Before any data is transmitted on the I²C Interface, the device, which should respond, is addressed first. Four 7-bit slave addresses (0111**100** to 0111**111**) are reserved for the ST7036. The R/W is assigned to 0 for Write only.
The I²C Interface protocol is illustrated in Fig.5.

The sequence is initiated with a START condition (S) from the I²C Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C Interface transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves.
A command word consists of a control byte, which defines Co and RS, plus a data byte.
The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data bytes will follow. The state of the RS bit defines whether the data byte is interpreted as a command or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte, depending on the RS bit setting; either a series of display data bytes or command data bytes may follow. If the RS bit is set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended ST7036i device. If the RS bit of the last control byte is set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the I²C INTERFACE-bus master issues a STOP condition (P).

I²C Interface protocol

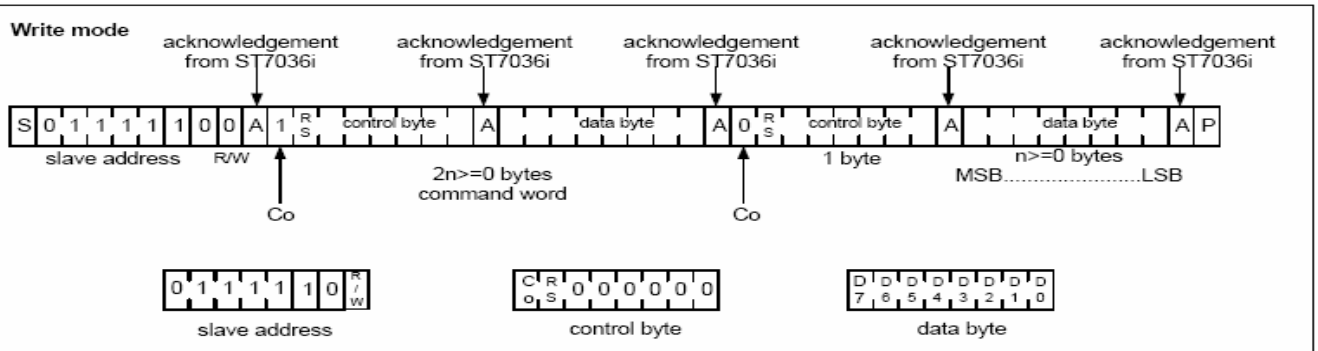


Fig .5 IIC Interface protocol

Co	0	Last control byte to be sent. Only a stream of data bytes is allowed to follow. This stream may only be terminated by a STOP condition.
	1	Another control byte will follow the data byte unless a STOP condition is received.

During write operation, two 8-bit registers are used. One is data register (DR), the other is instruction register(IR).

During write operation, two 8-bit registers are used. One is data register (DR), the other is instruction register(IR).

The data register(DR) is used as temporary data storage place for being written into DDRAM/CGRAM/ICON RAM, target RAM is selected by RAM address setting instruction. Each internal operation, writing into RAM, is done automatically. So to speak, after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM/ICON RAM automatically.

5.CHARACTER GENETATOR

- **Character Generator ROM (CGROM)**

The character generator ROM generates 5 x 8 dot character patterns from 8-bit character codes. It can generate 240/250/248/256 5 x 8 dot character patterns(select by OPR1/2 ITO pin). User-defined character patterns are also available by mask-programmed ROM.

- **Character Generator RAM (CGRAM)**

In the character generator RAM, the user can rewrite character patterns by program. For 5 x 8 dots, eight character patterns can be written.

Write into DDRAM the character codes at the addresses shown as the left column of Table 5 to show the character patterns stored in CGRAM.

See Table 5 for the relationship between CGRAM addresses and data and display patterns. Areas that are not used for display can be used as general data RAM.

- **ICON RAM**

In the ICON RAM, the user can rewrite icon pattern by program.
There are totally 80 dots for icon can be written.
See Table 6 for the relationship between ICON RAM address and data and the display patterns.

- **Timing Generation Circuit**

The timing generation circuit generates timing signals for the operation of internal circuits such as DDRAM, CGROM and CGRAM. RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interfering with each other. Therefore, when writing data to DDRAM, for example, there will be no undesirable interference, such as flickering, in areas other than the display area.

- **LCD Driver Circuit(N3=0)**

LCD Driver circuit has 17 common and 100 segment signals for LCD driving. Data from CGRAM/CGROM/ICON is transferred to 100 bit segment latch serially, and then it is stored to 100 bit shift latch. When each common is selected by 17 bit common register, segment data also output through segment driver from 100 bit segment latch. In case of 1-line display mode, COM1 ~ COM8(with COMI) have 1/9 duty, and in 2-line mode, COM1 ~ COM16(with COMI) have 1/17 duty ratio.

- **LCD Driver Circuit(N3=1)**

LCD Driver circuit has 25 common and 80 segment signals for LCD driving. Data from CGRAM/CGROM/ICON is transferred to 80 bit segment latch serially, and then it is stored to 80 bit shift latch. When each common is selected by 25 bit common register, segment data also output through segment driver from 80 bit segment latch. In case of 3-line display mode, COM1 ~ COM24(with COMI) have 1/25 duty.

COM/SEG Output pins

N3	COMI1	COM [1:8]	SEG [1:5]	SEG [6:10]	SEG [11:90]	SEG [91:96]	SEG [97:100]	COM [9:16]	COMI2
VSS	COMI1	COM [1:8]	SEG [1:5]	SEG [6:10]	SEG [11:90]	SEG [91:96]	SEG [97:100]	COM [9:16]	COMI2
VDD	NC	COM [5:12]	COM[4:1] + COMI1	NC	SEG [1:80]	NC	COM [13:16]	COM [17:24]	COMI2

Table 3. COM/SEG output define

- **Cursor/Blink Control Circuit**

It can generate the cursor or blink in the cursor/blink control circuit. The cursor or the blink appears in the digit at the display data RAM address set in the address counter.

Table 4 Correspondence between Character Codes and Character Patterns

ST7036-0A (ITO option OPR1=1,OPR2=1)

b7-b4 / b3-b0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000																
0001																
0010																
0011																
0100																
0101																
0110																
0111																
1000																
1001																
1010																
1011																
1100																
1101																
1110																
1111																

6. COMMANDS INSTRUCTION

■ Instructions

There are four categories of instructions that:

- **Designate ST7036 functions, such as display format, data length, etc.**
- **Set internal RAM addresses**
- **Perform data transfer with internal RAM**
- **Others**

➢ instruction table at "Normal mode"

(when "EXT" option pin connect to VDD, the instruction set follow below table)

Instruction	Instruction Code										Description	Instruction Execution Time		
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		OSC= 380kHz	OSC= 540kHz	OSC= 700kHz
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC	1.08 ms	0.76 ms	0.59 ms
Return Home	0	0	0	0	0	0	0	0	1	X	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.08 ms	0.76 ms	0.59 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	26.3 µs	18.5 µs	14.3 µs
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	D=1:entire display on C=1:cursor on B=1:cursor position on	26.3 µs	18.5 µs	14.3 µs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	X	X	S/C and R/L: Set cursor moving and display shift control bit, and the direction, without changing DDRAM data.	26.3 µs	18.5 µs	14.3 µs
Function Set	0	0	0	0	1	DL	N	X	X	X	DL: interface data is 8/4 bits N: number of line is 2/1	26.3 µs	18.5 µs	14.3 µs
Set CGRAM	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter	26.3 µs	18.5 µs	14.3 µs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter	26.3 µs	18.5 µs	14.3 µs
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0	0	0
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM)	26.3 µs	18.5 µs	14.3 µs
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM)	26.3 µs	18.5 µs	14.3 µs

Note:
Be sure the ST7036 is not in the busy state (BF = 0) before sending an instruction from the MPU to the ST7036. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself. Refer to Instruction Table for the list of each instruction execution time.

➢ instruction table at "Extension mode"

(when "EXT" option pin connect to Vss, the instruction set follow below table)

Instruction	Instruction Code										Description	Instruction Execution Time		
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		OSC= 380kHz	OSC= 540kHz	OSC= 700kHz
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC	1.08 ms	0.76 ms	0.59 ms
Return Home	0	0	0	0	0	0	0	0	1	x	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.08 ms	0.76 ms	0.59 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	26.3 µs	18.5 µs	14.3 µs
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	D=1:entire display on C=1:cursor on B=1:cursor position on	26.3 µs	18.5 µs	14.3 µs
Function Set	0	0	0	0	1	DL	N	DH	IS2	IS1	DL: interface data is 8/4 bits N: number of line is 2/1 DH: double height font IS[2:1]: instruction table select	26.3 µs	18.5 µs	14.3 µs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter	26.3 µs	18.5 µs	14.3 µs
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0	0	0
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM/ICONRAM)	26.3 µs	18.5 µs	14.3 µs
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM/ICONRAM)	26.3 µs	18.5 µs	14.3 µs

Instruction table 0(IS[2:1]=[0,0])														
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	X	X	S/C and R/L: Set cursor moving and display shift control bit, and the direction, without changing DDRAM data.	26.3 μs	18.5 μs	14.3 μs
Set CGRAM	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter	26.3 μs	18.5 μs	14.3 μs

Instruction table 1(IS[2:1]=[0,1])														
Bias Set	0	0	0	0	0	1	BS	1	0	FX	BS=1:1/4 bias BS=0:1/5 bias FX: fixed on high in 3-line application and fixed on low in other applications.	26.3 μs	18.5 μs	14.3 μs
Set ICON Address	0	0	0	1	0	0	AC3	AC2	AC1	AC0	Set ICON address in address counter.	26.3 μs	18.5 μs	14.3 μs
Power/ICON Control/ Contrast Set	0	0	0	1	0	1	Ion	Bon	C5	C4	Ion: ICON display on/off Bon: set booster circuit on/off C5,C4: Contrast set for internal follower mode.	26.3 μs	18.5 μs	14.3 μs
Follower Control	0	0	0	1	1	0	Fon	Rab 2	Rab 1	Rab 0	Fon: set follower circuit on/off Rab2~0: select follower amplified ratio.	26.3 μs	18.5 μs	14.3 μs
Contrast Set	0	0	0	1	1	1	C3	C2	C1	C0	Contrast set for internal follower mode.	26.3 μs	18.5 μs	14.3 μs

Instruction table 2(IS[2:1]=[1,0])														
Double Height Position Select	0	0	0	0	0	1	UD	X	x	x	UD: Double height position select	26.3 μs	18.5 μs	14.3 μs
Reserved	0	0	0	1	X	X	X	X	X	X	Do not use (reserved for test)	26.3 μs	18.5 μs	14.3 μs

Instruction table 3(IS[2:1]=[1,1]):Do not use (reserved for test)

- **Clear Display**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status, namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

- **Return Home**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	X

Return Home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM does not change.

- **Entry Mode Set**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	S

Set the moving direction of cursor and display.

➢ **I/D : Increment / decrement of DDRAM address (cursor or blink)**
When I/D = "High", cursor/blink moves to right and DDRAM address is increased by 1.
When I/D = "Low", cursor/blink moves to left and DDRAM address is decreased by 1.
* CGRAM operates the same as DDRAM, when read from or write to CGRAM.

➢ **S: Shift of entire display**
When DDRAM read (CGRAM read/write) operation or S = "Low", shift of entire display is not performed. I
S = "High" and DDRAM write operation, shift of entire display is performed according to I/D value (I/D = "1" : shift left, I/D = "0" : shift right).

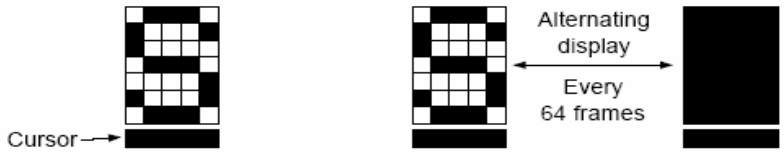
S	I/D	Description
H	H	Shift the display to the left
H	L	Shift the display to the right

- **Display ON/OFF**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

- **D : Display ON/OFF control bit**
  When D = "High", entire display is turned on.
  When D = "Low", display is turned off, but display data is remained in DDRAM.
- **C : Cursor ON/OFF control bit**
  When C = "High", cursor is turned on.
  When C = "Low", cursor is disappeared in current display, but I/D register remains its data.
- **B : Cursor Blink ON/OFF control bit**
  When B = "High", cursor blink is on, that performs alternate between all the high data and display character at the cursor position.
  When B = "Low", blink is off.



- **Cursor or Display Shift**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	X	X

- **S/C: Screen/Cursor select bit**
  When S/C="High", Screen is controlled by R/L bit.
  When S/C="Low", Cursor is controlled by R/L bit.
- **R/L: Right/Left**
  When R/L="High", set direction to right.
  When R/L="Low", set direction to left.

Without writing or reading of display data, shift right/left cursor position or display. This instruction is used to correct or search display data. During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line. Note that display shift is performed simultaneously in all the line. When displayed data is shifted repeatedly, each line shifted individually. When display shift is performed, the contents of address counter are not changed.

S/C	R/L	Description	AC Value
L	L	Shift cursor to the left	AC=AC-1
L	H	Shift cursor to the right	AC=AC+1
H	L	Shift display to the left. Cursor follows the display shift	AC=AC
H	H	Shift display to the right. Cursor follows the display shift	AC=AC

- **Function Set**

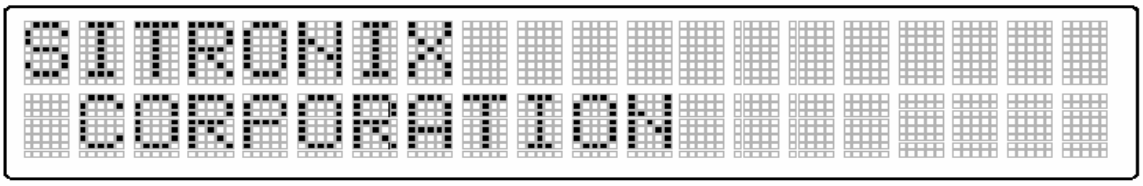
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	DH	IS2	IS1

➢ **DL : Interface data length control bit**
When DL = "High", it means 8-bit bus mode with MPU.
When DL = "Low", it means 4-bit bus mode with MPU. So to speak, DL is a signal to select 8-bit or 4-bit bus mode.
When 4-bit bus mode, it needs to transfer 4-bit data by two times.

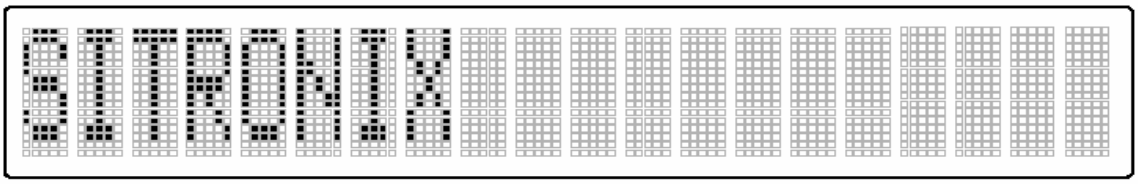
➢ **N : Display line number control bit**
When N = "High", 2-line display mode is set.
When N = "Low", it means 1-line display mode.
When "N3" option pin connect to VDD, N must set "N=1".

➢ **DH : Double height font type control bit**
When DH = " High " and N= "Low", display font is selected to double height mode(5x16 dot),RAM address can only use 00H~27H.
When DH= "High" and N= "High", it is forbidden.
When DH = " Low ", display font is normal (5x8 dot).

N	DH	EXT option pin connect to high		EXT option pin connect to low	
		Display Lines	Character Font	Display Lines	Character Font
L	L	1	5x8	1	5x8
L	H	1	5x8	1	5x16
H	L	2	5x8	2	5x8
H	H	2	5x8	Forbidden	



2 line mode normal display (DH=0/N=1)



1 line mode with double height font (DH=1/N=0)

- **Set CGRAM Address**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC.
This instruction makes CGRAM data available from MPU.

- **Set DDRAM Address**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC.
This instruction makes DDRAM data available from MPU.
When 1-line display mode (N = 0), DDRAM address is from "00H" to "4FH".
In 2-line display mode (N = 1), DDRAM address in the 1st line is from "00H" to "27H", and
DDRAM address in the 2nd line is from "40H" to "67H".
In 3-line display mode (N3=1, N=1), DDRAM address in the 1st line is from “00H” to “OFH”, DDRAM in the 2nd line is from “10H” to “1FH”, and DDRAM in the 3rd line is from “20H” to “2FH”.

- **Read Busy Flag and Address**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

When BF = “High”, indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted.
The address Counter (AC) stores DDRAM/CGRAM addresses, transferred from IR.
After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1.

- **Write Data to CGRAM,DDRAM or ICON RAM**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to **CGRAM,DDRAM or ICON RAM**
The selection of RAM from DDRAM, CGRAM or ICON RAM, is set by the previous address set instruction : DDRAM address set, CGRAM address set, ICON RAM address set. RAM set instruction can also determine the AC
direction to RAM.
After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

- **Read Data from CGRAM,DDRAM or ICON RAM**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM./ICON RAM

The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is
performed before this instruction, the data that read first is invalid, because the direction of AC is
determined. If you read RAM data several times without RAM address set instruction before read operati
you can get correct RAM data from the second, but the first data would be incorrect, because there is no ti
margin to transfer RAM data.

- **Bias Set**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	BS	1	0	FX

- **BS: bias selection**
  When BS="High", the bias will be 1/4
  When BS="Low", the bias will be 1/5
  BS will be invalid when external bias resistors are used(OPF1=1,OPF2=1)
- **FX:** must be fixed on high in 3-line application and fixed on low in other applications.

- **Set ICON RAM address**

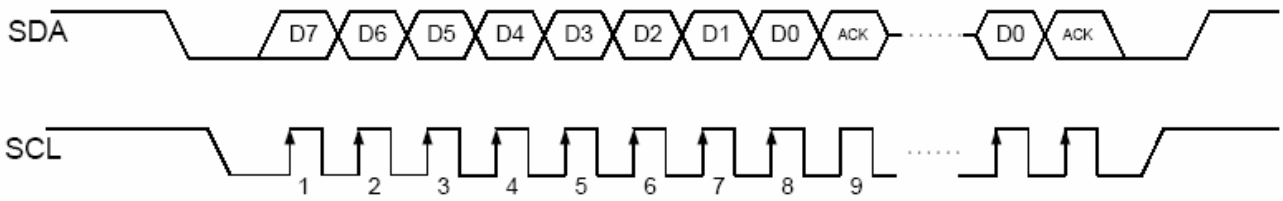
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	AC3	AC2	AC1	AC0

Set ICON RAM address to AC.
This instruction makes ICON data available from MPU.
When IS=1 at Extension mode,
The ICON RAM address is from "00H" to "0FH".

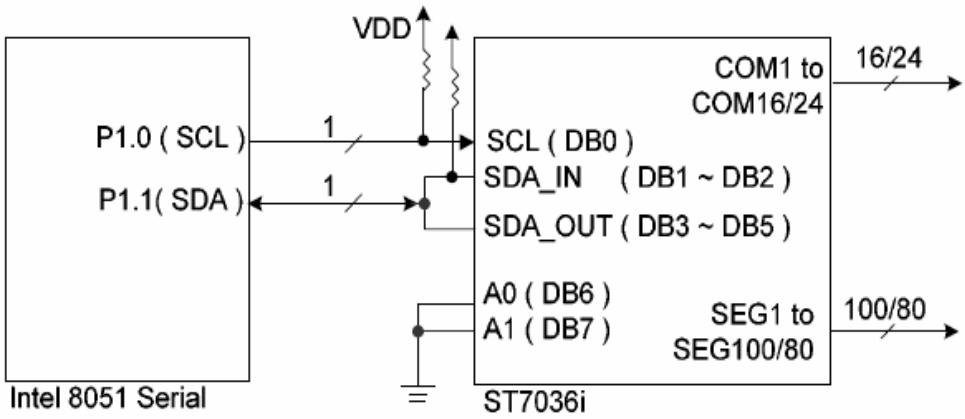
7.INTERFACE DESCRIPTION

- For I²C interface data, all eight bus lines (DB0 to DB7) are used.

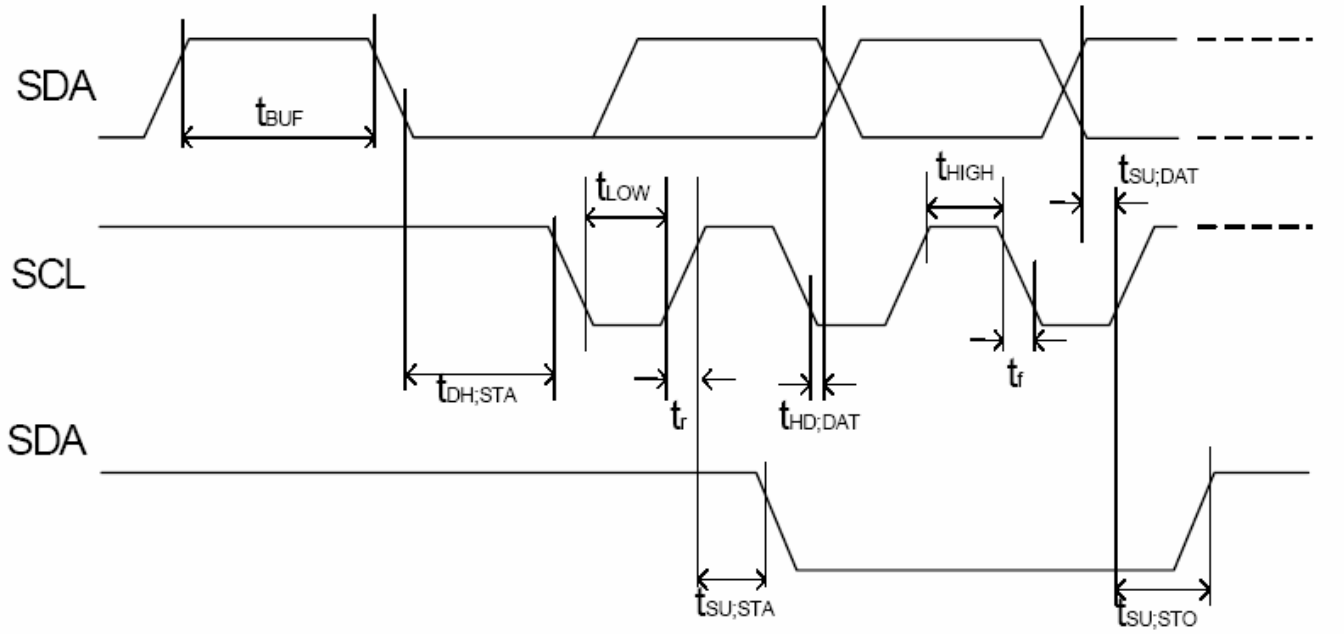
➢ **Example of timing sequence**



➢ **Intel 8051 interface (I²C interface)**



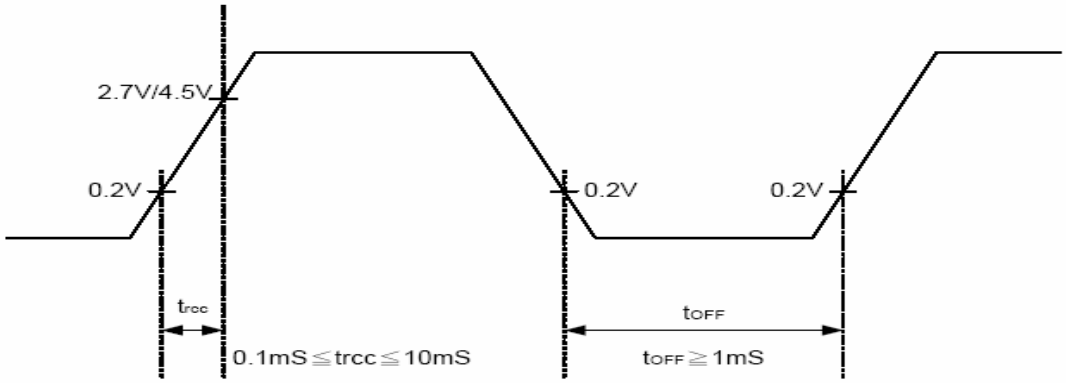
- **I2C interface**



(Ta = 25°C)

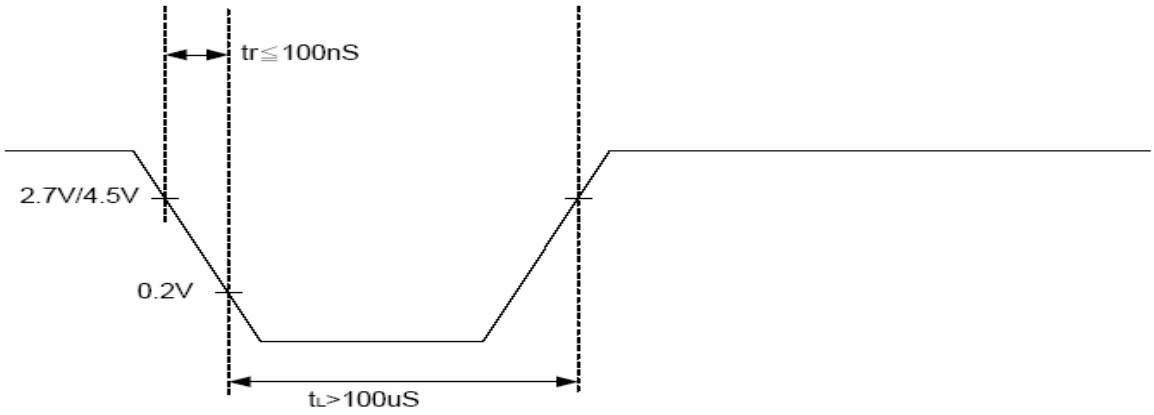
Item	Signal	Symbol	Condition	VDD=2.7 to 4.5V Rating		VDD=4.5 to 5.5V Rating		Units
				Min.	Max.	Min.	Max.	
SCL clock frequency	SCL	f_{SCLK}	—	DC	300K	DC	400	kHz
SCL clock low period		t_{LOW}		2.5	—	1.3	—	µs
SCL clock high period		t_{HIGH}		0.6	—	0.6	—	
Data set-up time	SDA	$t_{SU;DAT}$	—	1800	—	700	—	ns
Data hold time		$t_{HD:DAT}$		0	—	0	0.5	µs
SCL,SDA rise time	SCL, SDA	t_r	—	20+0.1C_b	300	20+0.1C_b	300	ns
SCL,SDA fall time		t_f		20+0.1C_b	300	20+0.1C_b	300	
Capacitive load represent by each bus line		C_b	—	—	400	—	400	pf
Setup time for a repeated START condition	SDA	$t_{SU;STA}$	—	0.6	—	0.6	—	µs
Start condition hold time		$t_{HD;STA}$	—	1.8	—	1.0	—	µs
Setup time for STOP condition		$t_{SU;STO}$	—	0.6	—	0.6	—	µs
Bus free time between a Stop and START condition	SCL	t_{BUF}	—	1.3	—	1.3	—	µs

- **Internal Power Supply Reset**



Notes:
- tOFF compensates for the power oscillation period caused by momentary power supply oscillations.
- Specified at 4.5V for 5V operation, and at 2.7V for 3V operation.
- For if 2.7V/4.5V is not reached during 3V/5V operation, internal reset circuit will not operate normally.

- **Hardware reset(XRESET)**



8.ELECTRICAL SPECS

■ Absolute Maximum Ratings

Characteristics	Symbol	Value
Power Supply Voltage	VDD	-0.3 to +7.0
LCD Driver Voltage	V_{LCD}	7.0- Vss to -0.3+Vss
Input Voltage	V_{IN}	-0.3 to VDD+0.3
Operating Temperature	T_A	-40°C to + 90°C
Storage Temperature	T_{STO}	-55°C to + 125°C

■ DC Characteristics

(TA = 25℃ , VDD = 2.7 V)

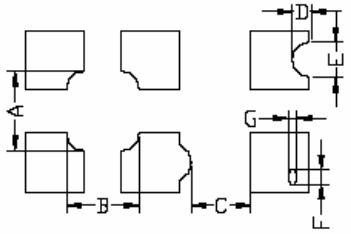
Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
VDD	Operating Voltage	-	2.7	-	4.5	V
V_{LCD}	LCD Voltage	V0-Vss	2.7	-	7.0	V
VIN	Power Supply	-	-	-	3.5	V
I_{CC}	Power Supply Current	VDD=3.0V (Use internal booster/follower circuit)	-	160	230	uA
V_{IH1}	Input High Voltage (Except OSC1)	-	0.7 VDD	-	VDD	V
V_{IL1}	Input Low Voltage (Except OSC1)	-	- 0.3	-	0.8	V
V_{IH2}	Input High Voltage (OSC1)	-	0.7 VDD	-	VDD	V
V_{IL2}	Input Low Voltage (OSC1)	-	-	-	0.2 VDD	V
V_{OH}	Output High Voltage (DB0 - DB7)	I_{OH} = -1.0mA	0.7 VDD	-	-	V
V_{OL}	Output Low Voltage (DB0 - DB7)	I_{OL} = 1.0mA	-	-	0.8	V
R_{COM}	Common Resistance	V_{LCD} = 4V, I_d = 0.05mA	-	2	20	KΩ
R_{SEG}	Segment Resistance	V_{LCD} = 4V, I_d = 0.05mA	-	2	30	KΩ
I_{LEAK}	Input Leakage Current	V_{IN} = 0V to VDD	-1	-	1	μA
I_{PUP}	Pull Up MOS Current	VDD = 3V	20	30	40	μA
fOSC	Oscillation frequency	VDD = 3V,1/17duty	350	540	1100	kHz

■ DC Characteristics

(TA = 25℃, VDD = 4.5 V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
VDD	Operating Voltage	-	4.5	-	5.5	V
V_{LCD}	LCD Voltage	V0-Vss	2.7	-	7.0	V
VIN	Power Supply	-	-	-	3.5	V
I_{CC}	Power Supply Current	VDD=5.0V (Use internal booster/follower circuit)	-	240	340	μA
V_{IH1}	Input High Voltage (Except OSC1)	-	0.7 VDD	-	VDD	V
V_{IL1}	Input Low Voltage (Except OSC1)	-	-0.3	-	0.8	V
V_{IH2}	Input High Voltage (OSC1)	-	0.7 VDD	-	VDD	V
V_{IL2}	Input Low Voltage (OSC1)	-	-	-	1.0	V
V_{OH}	Output High Voltage (DB0 - DB7)	I_{OH} = -1.0mA	0.8 VDD	-	VDD	V
V_{OL}	Output Low Voltage (DB0 - DB7)	I_{OL} = 1.0mA	-	-	0.8	V
R_{COM}	Common Resistance	V_{LCD} = 4V, I_d = 0.05mA	-	2	20	KΩ
R_{SEG}	Segment Resistance	V_{LCD} = 4V, I_d = 0.05mA	-	2	30	KΩ
I_{LEAK}	Input Leakage Current	V_{IN} = 0V to VDD	-1	-	1	μA
I_{PUP}	Pull Up MOS Current	VDD = 5V	65	95	125	μA
fOSC	Oscillation frequency	VDD = 5V,1/17duty	350	540	1100	kHz

Inspection Standards

Item	Criterion for defects	Defect type
1) Display on inspection	(1) Non display (2) Vertical line is deficient (3) Horizontal line is deficient (4) Cross line is deficient	Major
2) Black / White spot	Size Φ(mm) Acceptable number Φ≤0.3 Ignore (note) 0.3<Φ≤0.45 3 0.45<Φ≤0.6 1 0.6<Φ 0	Minor
3) Black / White line	Length (mm) Width (mm) Acceptable number L≤10 W≤0.03 Ignore 5.0≤L≤10 0.03<W≤0.04 3 5.0≤L≤10 0.04<W≤0.05 2 1.0≤L≤10 0.05<W≤0.06 2 1.0≤L≤10 0.06<W≤0.08 1 L≤10 0.08<W follows 2) point defect Defects separate with each other at an interval of more than 20mm	Minor
4) Display pattern	 $\frac{A+B}{2}\leq 0.28$ 0<C $\frac{D+E}{2}\leq 0.25$ $\frac{F+G}{2}\leq 0.25$ Note: 1) Up to 3 damages acceptable 2) Not allowed if there are two or more pinholes every three-fourth inch.	Minor
5) Spot-like contrast irregularity	Size Φ(mm) Acceptable Number Φ≤0.7 Ignore (note) 0.7<Φ≤1.0 3 1.0<Φ≤1.5 1 1.5<Φ 0 Note: 1) Conformed to limit samples. 2) Intervals of defects are more than 30mm.	Minor
6) Bubbles in polarizer	Size Φ(mm) Acceptable Number Φ≤0.4 Ignore (note) 0.4<Φ≤0.65 2 0.65<Φ≤1.2 1 1.2<Φ 0	Minor
7) Scratches and dent on the polarizer	Scratches and dent on the polarizer shall be in the accordance with "2) Black/white spot", and "3) Black/White line".	Minor
8) Stains on the surface of LCD panel	Stains which cannot be removed even when wiped lightly with a soft cloth or similar cleaning.	Minor
9) Rainbow color	No rainbow color is allowed in the optimum contrast on state within the active area.	Minor
10) Viewing area encroachment	Polarizer edge or line is visible in the opening viewing area due to polarizer shortness or sealing line.	Minor
11) Bezel appearance	Rust and deep damages that are visible in the bezel are rejected.	Minor
12) Defect of land surface contact	Evident crevices that are visible are rejected.	Minor
13) Parts mounting	(1) Failure to mount parts (2) Parts not in the specifications are mounted (3) For example: Polarity is reversed, HSC or TCP falls off.	Minor
14) Part alignment	(1) LSI, IC lead width is more than 50% beyond pad outline. (2) More than 50% of LSI, IC leads is off the pad outline.	Minor
15) Conductive foreign matter (solder ball, solder hips)	(1) 0.45<Φ, N≥1 (2) 0.3<Φ≤0.45, N≥1, Φ: Average diameter of solder ball (unit: mm) (3) 0.5<L, N≥1, L: Average length of solder chip (unit: mm)	Minor
16) Bezel flaw	Bezel claw missing or not bent	Minor
17) Indication on name plate (sampling indication label)	(1) Failure to stamp or label error, or not legible.(all acceptable if legible) (2) The separation is more than 1/3 for indication discoloration, in which the characters can be checked.	Minor