Question 1 (COMPULSORY)

Considering the two-stage amplifier circuit below :

a) Give the two transistor connection configurations. (10 marks)

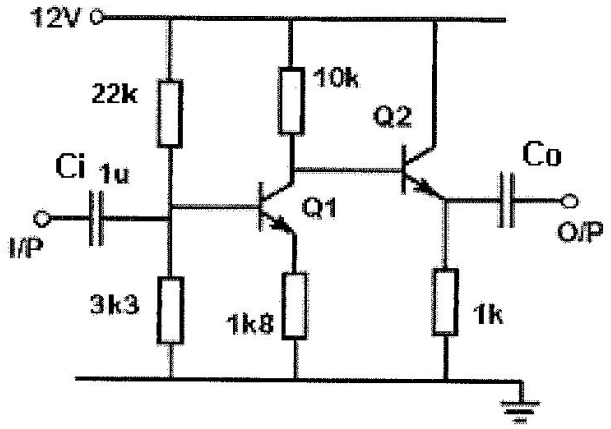
b) Calculate the quiescent voltage values of V_{CE} for both transistors, Q1 and Q2 (30 marks)

c) Determine the quiescent base current of Q2 (I_{BQ1}) (20 marks)

d) For an input signal of 10kHz, assuming that the capacitor impedances may be considered to be very small ($\approx 0\Omega$), determine the input resistance of the amplifier. (40 marks)

e) Determine the critical low frequency breakpoints produced by the input and ouput capacitors Ci and Co for the case of a 1kΩ load. (50 marks)

(Let $\beta_{Q1} = \beta_{Q2} = 100$ and $h_{FE} = h_{fe} = \beta$, Co = 1uF)

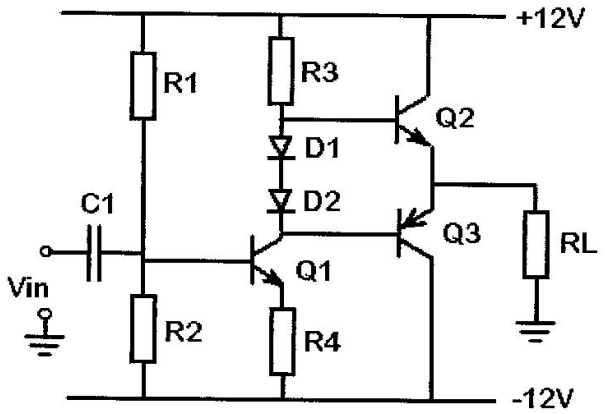


Question 2

(a) For the power amplifier below, determine the voltage gain (assuming that the capacitors are short-circuits at the small signal frequencies of operation). Assume a 1k load RL is connected to the output.

(Note: [$h_{fe} = h_{FE} = \beta = 200$ for Q1, 2 & 3]

- The d.c. bias conditions need to be established first to attain the necessary a.c. parameters.
- The output stage and the load may be converted to an equivalent resistance connected to the collector of Q1.)



Let R1 = 22k, R2 = 2.2k, R3 = 1.5k, R4 = 120Ω and C1 = 1uF. (110 marks)

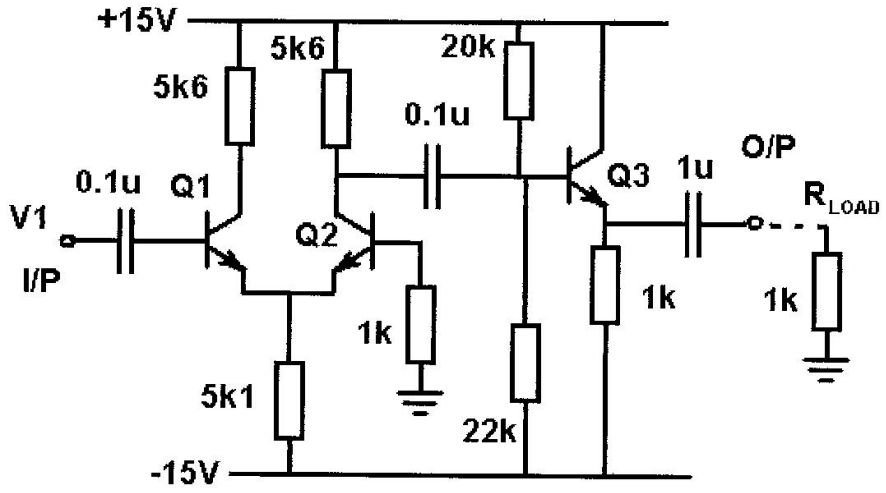
(b) Calculate the maximum input signal voltage (rms) possible without any distortion of the output sinusoidal signal for a frequency of 10kHz. (40 marks)

Question 1 (COMPULSORY)

Considering the two-stage amplifier circuit below :

a) Give the two transistor connection configurations and their purpose in this circuit. (10 marks)
b) Calculate the biased output voltage (quiescent) at the emitter of Q3. (30 marks)
c) Determine the value of h_{ie} for Q1. (20 marks)
d) For an input signal of 2kHz, assuming that the capacitor impedances may be considered to be very small ($\approx 0\Omega$), determine the input resistance of the amplifier. (30 marks)
e) With an output load of 1kΩ connected, determine the overall signal voltage gain of the amplifier, from I/P to O/P, in dB. (50 marks)
f) For an input voltage of 0.5Vp calculate the output power into the 1kΩ load. (10 marks)

(Let $\beta_{Q1} = 200$, $\beta_{Q2} = 60$ and $h_{FE} = h_{fe} = \beta$)



Question 2

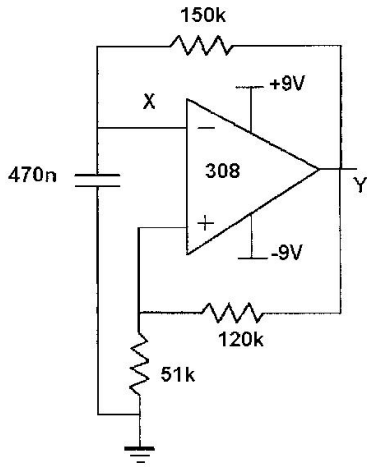
Considering the circuit diagram above in Question 1:

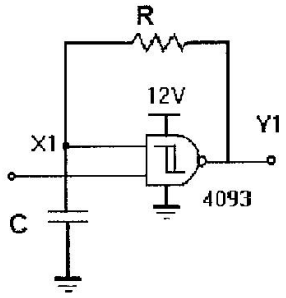
a) Determine the biased (quiescent) collector voltage for Q2, (20 marks)
b) Calculate the CMRR (dB) for the Q1, Q2 section of the circuit. (20 marks)
c) What is the quiescent power being dissipated by Q3 ? (20 marks)

With an input source with a resistance of 0Ω, and the output load of 1kΩ connected, determine the frequency breakpoints contributions of each capacitor to the overall frequency response for the amplifier. (90 marks)

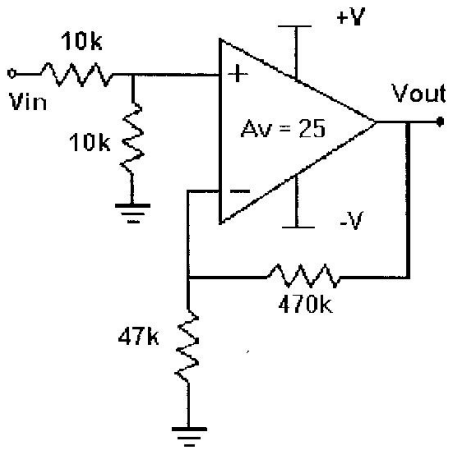
Question 3

a) For the two Schmitt oscillators below, by sketched plots, compare the waveforms of X : X1 and Y : Y1. (Use the same time axis for the plot comparisons.) Assume that both circuits timing periods are effectively the time constant t = RC. Begin the plots from a power-up condition where the voltages across the capacitors are zero. Indicate on the sketches any important parameter values. You may assume that the two thresholds for the 4093 are 4V and 8V. (Let **R** = 150kΩ and **C** = 470nF.) (90 marks)



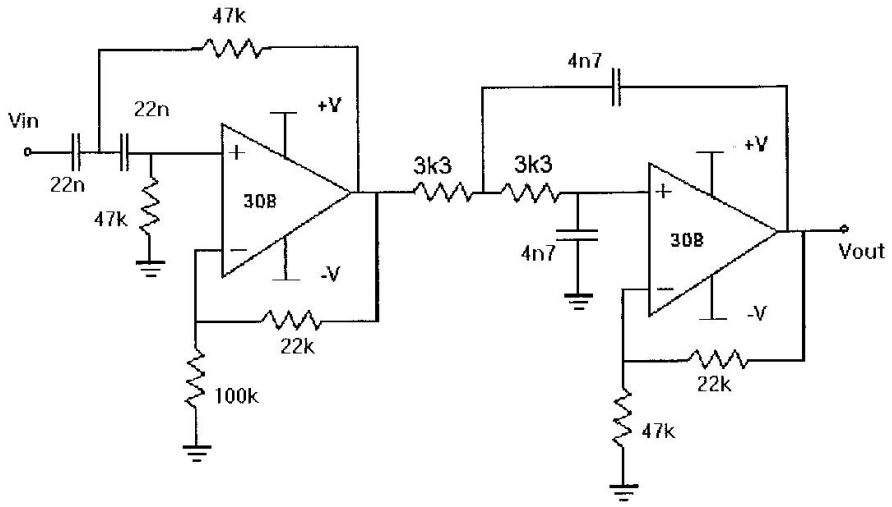


b) Determine the RMS output voltage of the amplifier below, if a 200mV (peak-to-peak) signal is applied to the input. (Assume the amplifier has high input resistance.) (60 marks)



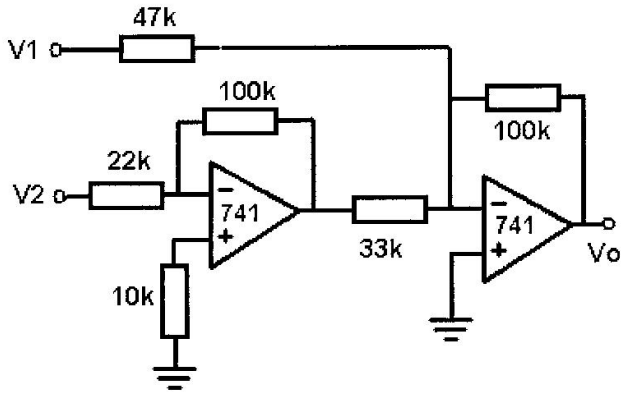
Question 4

a) Sketch the approximate gain vs frequency (for Vout/Vin) of the active filter network below. Indicate on the plot the important frequencies, roll-off slopes and gains.



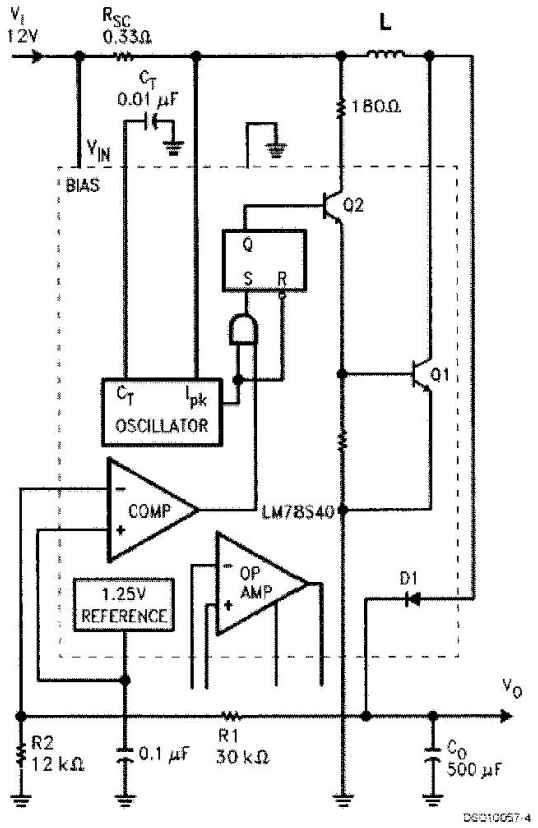
(80 marks)

b) Calculate the ideal output voltage for the op amp circuit below, given that the two input voltages are V1 = -12mV and V2 = -+10mV. (70 marks)



Question 5

a) For the power supply circuit shown, explain its purpose, its mode of voltage conversion and method of operation. (60 marks)



b) By considering R1 and R2, calculate the expected output voltage, Vo. (30 marks)

c) By considering the attached LM78S40 data sheet provided and the components connected to the SMPS controller IC in the above circuit, determine the minimum inductor value, L, needed for this circuit design. (40 marks)

d) Explain reasons why a switched mode power supply (SMPS) may be preferred over a linear power supply/regulator with similar input-output specifications. In particular discuss (with an example) the power dissipation differences. (20 marks)