Design Of A Power Factor Correction AC-DC Converter

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***Abstract*—The need to keep EMI emissions by electronic power supplies below the limit specified by international standards have dictated that any new power supply design must include active power factor correction at the front end. The modern trend in power supply designs is towards digital control. This paper reports an effort to design a power factor correction ac-dc converter that is geared towards digital control. The power factor correction circuit employs zero voltage transition arrangement to minimize switching losses. Calculations that led to the selection of the circuit components are presented. Interface requirements between the power converter stage and the digital control processor are tackled. Average current mode control method is employed in the controller. The complete design has been tested by means of Powersim power electronics simulation software. The resulting input voltage and current waveforms show that the design is successful.**

***Index terms*—ac-dc converter, power factor correction, control design**

I. INTRODUCTION

In most electronic power supplies, the AC input is rectified and a bulk capacitor is connected directly after the diode rectifier bridge. This type of utility interface draws excessive peak input currents; it produces a high level of harmonics, and both the input power factor (PF) and total harmonic distortion (THD) are poor. The low PF makes the efficiency of the electrical power grid to be very low. Regulatory standards with origins in Europe (EN 61000-3-2) and North America (IEC 1000-3) have been established that aim at protecting the utility grid from excessive harmonics. In order to meet the harmonics limits imposed by these standards, new ac-dc converter designs must employ active power factor correction (PFC) at the input.

The boost converter is the most widely used topology for achieving PFC. Figure 1 shows a PFC boost converter. The bulk energy storage capacitor sits on the output side of the boost converter rather than just after the diode rectifier bridge. The average inductor current (in each high-frequency switching cycle), which charges the bulk capacitor, is controlled to be proportional to the utility line-voltage waveform. For proper operation, the output voltage must be higher than the peak value of the line voltage and the current drawn from the line at any given instant must be proportional to the line voltage [1].

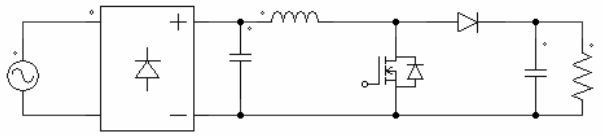

Figure1 Boost PFC ac-dc converter

In order to maintain good EMI performance and reduced switch current ratings, the PFC boost converter is usually operated in the continuous conduction mode (CCM). However, operating the boost converter in the CCM causes increased stress on the boost diode. While the boost transistor is off, load current flows through the boost diode. When the transistor turns on, the diode must recover quickly to prevent the output capacitor from discharging into the transistor. The diode has a finite reverse recovery time, t_{rr} , during which time it experiences reverse current through, and reverse voltage across it. This leads to increased power dissipation in the diode. Using faster diodes helps to reduce diode power dissipation; however, hard turn-off of the diode also increases EMI and degrades diode reliability.

In addition to the increased diode loss caused by reverse-recovery current, the boost transistor also experiences increased turn-on loss. This increase in switching loss is accentuated as switching frequencies increase [2]. In order to achieve acceptable efficiency, several soft switching techniques have been developed. Figure 2 shows a zero voltage transition (ZVT) boost converter, which makes use of an auxiliary resonant circuit which is activated only when the boost transistor is turning on or off. The auxi1iary circuit allows the boost transistor to turn on and off under zero voltage conditions thus reducing the switching losses [3].

The ZVT converter of Figure 2 does not offer a lossless turn on and turn off of the auxiliary switch, which results in lower efficiency in the converter. Even though the auxiliary switch inductor L_r limits di/dt through the boost diode D_1, there is nothing that limits the reverse recovery current from the auxiliary diode D_3. Consequently, each time the auxiliary switch turns on, it experiences a high surge current. Through simulation experiment I discovered that by including some inductance in series with the auxiliary diode D_3, the size of the surge current is greatly reduced, with no perceivable side effect. The resulting modified ZVT pfc circuit is shown in Figure 3.

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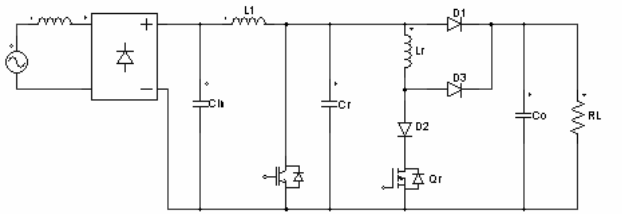

Figure 2 ZVT boost PFC ac-dc converter.

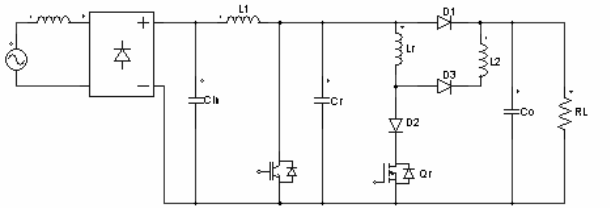

Figure 3 ZVT boost PFC circuit with additional inductor.

II. POWER STAGE DESIGN

The specifications of the boost PFC ac-dc converter are as follows:

AC Input Voltage (rms) 90 V – 270 V
Input Line Frequency 47-63 Hz
Target Efficiency 92% min @ 90VAC / 1000 W

Selection of the boost converter components is carried out following standard procedure, especially as described in [2, 4]. PF is assumed to be 0.99 or greater at low line.

$$P_{in(\max)} = \frac{P_{o(MAX)}}{\eta_{MIN}} = \frac{1000W}{0.92} = 1087W$$

$$I_{in(rms)\max} = \frac{P_{in(\max)}}{V_{in(rms)\min}} = \frac{1087W}{90V} = 12.1A$$

$$I_{in(pk)\max} = I_{in(rms)\max} = 12.1\times\sqrt{2} = 17.1A$$

$$I_{in(avg)\max} = \frac{2I_{in(pk)\max}}{\pi} = \frac{2\times 17.1A}{\pi} = 10.9A$$

A. High Frequency Input Capacitor

$$C_{in} = K_{\Delta I_L}\frac{I_{in(rms)\max}}{2\pi\times f_{sw}\times r\times V_{in(rms)\min}}$$

where:

$K_{\Delta I_L}$ = Inductor current ripple factor (20% in this design)
r = maximum high frequency voltage ripple factor ($\Delta V_{in}/V_{in}$), typically between 3% – 9%, 6% used for this design

$f_{sw} = 115200Hz$ is the switching frequency.

$$C_{in} = 0.2\times\frac{12.1}{2\pi\times 115200\times 0.06\times 90} = 0.62\mu F$$

C_{in} = 680 ηF, 450 V, is selected.

B. Input Lnductor

The inductance required is determined by the amount of switching ripple current that can be tolerated.

$$V_{in(pk)\min} = \sqrt{2}V_{in(rms)\min} = 90\sqrt{2} = 127V$$

Peak boost transistor duty cycle,

$$D_{pk} = 1 - \frac{V_{in(pk)}}{V_o} = 1 - \frac{127}{400} = 0.6825.$$

Inductor ripple current,

$$\Delta I_L = 0.2I_{in(pk)\max} = 0.2\times 17.1 \cong 3.42A.$$

ΔI_L is based on the assumption of 20% ripple current.

Peak inductor current,

$$I_{L(pk)\max} = I_{in(pk)\max} + \frac{\Delta I_L}{2} = 17.1 + \frac{3.42}{2} = 18.8A.$$

$$L = \frac{V_{in(pk)\min}\times D_{pk}}{f_{sw}\times\Delta I_L} = \frac{127\times 0.6825}{115200\times 3.42} = 220\mu H$$

L = 2.2 mH is selected, in order to achieve good dynamic performance.

C. Output Capacitor

The value of the output capacitor impacts hold up time and ripple voltage. In this design, the criterion for selection of this capacitor is the amount of tolerable ripple in the output voltage, as described in [5]:

$$C_{out} \geq \frac{\frac{P_o}{V_o}}{2\pi f_r\times\Delta V};$$

where f_r is the frequency of the rectified sine wave (100 Hz—worst case), and ΔV is the desired peak-to-peak output voltage ripple.

$$C_{out(\min)} = \frac{1000/400}{2\pi\times 100\times 0.03\times 400} = 332\mu F$$

Derating the output capacitor value by 20% for tolerance in order to guarantee minimum capacitance requirement is satisfied,

$$C_{out} = \frac{C_{out(\min)}}{1-\Delta C_{tol}} = \frac{199}{1-0.2} = 415\mu F \cdot$$

For ease of realization $C_{out} = 400\mu F$, 450V, is selected.

D. Boost Diode

The boost diode is selected in accordance with the considerations given in [2]. The International Rectifier 15ETH06 15A, 600V, ultra-fast rectifier is selected for this application. The use of an ultra-fast diode helps to increase overall system efficiency reduces the peak stress of the diode and ZVT transistor.

E. Boost transistor

The main MOSFET is chosen according to standard design criteria. The maximum voltage that it must be able to handle is the output voltage V_o, with ripple. Thus the main MOSFET must handle more than 412 V. The voltage rating must be sufficient to withstand the full output current at low line voltage, maximum load. Fairchild's FCB20N60 N-Channel MOSFET is selected—rated at 600V, 20A, with $R_{OS}(on)$ = 0.15Ω (25°C), C_{oss} ~ 165pF.

F. Input Rectifier Diodes

The maximum voltage that appears across an input bridge diode is the maximum input voltage that is encountered during high line conditions $V_{in(rms)max}$ at input of the converter:

$$V_{in(pk)} = \sqrt{2} \times V_{in(rms)\max} = 270\sqrt{2} = 382V$$

The peak current that flows through them is $I_{L(pk)\max} = 18.8A \cdot$

The average current that an input diode must conduct is

$$I_{in(avg)\max} = 10.9A \,.$$

G. Auxiliary transistor

The RMS current seen by the ZVS MOSFET is small. A MOSFET with reduced capacitance and higher on-resistance is required in order to reduce switching losses. Fairchild's FCP7N60 N-Channel MOSFET is selected as the auxiliary switch—rated at 600V, 7A, with $R_{OS}(on)$ = 0.53Ω (25°C), C_{oss} ~ 60pF.

H. Resonant Inductor:

The resonant inductor is selected according to considerations described in [2].

$$\frac{di}{dt} = \frac{I_{in(\max)}}{3 \cdot t_{rr}} = \frac{18.8A}{105ns} = \frac{179A}{\mu s}$$

$$L_r = \frac{V_o}{di/dt} = \frac{400V}{179A/\mu s} = 2.2\mu H$$

I. Resonant Capacitor

The resonant capacitor is sized to ensure a controlled dv/dt of the main switch. The effective resonant capacitor is the sum of the MOSFET capacitance and the external node capacitance. The FCB20N60 has approximately 165 pF of output capacitance; adding an external capacitance of 680pF across the device is adequate.

J. Auxiliary diodes

The same diode (the International Rectifier 15ETH06) is selected for the realization of diodes D_2 and D_3 in Figure 3.

III. POWER STAGE-CONTROLLER INTERFACING

In order for a digital processor to control the inductor current and the output voltage of the PFC circuit, it must be able to acquire the values of three signals. These are the rectified input voltage V_{in}, the inductor current I_{in}, and the dc bus capacitor voltage V_o.

A. Output voltage sensing

Output voltage of the converter is sensed by means of a resistive voltage divider network, as described in [4]. The divider is made up of an upper 1 MΩ resistor and a lower resistor whose value is calculated. The upper 1 MΩ resistor is made up of two 499 KΩ resistors, so that the power rating of the resistors will not be exceeded.

$R_{fb1} = R_{fb2}$ = 499KΩ, 1% tolerance.

$$R_{fb3} = \frac{V_{FS}(R_{fb1} + R_{fb2})}{V_{out(abs-\max)} - V_{FS}}$$

where $V_{FS} = 4.096$ V is the reference voltage of the A/D converter connected to the digital processor and $V_{out(abs-\max)}$ is the expected absolute maximum output voltage. Since the nominal value of the output voltage is 400 V, $V_{out(abs-\max)}$ is made equal to 450 V, the voltage rating of the output bulk capacitor.

$$R_{fb3} = \frac{4.096V(499K + 499K)}{450V - 4.096V} = 9.2K\Omega$$

(R_{fb3} = 9.09kΩ, 1% tolerance.)

B. Input voltage sensing

Similar to considerations that led to the selection of the feedback resistors, in order to reduce power dissipation in the input voltage sensing divider, the feed-forward resistors R_{ff1} and R_{ff2} are selected as

$$R_{ff1} = R_{ff2} = 499K\Omega, \text{ 1\% tolerance.}$$

$$R_{ff3} = \frac{V_{FS}(R_{vi1} + R_{vi2})}{V_{in(abs-\max)} - V_{FS}}.$$

$V_{in(abs-\max)}$ is assigned the value of 450 V.

$$R_{ff3} = \frac{4.096(499K + 499K)}{450 - 4.096} = 9.2K\Omega$$

(R_{ff3} = 9.09kΩ, 1% tolerance, is selected.)

C. Input current sensing

The voltage drop across the current sense resistor should not exceed the reference voltage source of the A/D converter.

$$R_s = \frac{V_{FS}}{I_{in(abs-\max)}} = \frac{4.096V}{20A} \cong 0.2\Omega$$

D. Signal conditioning

Analog low-pass filters with cutoff frequency well below half of the switching frequency are inserted in the current and voltage feedback loops in order to reduce the aliasing effect.

IV. CONVERTER CONTROL

Figure 4 shows the structure of the control strategy employed by the digital processor to force the average inductor current to be proportional to the voltage output of the input bridge rectifier. The PFC converter is controlled by two feedback loops. The average output dc voltage is regulated by a slow response 'outer loop'; whereas, the inner loop that shapes the input current is a much faster loop.

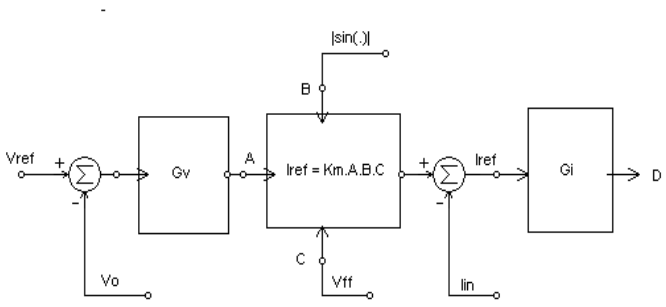

Figure 4 Structure of boost PFC control strategy.

As indicated in the previous section, the digital processor receives sampled valued of three power stage variables. Each sample received by the processor is already in normalized form, meaning that the values exist in the range [0 1]. This is easily achieved by configuring the A/D converter to present its digital output to the processor in fractional number type.

One of the variables which samples are acquired by the processor is V_O, normalized value of the output voltage. The value of V_O is subtracted from the normalized control reference V_{ref} and the result is the error voltage. The error voltage value becomes the "A" input of the reference current calculator. Two other values are required in order to calculate the reference current. "B" is unit amplitude rectified sine wave generated by the processor. In analog controllers, "B" is obtained by normalizing the feed-forward voltage. The feed-forward voltage is usually corrupted by EMI noise, so that it is impossible to obtain pure sinusoidal shape. By programming the processor to generate a sine wave, purity is achieved. However, the generated sine wave must be synchronized to the input line voltage waveform.

Input "C" to the reference current calculator is derived from the voltage feed-forward signal. "C" causes power input to the PFC regulator to remain constant at a specified level (determined by the load) regardless of line voltage changes. In order to obtain "C", a voltage proportional to rms value of the input voltage must be derived from the normalized voltage feed-forward input to the processor. The average value of the voltage feed-forward input satisfies this requirement. The average value can be obtained either by analog low-pass-filtering, or better by averaging the signal over a period of the input waveform. The averaging method is more easily implemented by the digital processor, as described in [5]. The same algorithm that synchronizes the processor-generated sine shape to the voltage feed-forward signal also enables averaging of the voltage feed-forward signal over a period.

Let the average value of the normalized voltage feed-forward signal calculated by the processor be designated as V_{dc}. The maximum value of V_{dc} will be

$$V_{dc(\max)} = \frac{2V_{in}}{\pi V_{in(\max)}},$$

where all the voltages are peak values of input line voltage.

In order to obtain "C", the reciprocal of V_{dc} must be calculated and then normalized, as follows.

$$C = \frac{\frac{1}{V_{dc}}}{\left.\frac{1}{V_{dc}}\right|_{\max}}$$

It can be shown that

$$\left.\frac{1}{V_{dc}}\right|_{\max} = \frac{\pi V_{in(\max)}}{2V_{in(\min)}},$$

so that

$$C = \frac{1}{V_{dc}} \times \frac{2V_{in(\min)}}{\pi V_{in(\max)}} = \frac{2\times 90}{\pi \times 270} = \frac{0.2122}{V_{dc}}. \quad (1)$$

If eq. (1) is adopted as the expression for "C", then K_m in Figure 4 is equal to 1. Alternatively, if

$$C = \frac{1}{V_{dc}}$$

is adopted, then

$$K_m = 0.2122.$$

The reference current calculation is then carried out as follows:

$$I_{ref} = K_m.A.B.C$$

Following the calculation of I_{ref}, normalized value of inductor current, measured by the sensing resistor, is subtracted from I_{ref} to form the current error signal. The current error is operated upon by the current loop compensator to produce suitable value of boost transistor duty cycle that will make the average inductor current to track the line input voltage waveform.

A. Current Loop Compensator

The small signal model of the ZVT converter is the same as that of the basic PFC boost converter as both of the converters operate similarly during most of their switching cycle. The only difference is during the turn-on and turn-off transitions of the main switch and this has no bearing on the design of the control loop.

In the design of the current compensator, the influence of the (slow) voltage loop is ignored. In order to faithfully track the semi-sinusoidal current reference waveform, a bandwidth of 8 kHz is appropriate for the current loop [5].

The loop gain equation for the current loop is,

$$T_i = G_{id} K_S G_C$$

where G_{id} is the relationship between the boost transistor duty cycle and the average inductor current,

$K_S = \frac{1}{I_{\max}} = \frac{1}{20}$, is the normalization (or scaling) factor of the inductor current and G_c is transfer function of the current loop compensator.

High frequency approximation of the current loop power stage (1/sC = 0) is given by: [5]

$$G_{id} = \frac{\hat{I}_{in}}{\hat{d}} = \frac{V_o}{sL}$$

At the gain crossover frequency of the current control loop,

$$T_i\big|_{\max} = \frac{V_o}{2\pi f_{ci} L} K_S G_{CA} = 1,$$

where G_{CA} is the gain of the current error amplifier and f_{ci} is the current loop bandwidth.

For a current loop bandwidth of $f_{ci} = 8kHz$, the required current error amplifier gain is, [5]

$$G_{CA} = \frac{2\pi f_{ci} L}{K_s V_o} = \frac{2\pi \times 8000 \times 2.2\times 10^{-3}}{\frac{1}{20}\times 400} = 5.53$$

Setting the current loop PI compensator zero at 800 Hz, the integral time constant for the current compensator becomes:

$$T_{iC} = \frac{1}{2\pi \times 800} = 1.99\times 10^{-4}$$

Therefore, the transfer function of the current loop compensator is

$$G_C = 0.553\left(\frac{1+1.99\times 10^{-4} s}{1.99\times 10^{-4} s}\right)$$

B. Voltage Loop Compensation

In the design of the voltage loop compensator, it is assumed that the input current is perfectly controlled by the current loop controller and that it perfectly tracks the input voltage. In order to avoid large distortion due to power stage output voltage ripple, the voltage loop compensation should have a bandwidth much smaller than 100Hz. Usually, the bandwidth of the voltage loop is chosen to be 10~20Hz.

Assuming equality of input and output power:

$$P_{in} = P_{out}$$

$$\frac{I_{in(pk)}V_{in(pk)}}{2} = I_O V_O$$

$$I_O = \frac{I_{in(pk)}V_{in(pk)}}{2V_O}$$

From Figure 4, once the current loop is closed, the voltage loop power stage transfer function can be calculated as,

$$G_{VC} = \frac{v_o}{v_{err}} = \frac{K_m.A.B.C}{K_s} \times \frac{V_{in}}{2V_o} \times Z_f$$

where, Z_f represents the equivalent impedance of the parallel branch consisting of the bus capacitor C, the PFC stage output impedance r_o and the load impedance Z_L, and is given by, [5]

$$Z_f = \frac{1}{\frac{1}{r_o} + \frac{1}{Z_L} + sC}.$$

For resistive load R_L, as in Figure 3, the load impedance Z_L and the output impedance r_o are related by,

$$Z_L = R_L = \frac{V_o}{I_o} = r_o$$

The loop gain equation for the voltage loop is,

$$T_v = K_{vo} G_{VA} G_{VC}$$

where K_{vo} is the output voltage normalization factor and G_{VA} is the voltage error amplifier gain.

At the voltage loop gain crossover frequency,

$$T_v\big|_{\max} = \frac{K_{vo}}{K_S} \times \frac{V_{in(\max)}}{2V_O} Z_f.G_{VA} = 1$$

Using the voltage loop gain equation, for a voltage loop crossover frequency of f_{cv} = 10 Hz, the required voltage error amplifier compensator is,

$$G_{VA} = \frac{2K_S V_O}{K_{vo} V_{in(\max)} Z_f\big|_{f=f_{cv}}}$$

Overall output impedance,

$$Z_f = \frac{1}{\frac{1}{r_o} + \frac{1}{Z_L} + sC}$$

$$Z_f = \frac{1}{\sqrt{\left(\frac{1000}{400^2} + \frac{1000}{400^2}\right)^2 + \left(2\pi \times 10 \times 450.10^{-6}\right)^2}} = 32.3$$

$$G_{VA} = \frac{2 \times \frac{1}{20} \times 400}{\frac{1}{450} \times 270\sqrt{2} \times 32.3} = 1.46$$

Setting the voltage loop PI compensator zero at 10 Hz, the integral time constant for the voltage compensator becomes:

$$T_{VC} = \frac{1}{2\pi \times 10} = 1.59 \times 10^{-2}$$

Therefore, the transfer function of the voltage loop compensator is

$$G_C = 1.46\left(\frac{1 + 1.59 \times 10^{-2} s}{1.59 \times 10^{-2} s}\right)$$

The designed analog compensators are converted to digital forms through standard procedures.

V. SIMULATION RESULT

Simulation experiments were carried out on the designed boost PFC circuit, together with the compensator. Powersim simulator was employed for the experiments. The schematic entry into the simulator is shown in Figure 5. Figure 6 shows the resulting input voltage and current waveforms.

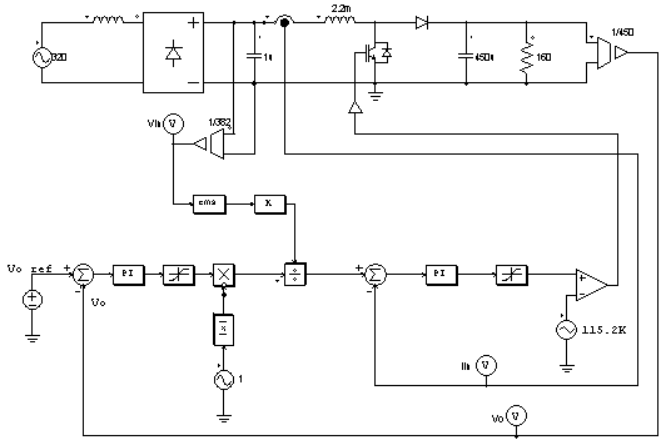

Figure 5 PFC circuit and control simulation using Powersim.

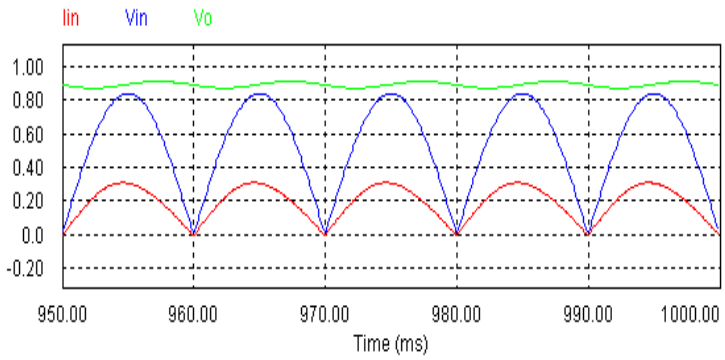

Figure 6 Normalized input voltage and current.

VI. CONCLUSION

A boost PFC ac-dc converter that is suitable for digital processor control has been designed. Calculations that led to selection of circuit components have been presented. Standard procedure has been followed to design compensators for both the current and voltage loops. The whole design has been tested by means of simulation using Powersim power electronics and drives simulation package. Even though the simulator restricted the implementation of the control law, the results are encouraging. There is indication that if a practical system is realized with the freedom of practical digital processor programming, excellent results will be achieved.

REFERENCES

[1] S. Davis, "Basics of power factor correction design," ED Online 9507, February 3, 2005, www.elecdesign.com/Files/29/9507/9507_01.pdf. [Accessed March 2, 2007.]

[2] James P. Noon, "A 250 kHz, 500 W power factor correction circuit employing zero voltage transitions," focus.ti.com/lit/ml/slup106/slup106.pdf, Oct '94. [Accessed March 3, 2007.]

[3] N. Jain, "A zero voltage switching boost converter using a soft switching auxiliary circuit with reduced conduction losses," MASc Thesis, Concordia University, Montreal, Quebec, Canada, 2000.

[4] R. Brown and M. Soldano, "PFC Converter Design with IR1150 One Cycle Control IC," International Rectifier Application Note AN-1077.

[5] S. Choudhury, "Average Current Mode Controlled Power Factor Correction Converter using TMS320LF2407A," Texas Instrument Application Report, SPRA902A, July 2005.

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