Common-Source Amplifier Designs

1) Resistor Load

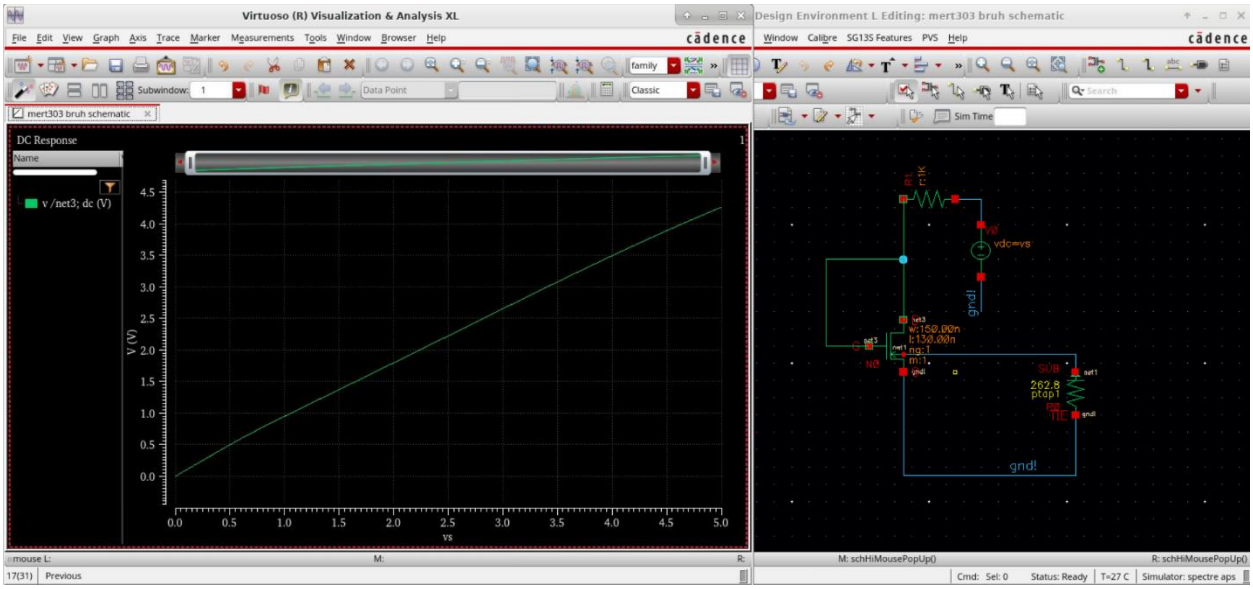
A) Schematic Design

First, I needed to determine Vt and Kn values. For that I used the

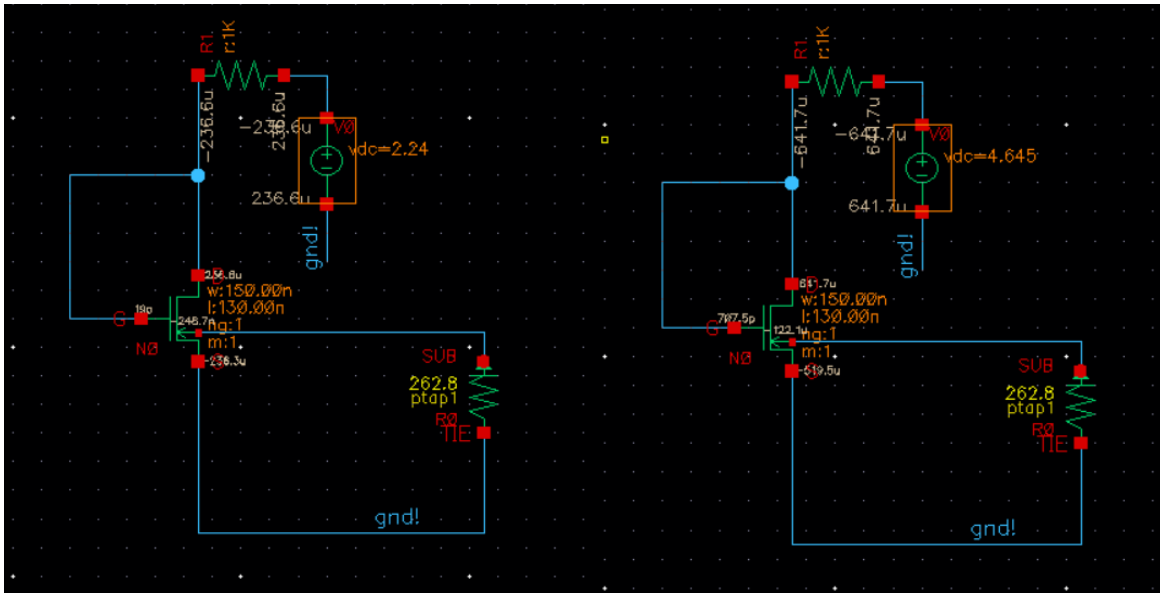
Vt = (Vgs2-Vgs1(Id2/Id1)^1/2) / (1-(Id2/Id1)^1/2)

Kn = Id1 / (Vgs1-Vt)^2

Diode connection setup for finding Vt and Kn:



From Lab report 10 from other semester, I used 2V drop over Rd and 4V drop as reference point for calculating these values. (2.24V Vdd gives 2V and 4.645 gives 4V)

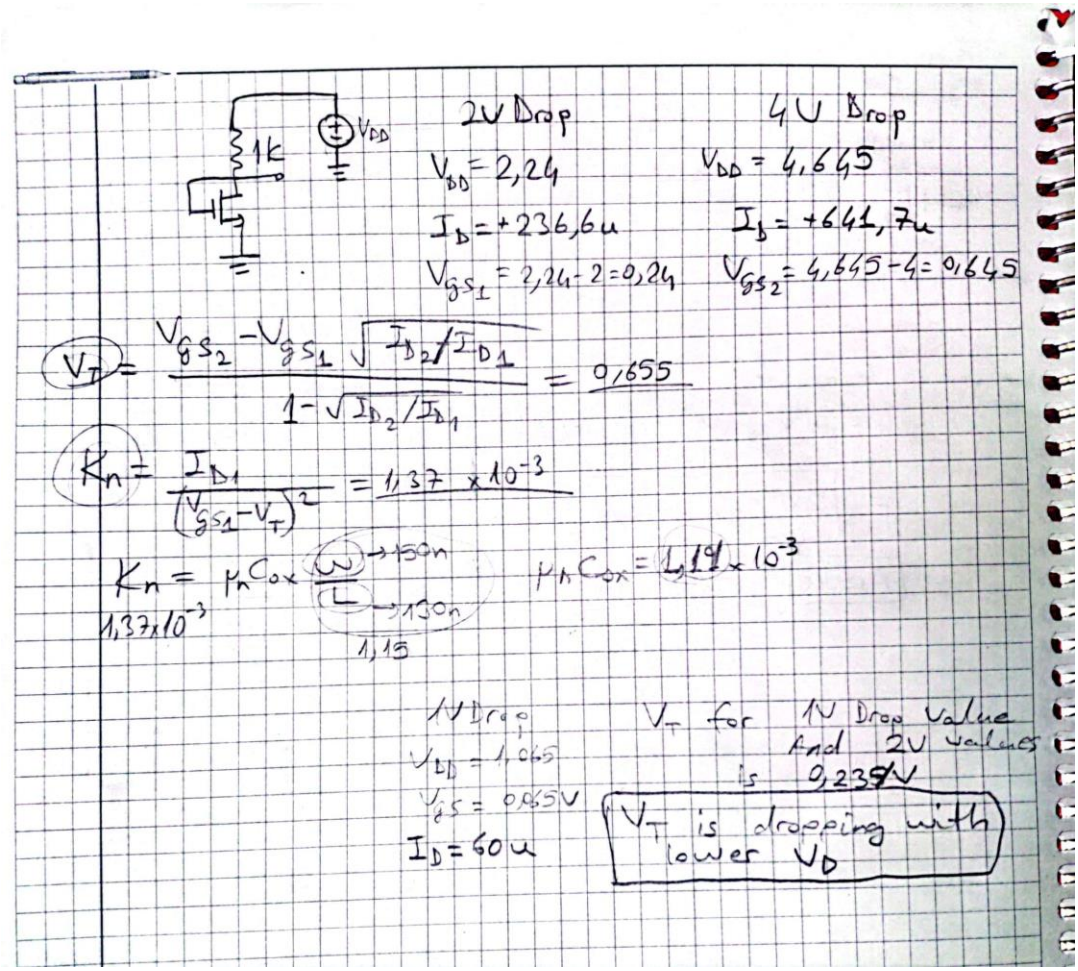


Vt = 655mV

$$\left|\frac{\left(0.645-0.24\sqrt{\left(641\cdot10^{-6}\right)-\left(236.10^{-6}\right)}\right)}{1-\sqrt{\left(641\cdot10^{-6}\right)-\left(236.10^{-6}\right)}}\right| = 0.6555201294$$

Kn = 1.37m

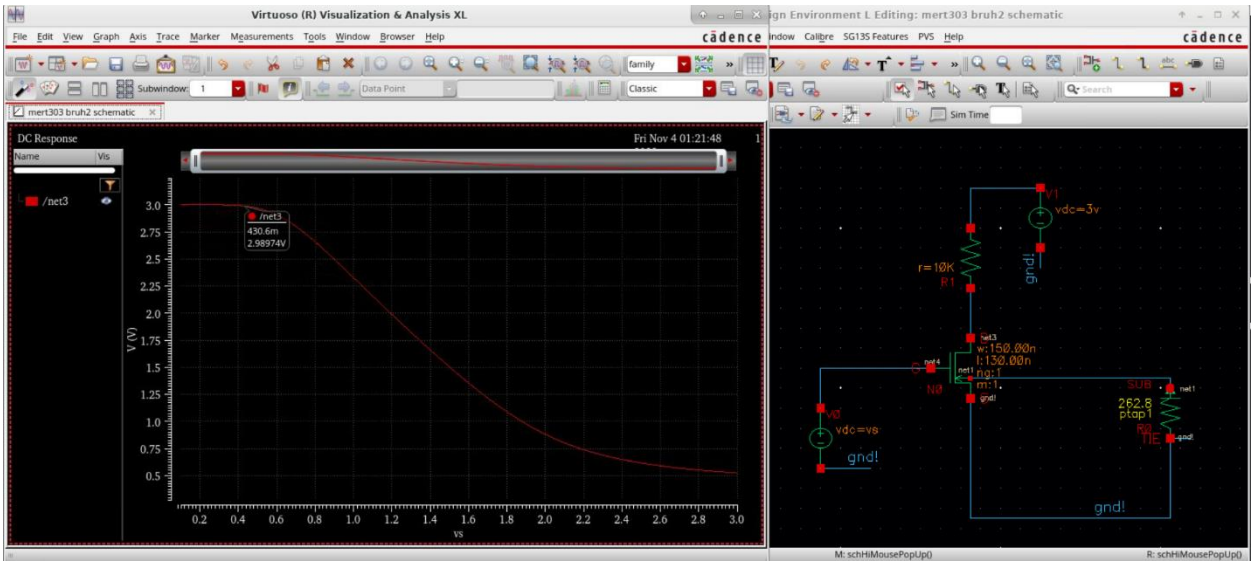
$$\left|\frac{\left(236\cdot10^{-6}\right)}{(0.24-0.655)^2}\cdot10^3\right| = 1.370300479$$



The problem with calculating Vt is that it changes and Vt decreases when Rd increases or Vdd decreases.

$$\frac{\left(0.24-0.065\sqrt{\left(236\cdot 10^{-6}\right)-\left(60.10^{-6}\right)}\right)}{1-\sqrt{\left(0.236\cdot 10^{-6}\right)-\left(60.10^{-6}\right)}} = 0.2391176088$$

The Vdd vs. Vd voltages get closer to each other when we go to the left side of the graph. For example, for 1V drop over Rd Vdd only needs to be 1.065V and results vary. Because Vt changes we cannot make decisions with normal methods and expect accurate results from Cadence. From testing I confirmed this behavior myself with different amplifier structures.



We can also see the inverter behavior and how un-ideal the real mosfet simulation is. From here we start seeing Vd drop from 4.99 to 4.98 at around 450mV Vgs voltage. Vt is somewhere between 650mV and 300mV from my tests, so it checks out.

Now that I know I can no longer rely on facts and logic when working with real devices I can design with gm and Rd to get Av = -gm((Rd*ro) / (Rd+ro)) without bothering with other values. The Kn value isn't as volatile as Vt so It can be still used. (Not: it wasn't)

From here I tried with experimental methods instead of hand calculations.

Below there is the finalized resistor load CS amplifier:

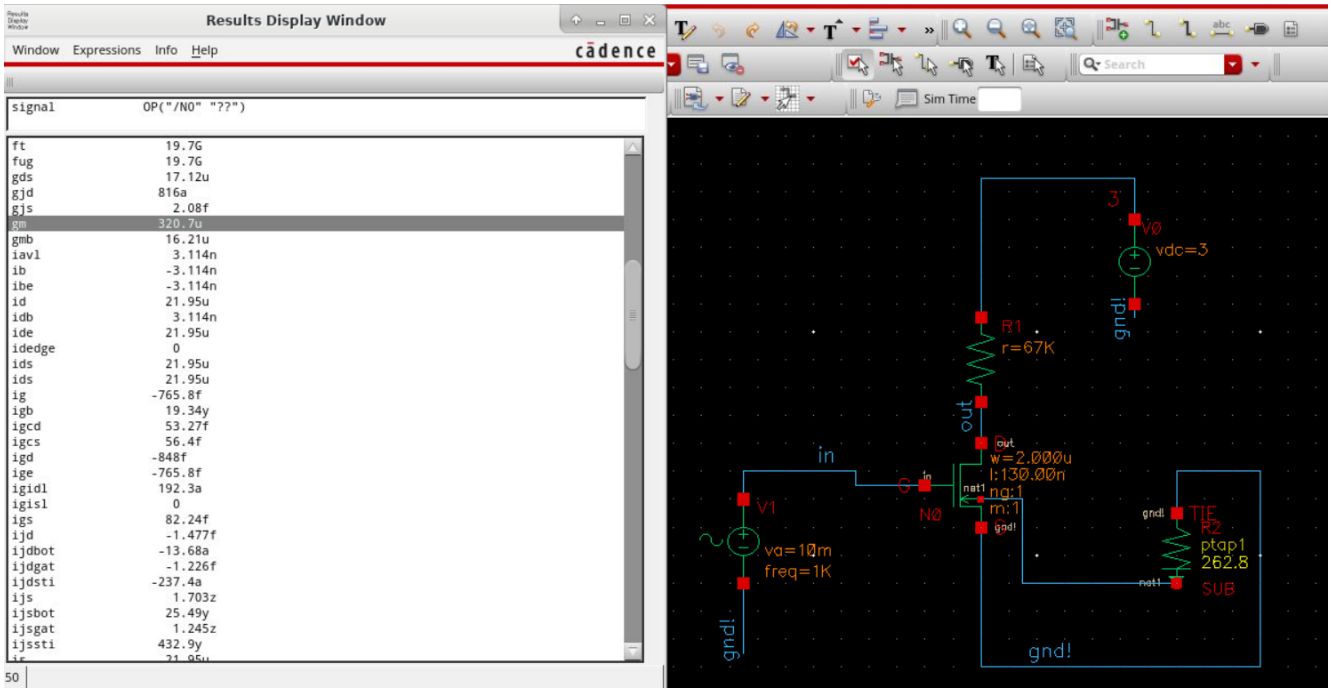


Figure 1: Amplifier I made with 10 gain by experimenting

If I fill gm formula of (2*un*Cox*(W/L)Id)^1/2 according to the un*Cox value I found at the beginning with Kn I get more gm than there really is.

$$10^{6}\sqrt{2 \cdot 1.19 \cdot 10^{-3} \cdot 22 \cdot 10^{-6} \cdot \frac{2000}{130}} \; = 897.517945$$

Calculating un*Cox from here gives 0.15*10^-3 which is way lower than what I calculated. Accepting and using this value on other amplifier examples doesn't yield comparable results either even though I am ignoring early voltage. The amplifier on top has 10 times gain as required but if we try to calculate Rd value for it from gm of 320u to validate that 67K we instead get 31.25K. Since I don't know the early voltage, I can assume it is causing this difference and calculate it from parallel resistor formula.

31250 = (67000*ro)/67000 + ro)

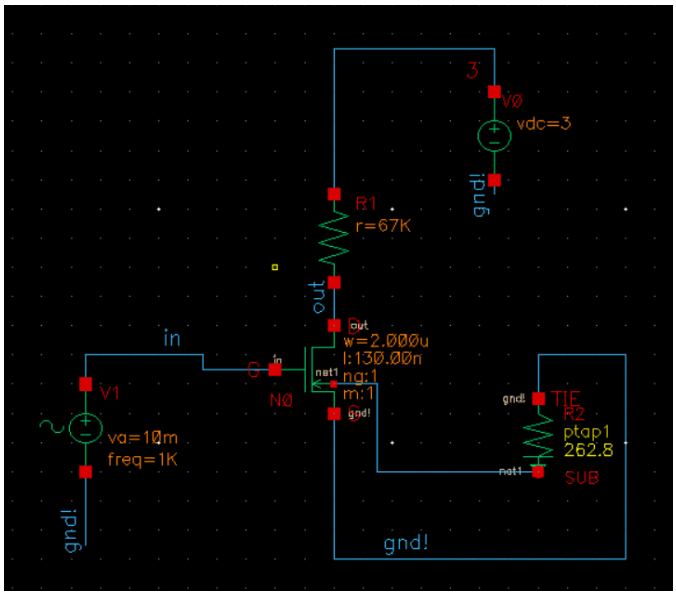
ro = 58566ohm

early voltage = 1/ro = 1.707*10^-5

early voltage is too low to change gm marginally and make the inconsistency I face normal and even if it did it would only increase the gm I calculated.

When designing the amplifier, I first tried using source resistor as well to get better characteristics. But it created the problem of having the body voltage difference and generally adding more complexity that I didn't need. For that reason I started with the regular 1K Rd and

started increasing the drain resistance to obtain more gain. While I was increasing drain resistance the Vd dropped and required bias voltage got lower as well. Also for the reasons I explained Vt also decreases.



For this setup 450mV bias voltage is used. If bias voltage gets around 400mV mosfet quickly gets into the cutoff region and gain drops dramatically. Bias voltage always needs to be determined by testing in simulation since it is not possible to hand calculate the Vt.

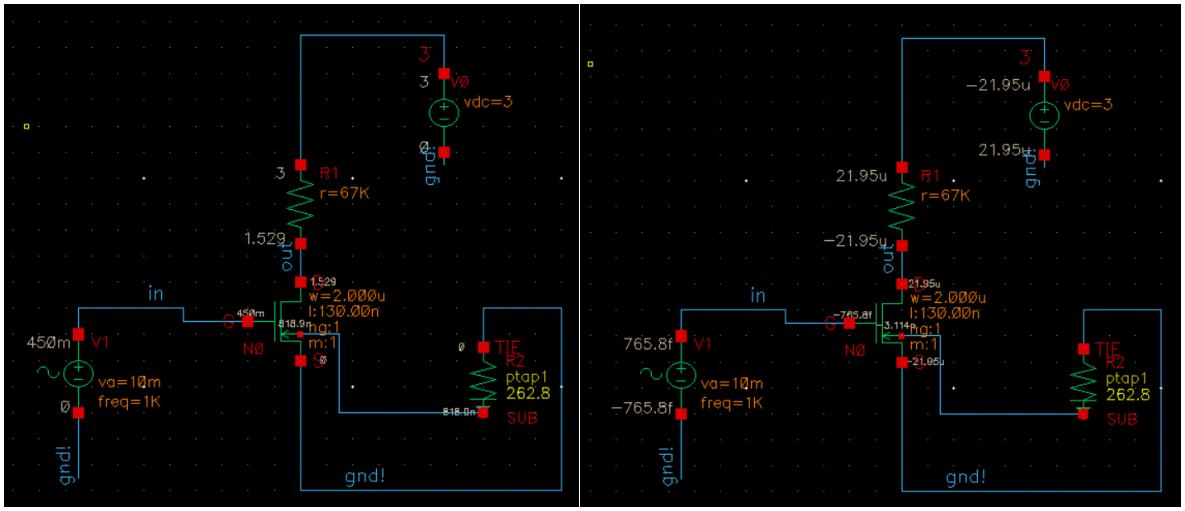
Mosfet Width had to be increased to 2um because it is not feasible to keep it at minimum value of 150nm. For this case 2um is the sweet spot and going up or down from there only drops the gain. I cannot just increase gm by increasing width because increasing width increases current draw which at the same times decreases gain. It is not possible to increase gain without giving something in return with a single stage CS amplifier.

$$\Rightarrow A_v = -\sqrt{2\mu_n C_{ox}\frac{W}{L}}\frac{V_{RD}}{\sqrt{I_D}}$$

B) Simulation Results

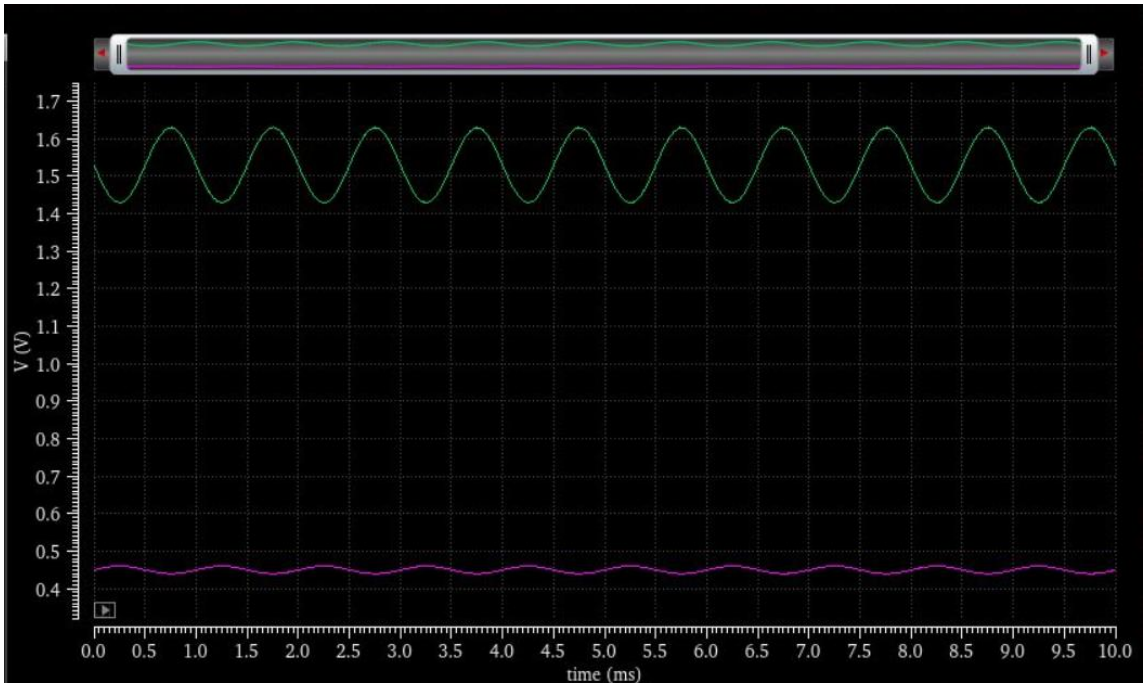
For simulations DC, AC from 1Hz to 10Ghz and transient for 0.01s is used.

DC results:



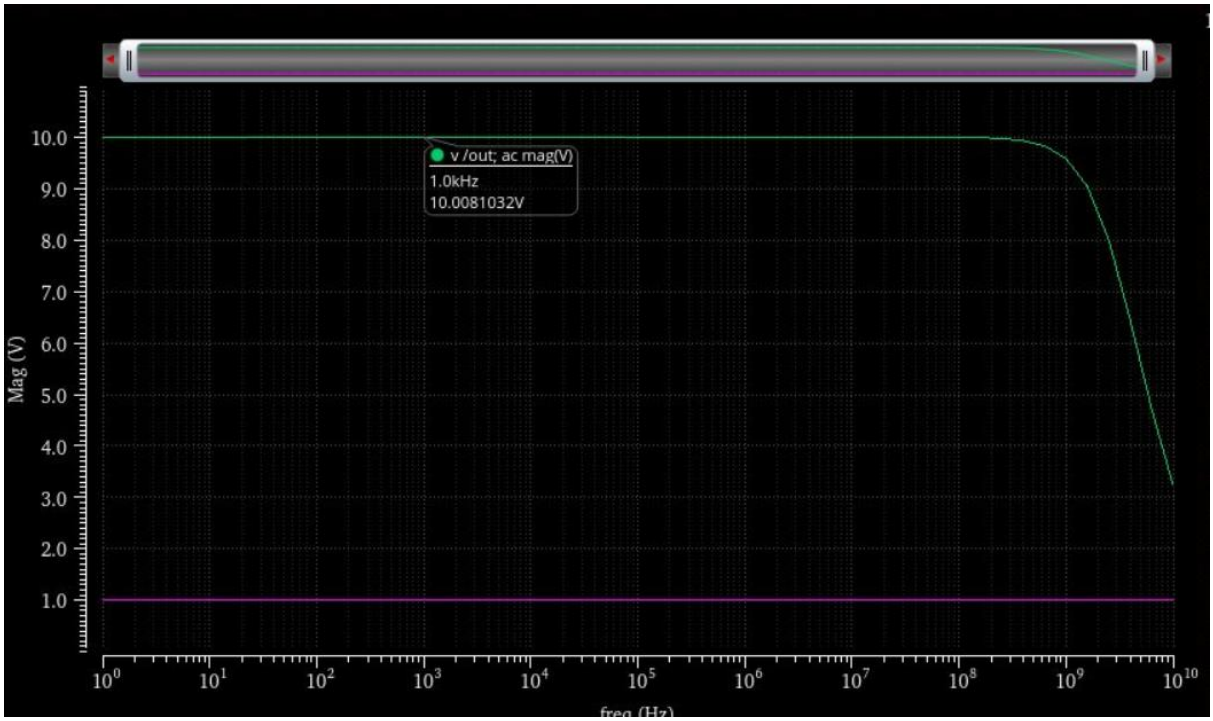
1.529 is a good middle point from 3V power supply for maximum headroom and 22uA is ideally small for power consumption.

Transient results:

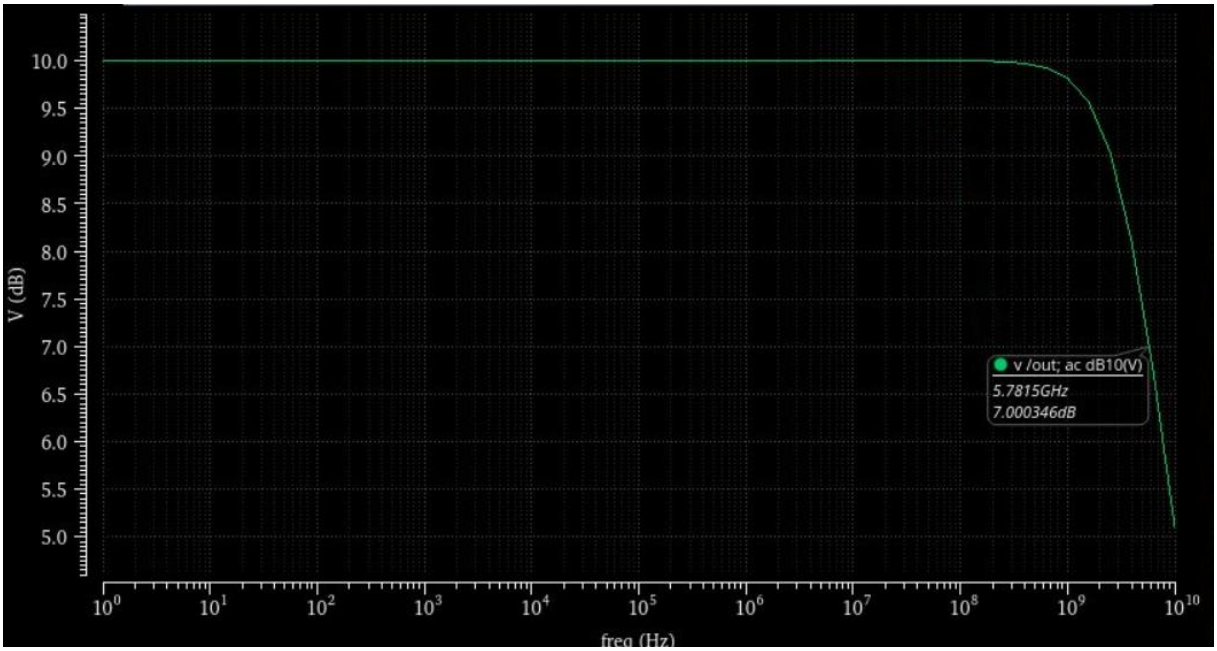


10 times gain can be seen from here, but AC will make it more obvious.

AC results:

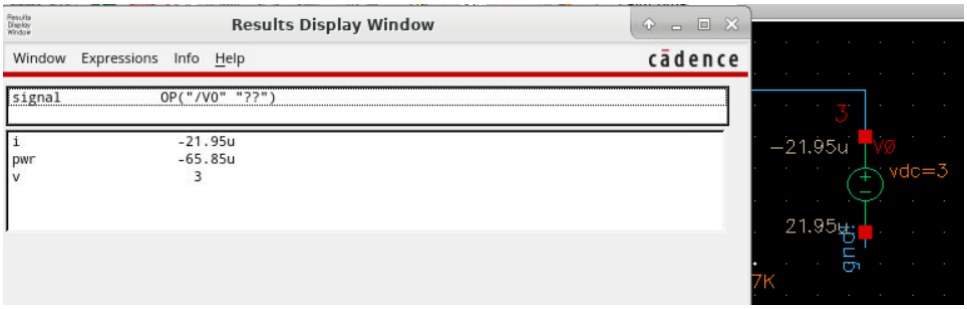


I have tuned the gain to be exactly 10 and it was spot on. If I open it for showing 10dB value instead, I can see that -3dB point is around 5.8Ghz which is not bad at all considering Rd is quite large and adding to the time constant. It is where gain drops to 10/(2)^1/2.



Calculating FOM:

FOM = Voltage Gain * 3-dB Bandwidth (MHz) / Power Consumption (uW)

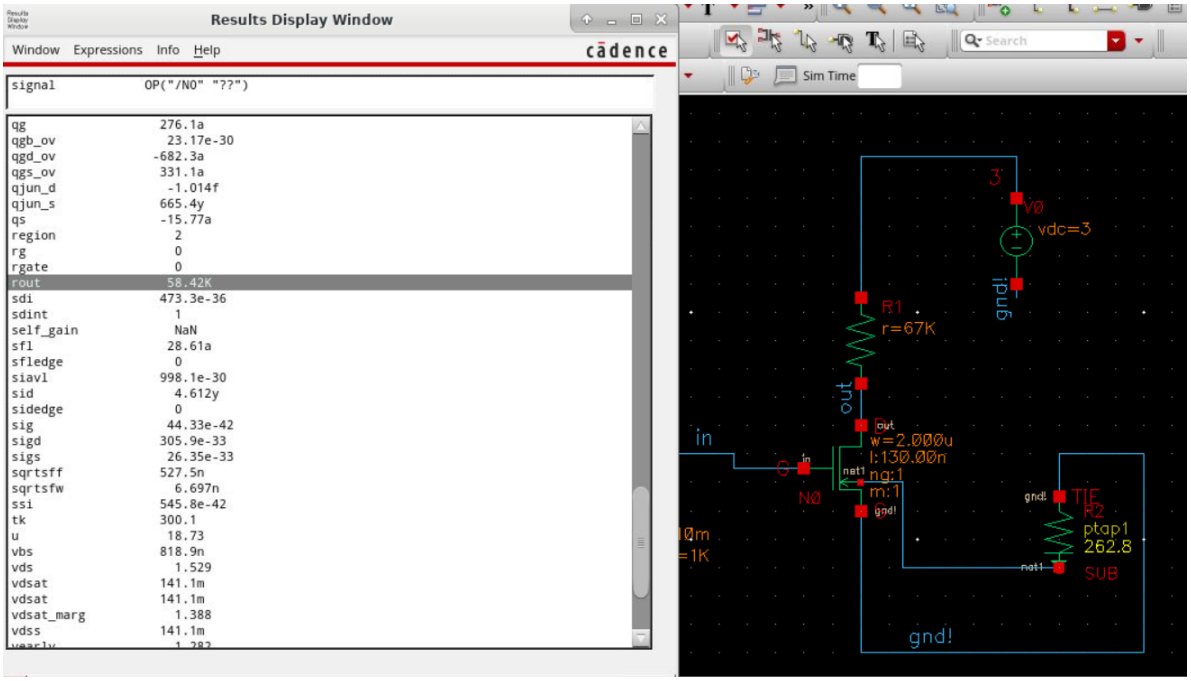


Clicking on power supply in DC Operating Points mode show that the power usage is 65.85uW.

FOM =

$$\frac{\left(10 \cdot 5.78 \cdot 10^{3}\right)}{65} = 889.2307692$$

It is quite over spec compared of the required 10.



ro was actually 58K. (I learned that I can check ro right now)

This concludes resistor load amplifier.

2) Diode-connected Load

A) Schematic Design

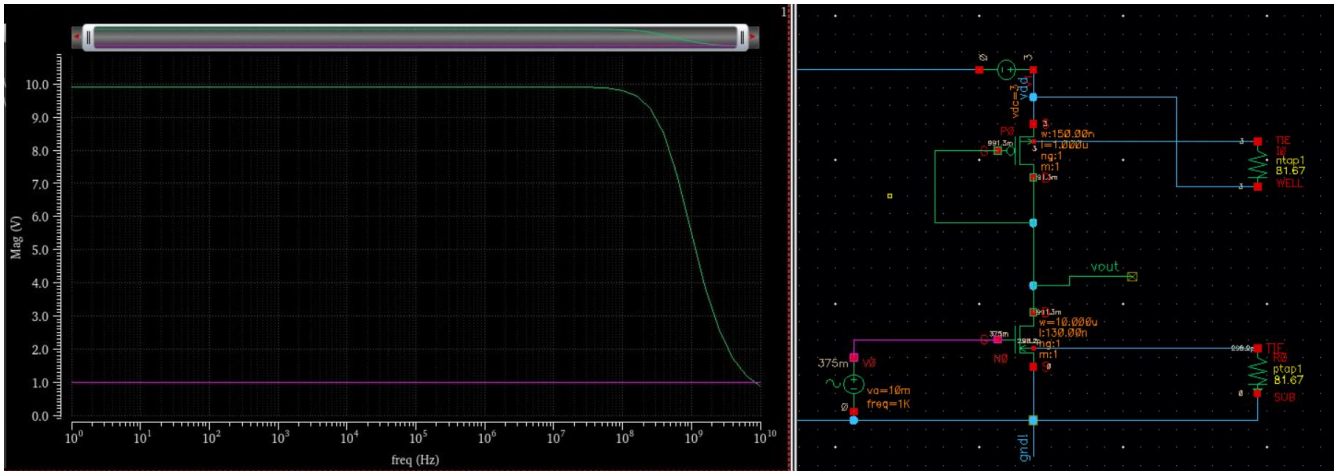
PMOS Diode connected load acts like a current source because it is always guaranteed to be in saturation mode and used instead of regular resistors because using CMOS which is NMOS and CMOS combined is cheap and reliable way to make digital and analog chips. Producing precise resistors on silicon is expensive. For example, AD633 is an analog multiplier with laser cut precision resistors but it costs around 20USD to get a hold of one. AD620 is another IC with laser cut resistors that cost around 8USD because its internal structure is simpler but still way more expensive when compared with generally under 1USD CMOS chips.

$$A_{vo} = \frac{v_o}{v_i} = \frac{-(r_{o1} \| r_{o2}) g_{m1}}{1 + (r_{o1} \| r_{o2}) g_{m2}} \approx \frac{-g_{m1}}{g_{m2}}$$

$$A_{vo} = \frac{-g_{m1}}{g_{m2}} = -\frac{2\sqrt{K_1}\sqrt{I_D}}{2\sqrt{K_2}\sqrt{I_D}} = -\sqrt{\frac{K_1}{K_2}} = -\frac{\sqrt{(W/L)_1}}{\sqrt{(W/L)_2}}$$

Strong main device and weak load device gives higher gain

I tested and figured out the values for getting 10 times gain. (9.9V/V)



Normally using this W/L ratios would give more than 10 times gain in ideal conditions.

$$\sqrt{\left(\frac{\left(\frac{10000}{130}\right)}{\frac{150}{1000}}\right)} = 22.64554068$$

Because I know the ro of NMOS from resistor load amplifier I should be able to figure out PMOS ro and see if this is caused by ro. I can also find Kn and Kp from gm and Id like I did from DC values since both transistors share same current.

ro was already listed in DC parameters and it is 3.3M for PMOS in this circuit.

gm of PMOS = 15.21

gm of NMOS = 370.4 (looks like gm over 300u is ideal comparing with resistor load having gm = 320u)

$$\frac{370.4}{15.21} = 24.35239974$$

Again, an overestimation. The effect of ro on nanometer devices must be something that can not be ignored even at currents as low as 14.89uA. Low current passing over the PMOS means it is acting like a very large resistor.

$$\frac{3}{14.89 \cdot 10^{-6}} = 201477.5017$$

Because it is equivalent of a 200K resistor current is lower than the resistor load amplifier with 67K resistor.

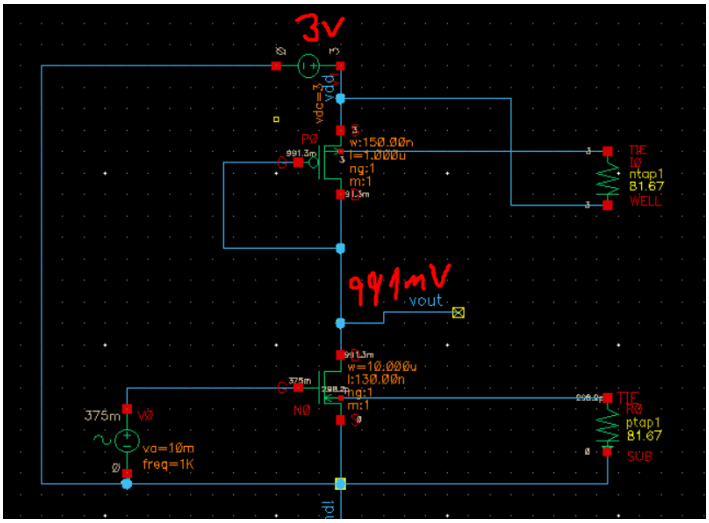
$$10^{6} \cdot \sqrt{2 \cdot 10^{-3} \cdot 14.89 \cdot 10^{-6} \cdot \frac{150}{1000} \cdot 0.052|} = 15.24086612$$

Kp for PMOS is around 0.052u. This would make sense since holes have less mobility so up is lower than un which makes Kp smaller than Kn but If I change 150/1000 with 10000/130 for NMOS and keep the Id same since they pass the same current, I will have even smaller Kn value which shouldn't make sense. This is the last time I will try to calculate or use K value for mosfets in these simulations but wanted to check it again.

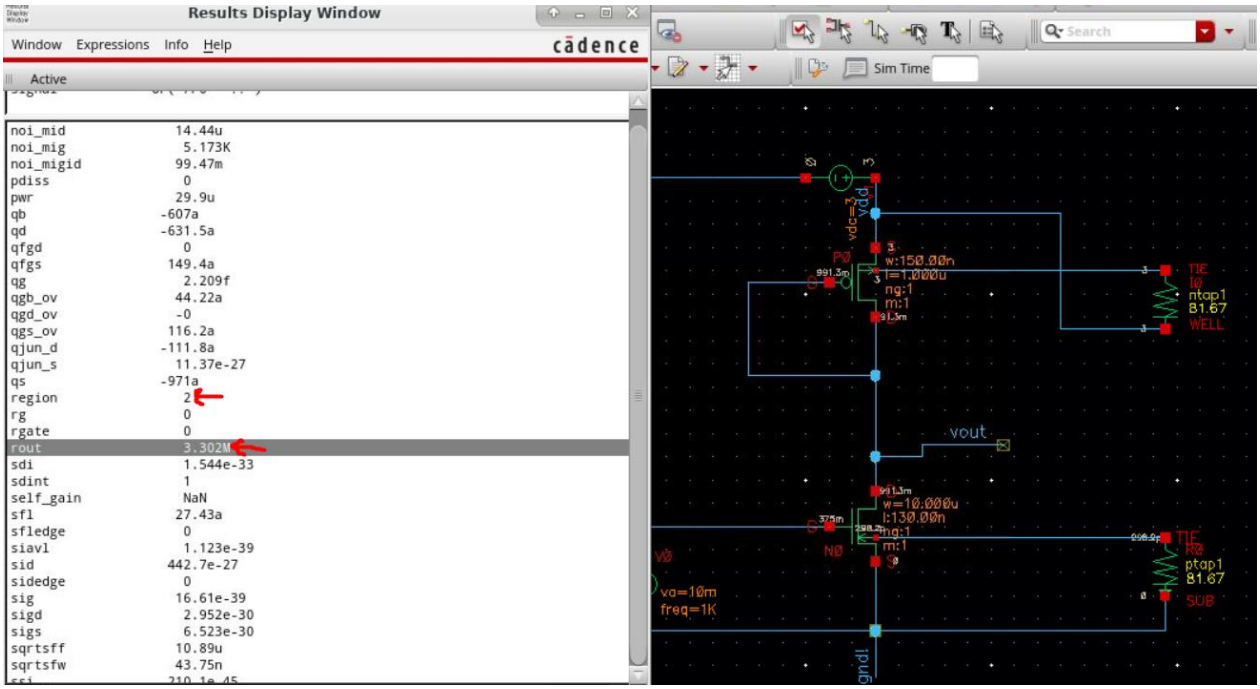
B) Simulation Results

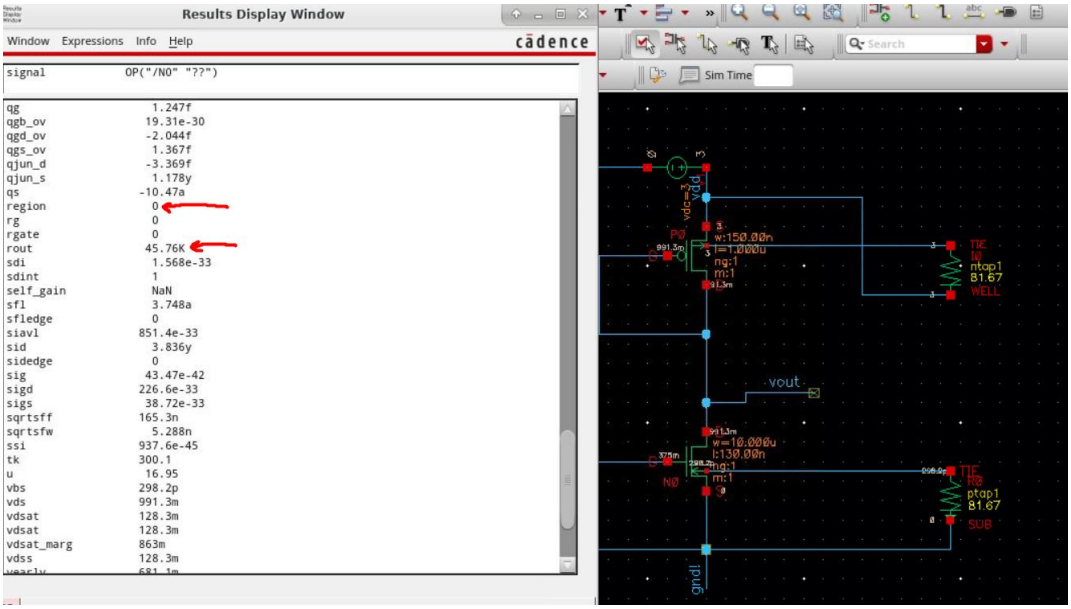
This time amplifier is less perfect. I could have decreased the width of the bottom mosfet and increased the length of the top mosfet more to decrease gate capacitance of the amplifier but that would decrease the current more and increase the effective resistance of the top mosfet more which is something I want to avoid.

DC results:



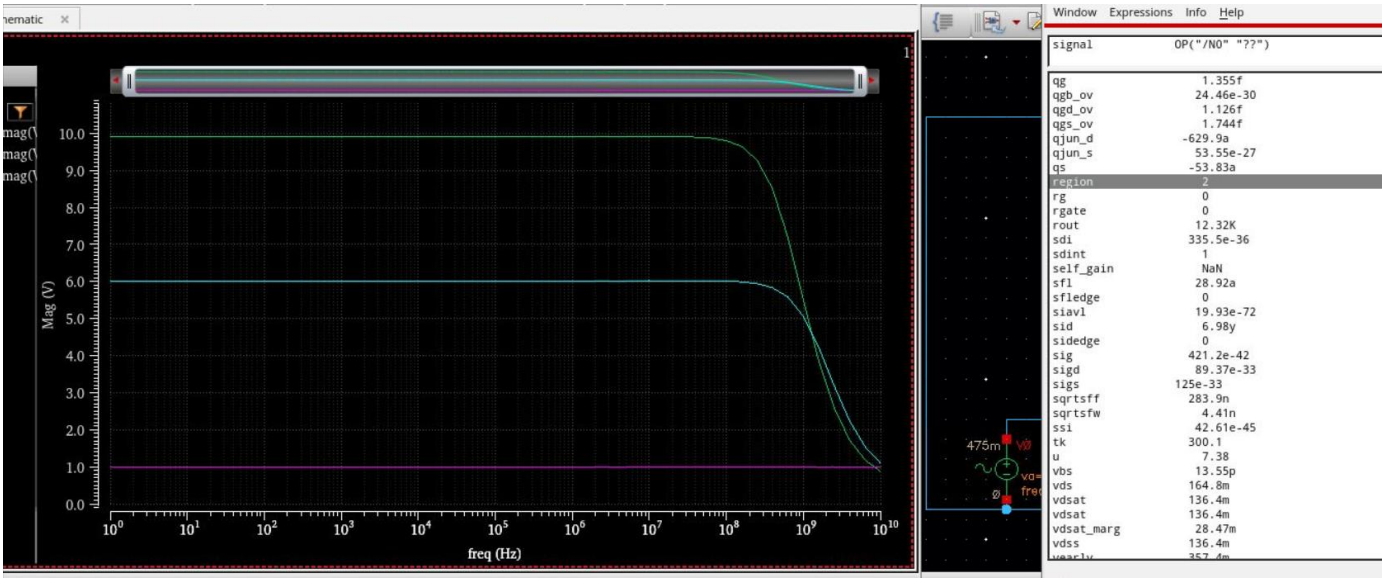
Region and ro of PMOS





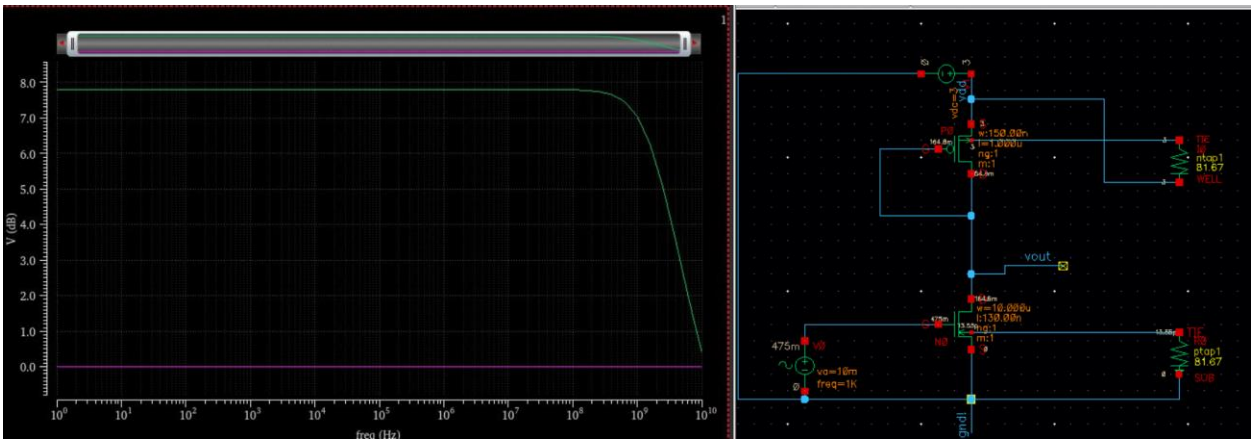
It turns out bottom mosfet was in cutoff mode instead of saturation.

This explains the inaccuracies I had while checking. Will increase Vbias from 375mV to something higher. The exponential gain characteristics of cutoff region made me think I was in saturation instead.



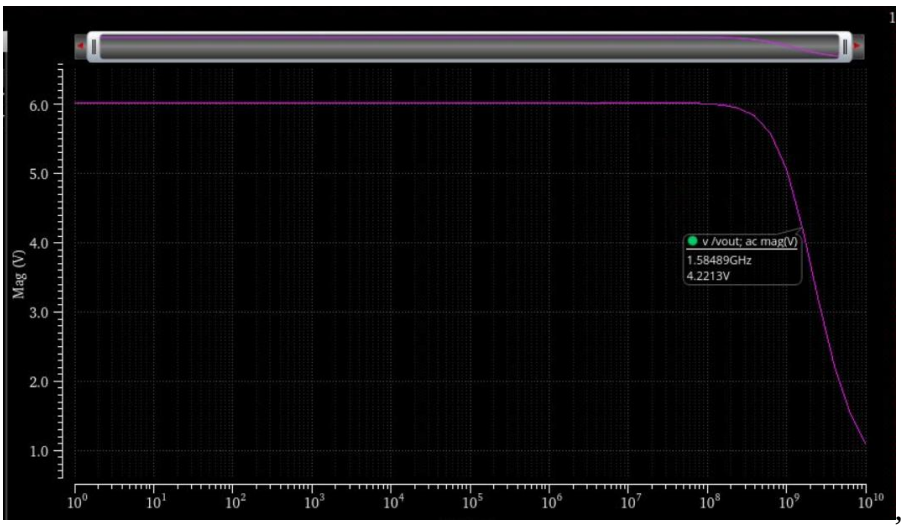
Setting bias to 475mV puts it in saturation mode. 500mV puts it in triode and 450mV puts it in cutoff. Regions are very close to each other. There is the possibility of Cadence assuming it is cutoff region even though it isn't because my gain dropped to 6 from 10. To be fair there is no instructions to have to bottom NMOS in saturation mode and it seems like I can not really change anything to get it in saturation mode and have 10 times gain at the same time. For these reasons I will go back to Vbias of 375mV and have 10 times gain in cutoff mode. Also check

how low r0 is at 12Kohms. Increasing the top transistor length to decrease current wouldn't increase the gain at all.



Running same simulation at dB gave me 7.8dB gain this time instead of 6V/V. Cutoff frequency is much lower because of the maximum 10n width. I will check the point where 6V gain drops to 4.24 to find the 3dB point because working with dB confuses me.

$$\left|\frac{6}{\sqrt{2}}\right| = 4.242640687$$



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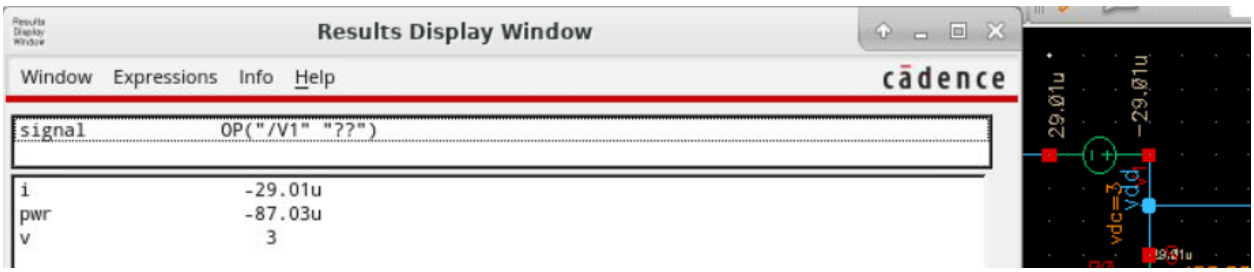
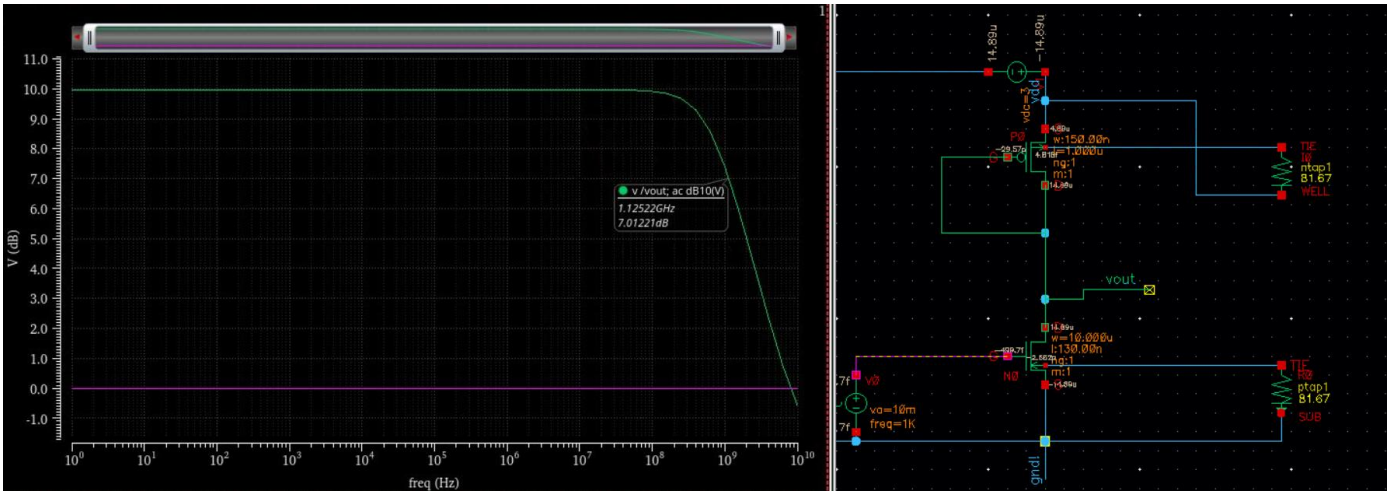
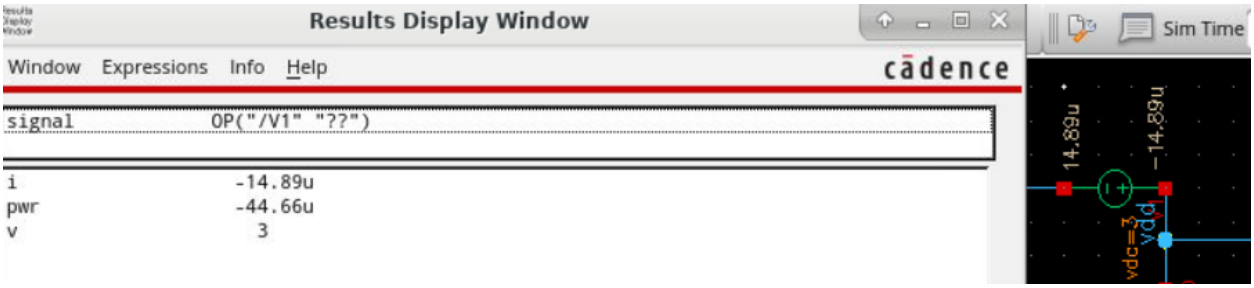


Power is 87uW

$$\frac{\left(6 \cdot 1.58 \cdot 10^{3}\right)}{87} = 108.9655172$$

When it is working in saturation mode FOM is 108. Much worse than the resistor load but 10 times the requirement anyway. Since 6 times gain is too low I will go back to original circuit and test again.





FOM =

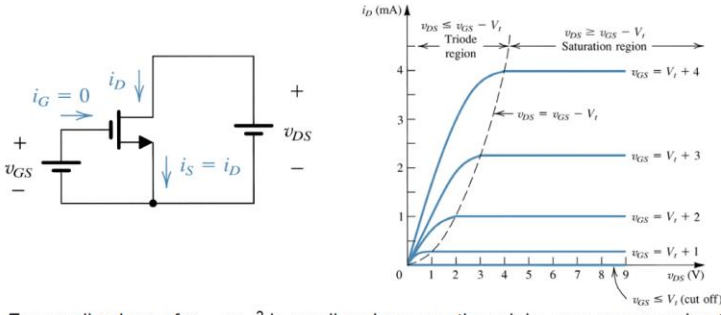
$$\frac{\left(10 \cdot 1.12 \cdot 10^{3}\right)}{44.66} = 250.7836991$$

Much better performance.

3) MOS Load Operating in Triode Region

A) Schematic Design

Only change I need to do is to remove the gate connection of the PMOS from its drain and feed it another dc voltage to get it in triode region and have an equivalent resistance of 67K.

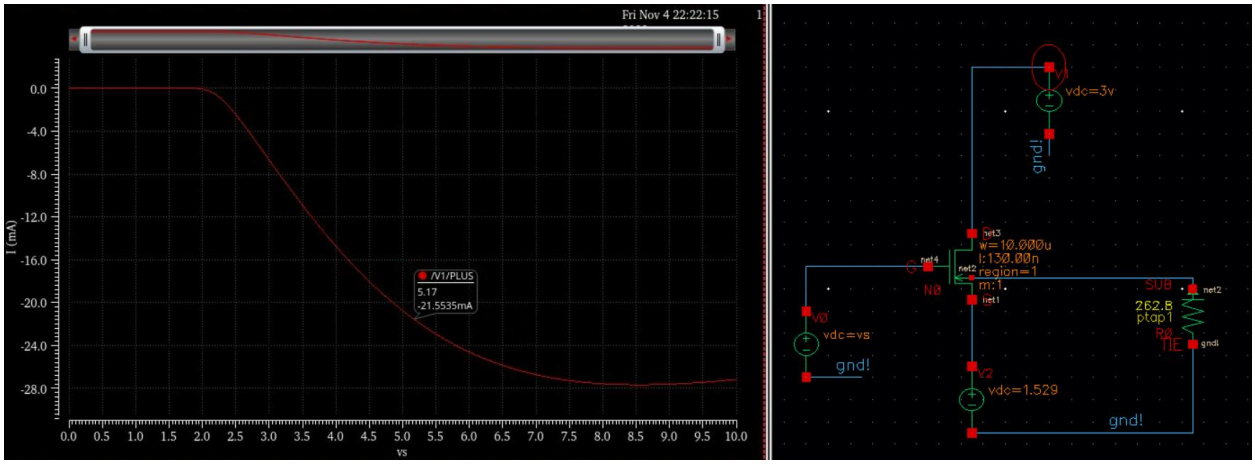


- For small values of v_{DS}, v_{DS}^2 is small and so near the origin, we can approximate the transistor as a linear resistor

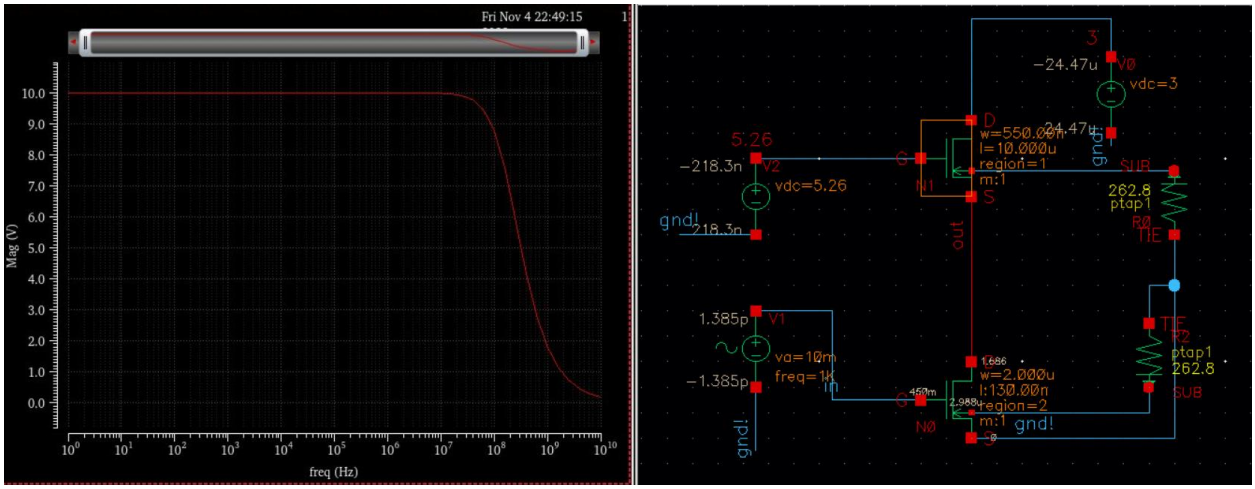
$$i_D = \mu_n C_{ox} \frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^{\ 2}\right] \Rightarrow i_D \cong \mu_n C_{ox} \frac{W}{L}(v_{GS} - V_t)v_{DS} \text{ when } v_{DS} \text{ is small}$$

$$\Rightarrow r_{DS} \equiv \frac{vDS}{iD} = \left[\mu_n C_{ox} \frac{W}{L}(v_{GS} - V_t)\right]^{-1}$$

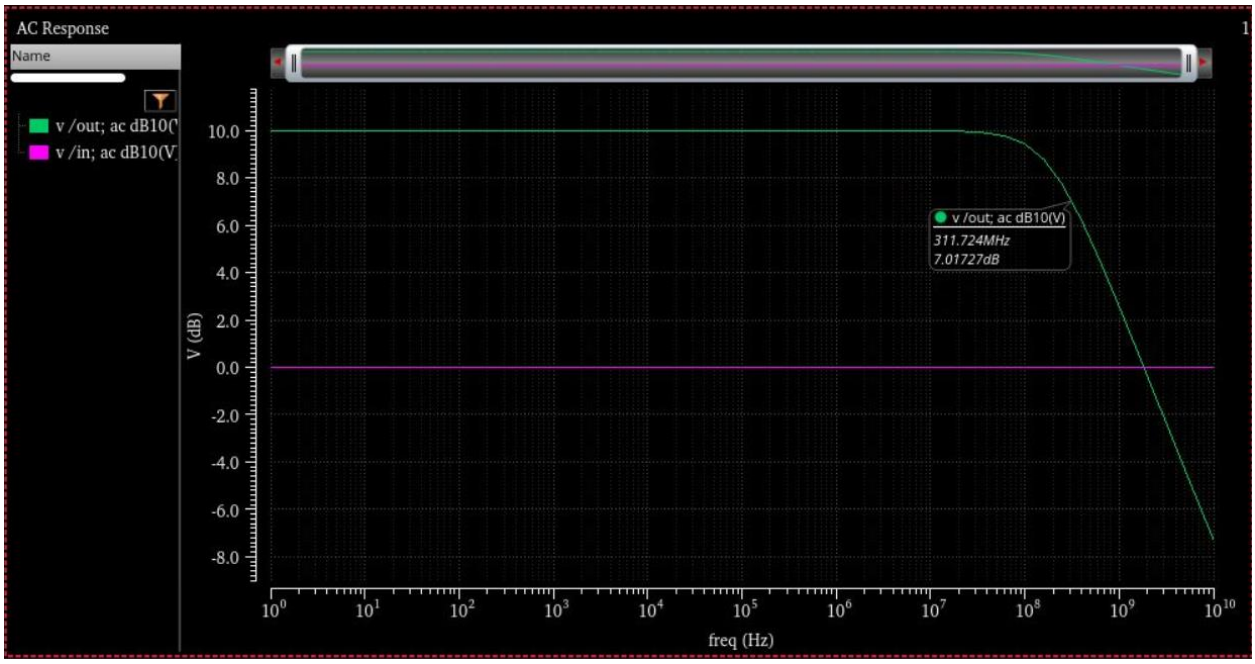
Easiest solution is using the inverter setup without Rd and sweeping gate voltage and seeing when current gets to 21.95uA on the mosfet same with the 67K resistor load.

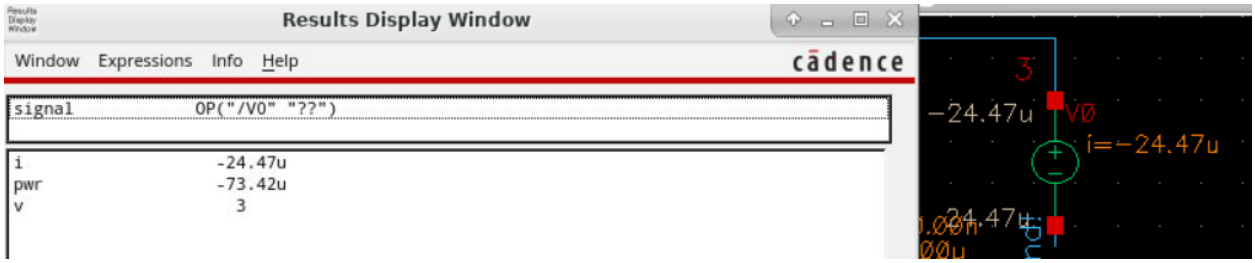


According to simulation ideal bias should be around 5.26V for NMOS to act like a 67K resistor in triode mode. In theory I should be able to replace this with the drain resistor resistor load amplifier and have identical results.



For some reason using mosfet with long width did not gave me any gain. Which did not make sense since it worked when I tested it separately. Before giving up I tried increasing the length instead. This worked splendidly.





FOM =

$$\frac{(10 \cdot 311.7)}{73.42} = 42.45437211$$

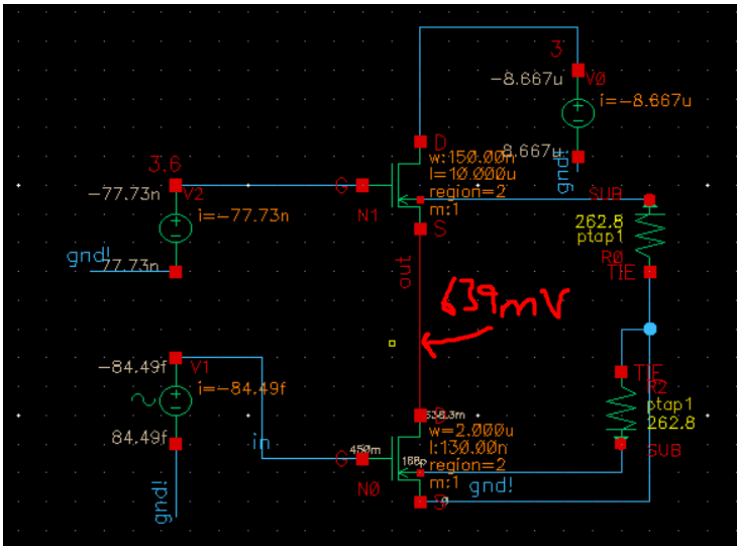
Around 2.5V Vg must be the value I need in order to NMOS to act like a 67K resistor in triode mode.

4) Current Source Load

A) Schematic Design

Because 2. Circuit is already Current source load I will not go in details.

There is the NMOS only version I acquired from modifying 3. Circuit's Vbias voltage.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l=10.000u
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m:1
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TIE
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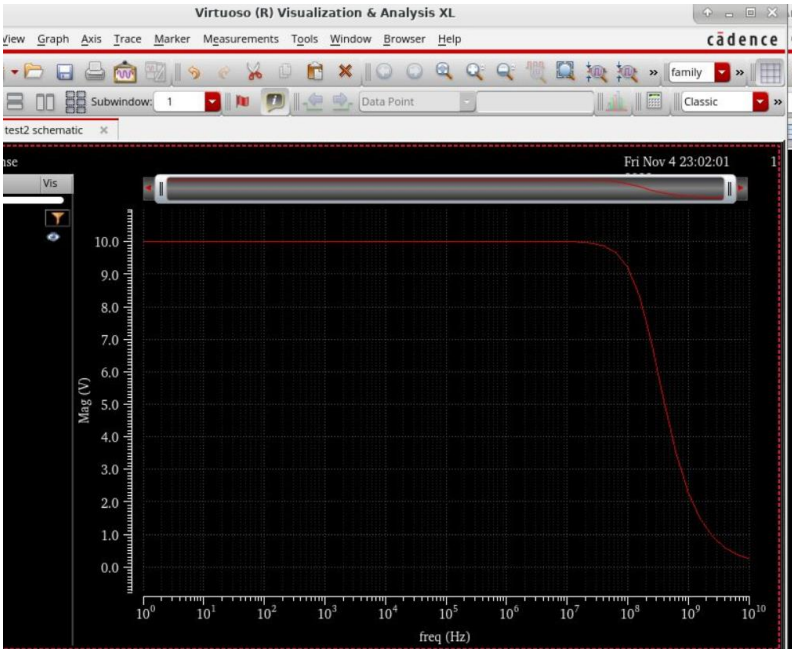
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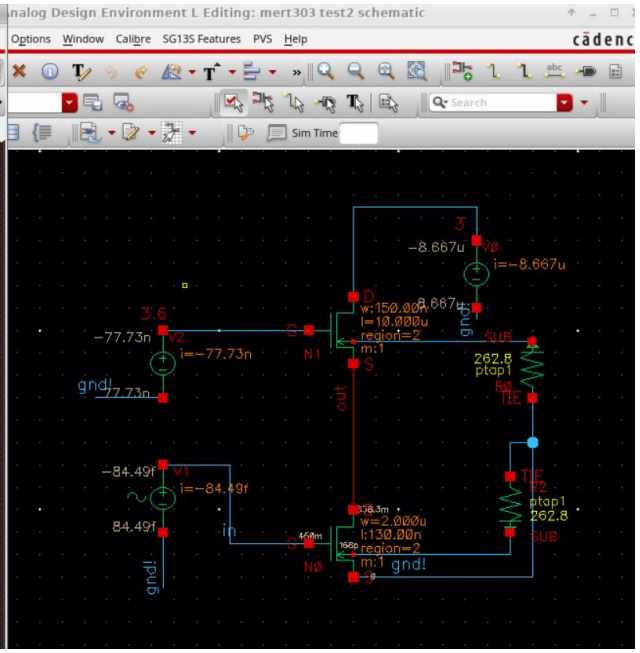
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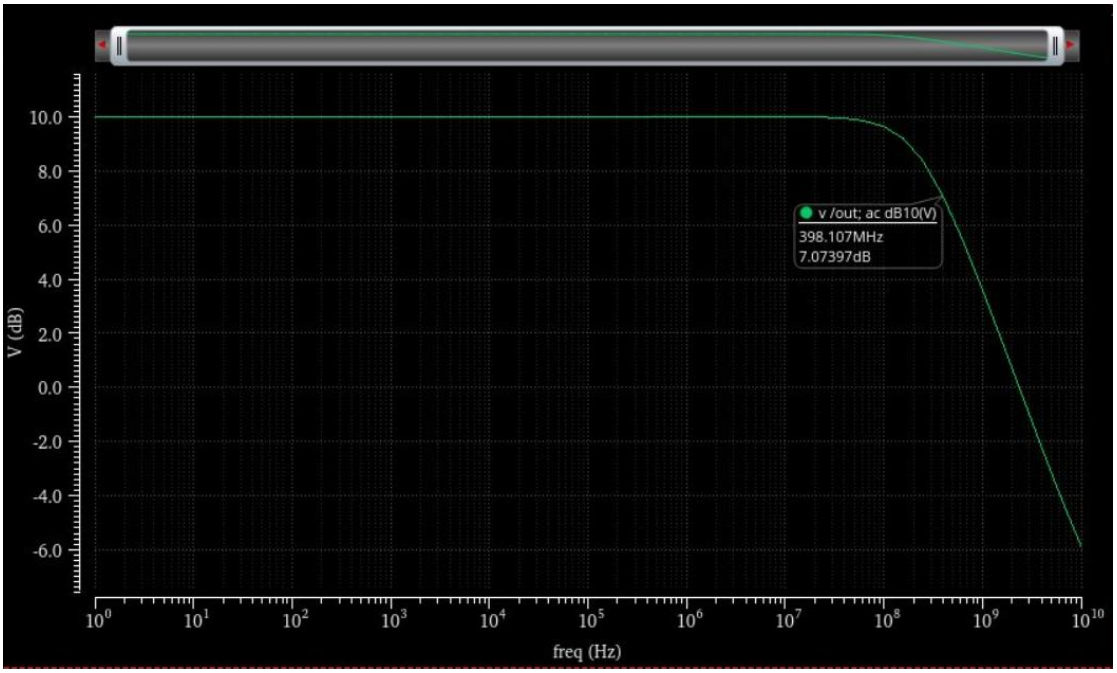

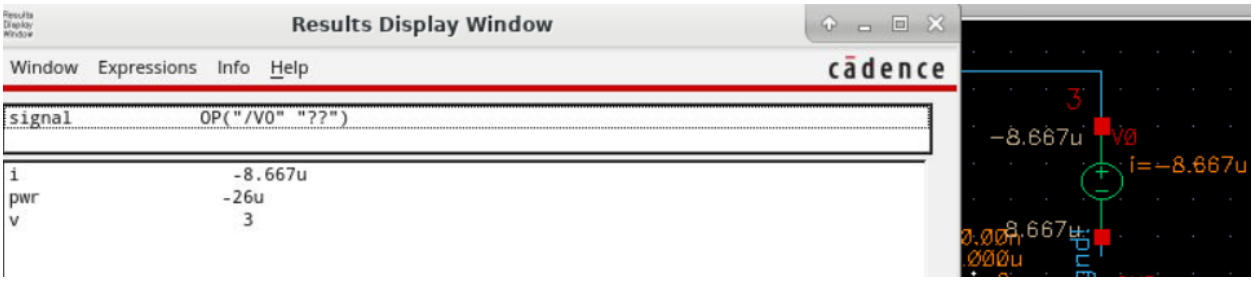

FOM =

$$\frac{(10 \cdot 400)}{73.42} = 54.48106783$$

Comparison of the Designed Amplifiers

In this part you will compare the designed amplifiers having different type of loads in terms of:

Power Consumption: Lowest power consumption was with NMOS load in saturation mode with 26uW.

Frequency Response: Best with resistor load at 5.7Ghz 3dB point

Output Voltage Swing Range: Best with resistor load since Vd was at the middle of supply range. 1.526V at 3V Vdd

Conclusion

Best amplifier was naturally the resistor load one because resistor always keeps it resistance stable in simulations but mosfets as loads are inconsistent and their Id values also change with output voltage. They also introduce lots of stray capacitances in the circuit. But in real life I know that making good resistors on silicon is difficult and expensive. And using CMOS is much better after carefully designing it. So, unless the device is going to be used for very high frequency high precision applications other solutions are more logical. Except triode load. Because it was both inefficient and had bad frequency response.