2. V_{CEO} — since $V_{CE(Q2)}$ is equal to $V_{in1(max)}$ when the output is shorted or during start up:

$$V_{CEO(Q2)} \leq V_{in1(max)} \quad (4.5)$$

3. h_{fe} — the minimum DC current gain for Q2 in Figures 4–1A and 4–1B is given by:

$$h_{fe(min)(Q2)} \geq \frac{I_{C(max)(Q2)}}{I_{B(max)(Q2)}} @ V_{CE} = (V_{in1(min)} - V_O) \quad (4.6)$$

4. Maximum Power Dissipation $P_{D(max)}$, and Safe Operating Area (SOA)

For any transistor there are certain combinations of I_C and V_{CE} at which it may safely be operated. When plotted on a graph, whose axes are V_{CE} and I_C, a safe–operating region is formed.

As an example, the safe–operating–area (SOA) curve for the well known 2N3055 NPN silicon power transistor is shown in Figure 4–2. The boundaries of the SOA curve are formed by $I_{C(max)}$, power dissipation, second breakdown and V_{CEO} ratings of the transistor. Notice that the power dissipation and second breakdown ratings are given for a case temperature of +25°C and must be derated at higher case temperatures. (Derating factors may be found in the transistors' data sheets.) These boundaries must never be exceeded during operation, or destruction of the transistor(s) which constitute the pass element may result. (In addition, the maximum operating junction temperature *must not be exceeded*, see Section 15.)

C. Current Limiting Techniques

In order to select a transistor or transistors with adequate SOA, the locus of pass element I_C and V_{CE} operating points must be known. This locus of points is determined by the input voltage (V_{in1}, output voltage (V_O), output current (I_O) and the type of output current limiting technique employed.

In most cases, V_{in1}, V_O, and the required output current are already known. All that is left to determine is how the chosen current limit scheme affects required pass element SOA.

Note, since the external pass element is merely an extension of the IC regulator, the following discussions apply equally well to IC regulators not using an external pass element.

1. Constant Current Limiting

This method is the simplest to implement and is extensively used, especially at the lower output current levels. The basic circuit configuration is shown in Figure 4–3A, and operates in the following manner.

As the output current increases, the voltage drop across R_{SC} increases, proportionately. When the output current has increased to the point that the voltage drop across R_{SC} is equal to the base–emitter ON voltage of Q3 (V_{BEon}(Q3)), Q3 conducts. This diverts base current (I_{Drive}) away from Q1, the IC regulator's internal series pass element. Base drive ($I_{B(Q2)}$) of Q2 is therefore reduced and its collector–emitter voltage increases, thereby reducing the output voltage below its regulated value, V_{out}. The resulting output voltage–current characteristic is shown in Figure 4–3B.

The value of I_{SC} is given by:

$$I_{SC} = \frac{V_{BEon(Q3)}}{R_{SC}} \quad (4.7)$$

Figure 4–2. 2N3055 Safe Operating Area (SOA)

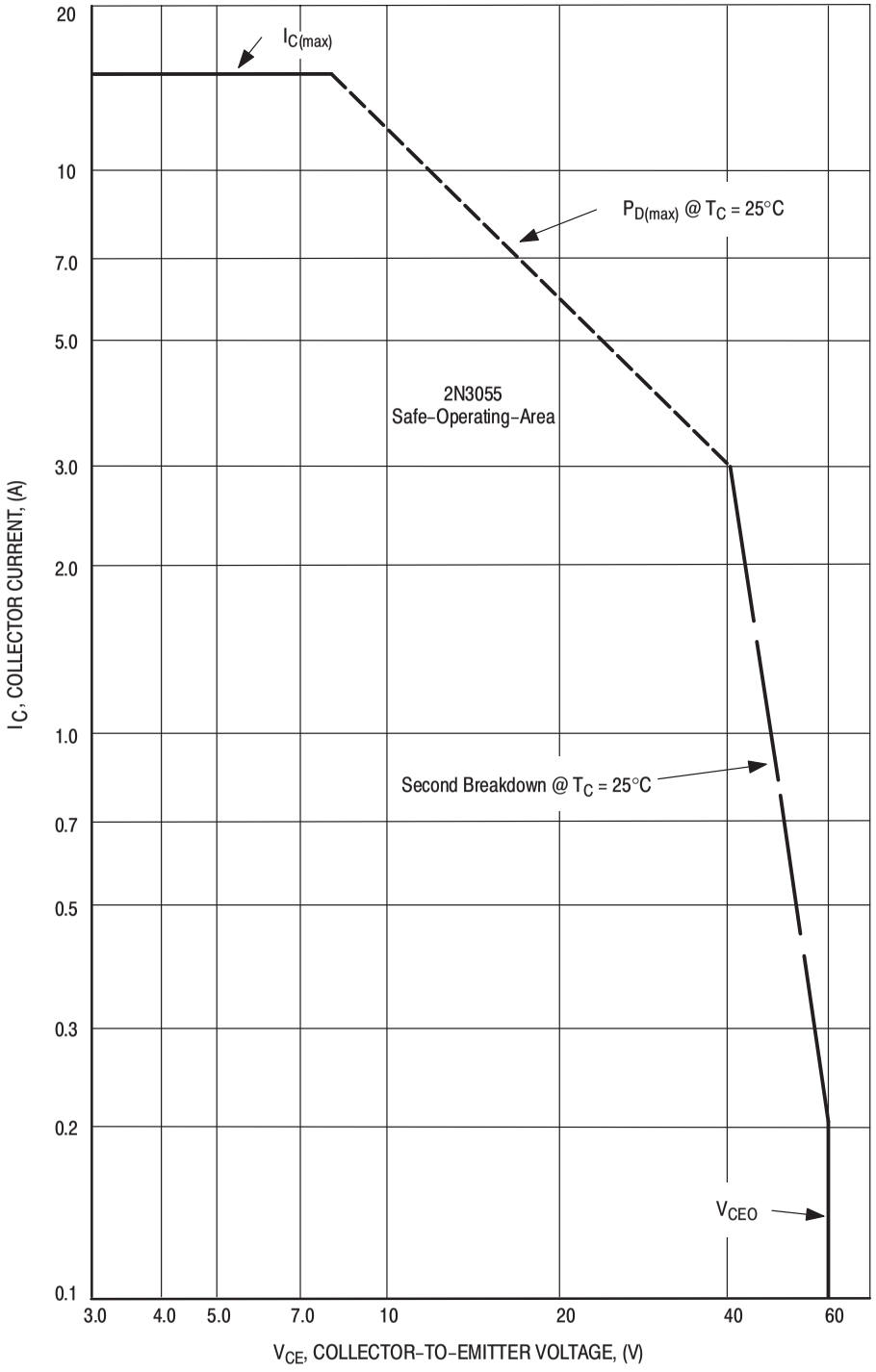
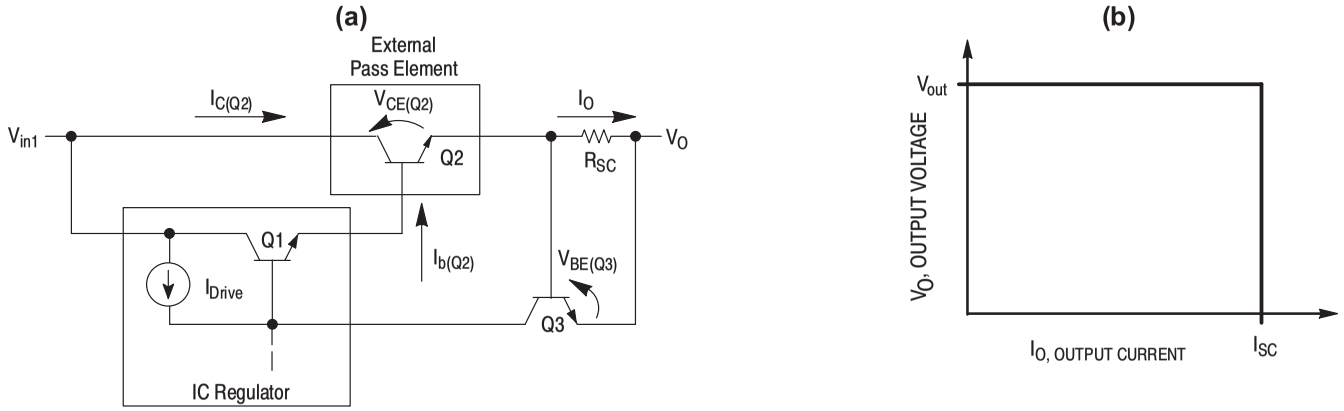


Figure 4–3. Constant Current Limiting



By using the base of Q1 in the IC regulator as a control point, this configuration has the added benefit of limiting the IC regulator output current ($I_{B(Q2)}$) to $Isc/h_{fe(Q2)}$, as well as limiting the collector current of Q2 to I_{SC}. Of course, access to this point is necessary. Fortunately, it is usually available in the form of a separate pin or as the regulator's compensation terminal.(1)

The required safe–operating–area for Q2 can be obtained by plotting the V_{CE} and I_C of Q2 given by:

$$V_{CE(Q2)} = V_{in1} - V_O - I_O R_{SC} \simeq V_{in1} - V_O \quad (4.8)$$

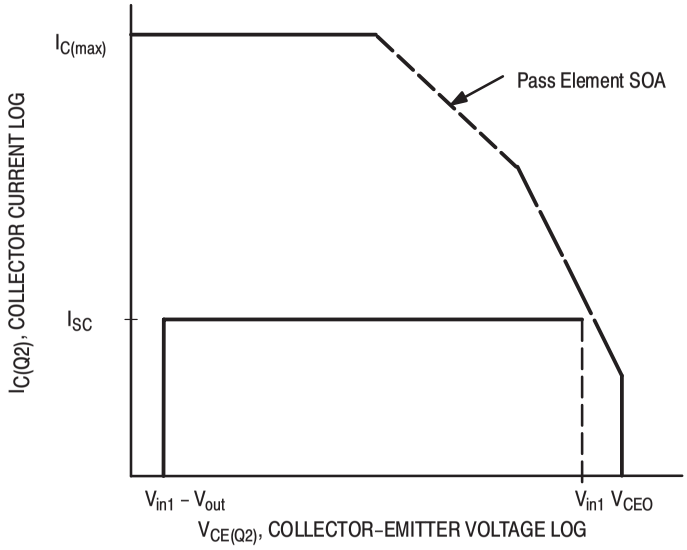
$$I_{C(Q2)} \simeq I_O \quad (4.9)$$

$$\text{where, } V_O = V_{out} \text{ for } 0 \le I_O \le I_{SC} \quad (4.10)$$

$$\text{and, } I_O = I_{SC} \text{ for } 0 \le V_O \le V_{out} \quad (4.11)$$

The resulting plot is shown in Figure 4–4. The transistor chosen for Q2 must have an SOA which encloses this plot, see Figure 4–4. Note that the greatest demand on the transistor's SOA capability occurs when the output of the regulator is short circuited and the pass element must support the full input voltage and short circuit current simultaneously.

Figure 4–4. Constant Current Limit SOA Requirements
(See Section 3 for Circuit Techniques)



(1) The three–terminal regulators have internal current limiting and therefore do not provide access to this point. If an external pass element is used with these regulators, constant current limiting can still be accomplished by diverting pass element drive.