

ZZZ1
PCB
MTDAZ@

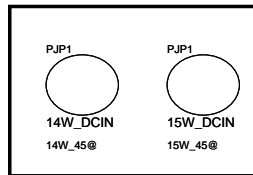
04/27 Add PCB Panel P/N for MTDAAZ@
04/27 Add PCB Panel P/N DAZ01S00100
07/09 Change PCB Panel P/N from DAZ01S00100 to DAZ01S00200

ZZZ25
PCB
FBDAAZ@

03/28 Change PCB Panel PN from DAZ01W00101 to DAZ01Q00101
04/18 Change PCB Panel PN from DAZ01Q00101 to DAZ01Q00102
04/26 Change PCB Panel from DAZ@ to A30DAZ@
04/27 Change PCB Panel from A30DAZ@ to FBDAAZ@
05/03 Change PCB Panel from DAZ01Q00102 to DAZ01Q00103
07/09 Change PCB Panel P/N from DAZ01Q00103 to DAZ01Q00200

ZZZ26
PCB
HSDAAZ@

04/27 Add PCB Panel P/N for HSDAAZ@
07/09 Change PCB Panel P/N from DAZ01W00102 to DAZ01W00103



12/21 Add PJP1 for DCIN Cable on 45 Level
One for 14W DCIN , PN: DC301001Y00
Another for 15W DCIN , PN: DC301001V00

Compal Confidential

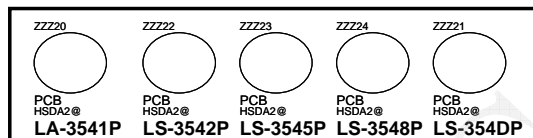
IFXXX Schematics Document

Intel Merom Processor with Crestline + DDRII + ICH8M

(With nVIDIA MXM/B)

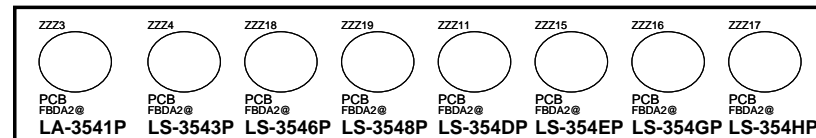
2008-04-11

REV: 2.0



04/27 Add LS-3542P,LS-3545P for HSDA2@

11/19 Change PCB from DA600004S1A to DA600004S20

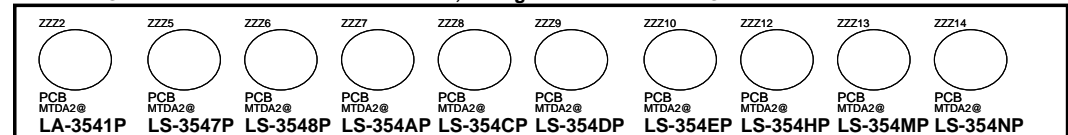


04/18 Change LA-3541P P/N from DA600004S10 to DA600004S1A 04/27 Change PCB from DA2@ to FBDAAZ@

04/18 Change LS-3543P P/N from DA200008810 to DA20000881A

04/18 Change LS-354HP P/N from DA200008110 to DA400007F1A

07/09 Change LS-354MP MTDAAZ@ from DA200009900 to DA200009910 , Change LS-354NP MTDAAZ@ from DA200009A00 to DA200009A10



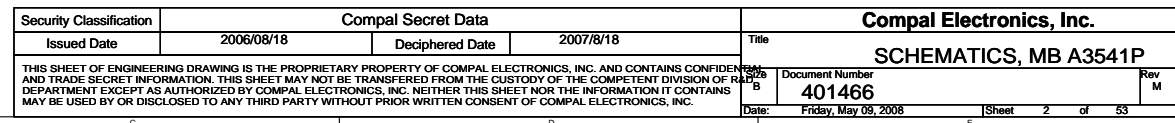
05/14 Change PCB from DA600006000 to DA600004S1A

04/27 Change PCB from DA2@ to MTDAAZ@

04/27 Add LS-354MP,LS-354NP for MTDAAZ@

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Model Name : IFTXX
File Name : LA-3541P



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS (Actual +0.9V)	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSb always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

PROJECT ID Table

	ID1	ID0
IFT00 (00@)	R284	R283
IFT01 (01@)	R284	R281
IFL90 (10@)	R694	R283
IFT91 (11@)	R694	R281

BOARD ID Table

R	Structure
Ra (R743)	15W@
Rb (R740)	14W@

MIC ID Table

R	Structure
R785 Single MIC	INT@
R786 Array MIC	DUAL@

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
CARD BUS CB1410	AD20	2	C,D
1394+Cardreader	AD22	0	G,H

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b	NVIDIA NB8X	

EC SM Bus2 address

ICH8M SM Bus address

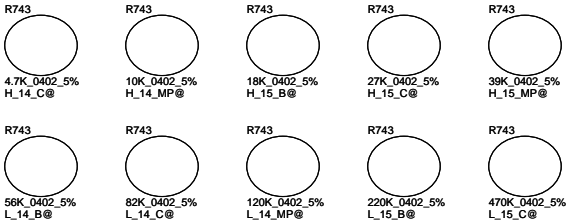
Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM1	1010 010Xb

SKU ID Table

Vcc	3.3V +/- 5%
Rb	47K +/- 5%

Rb~ R740

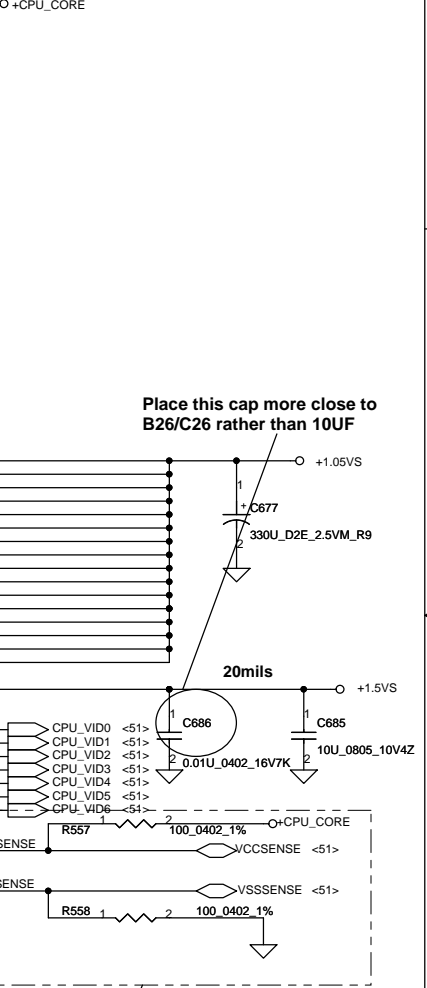
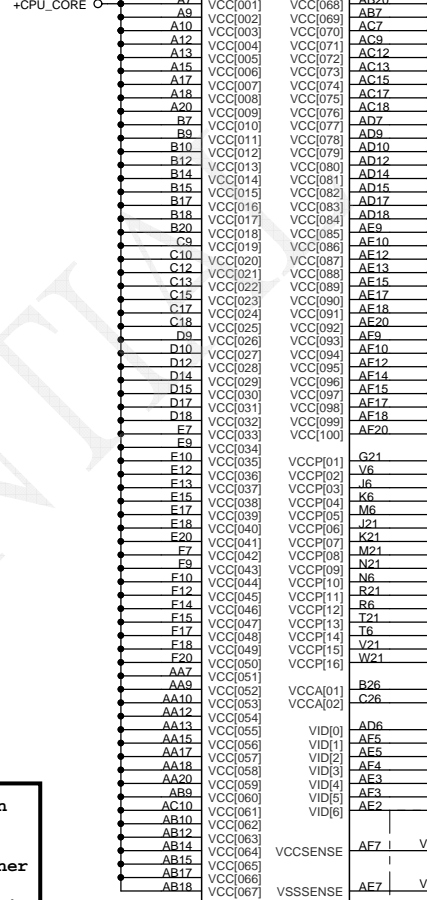
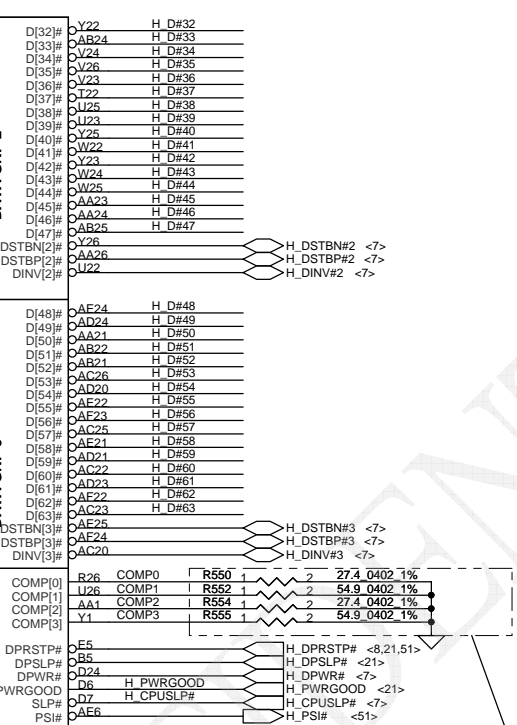
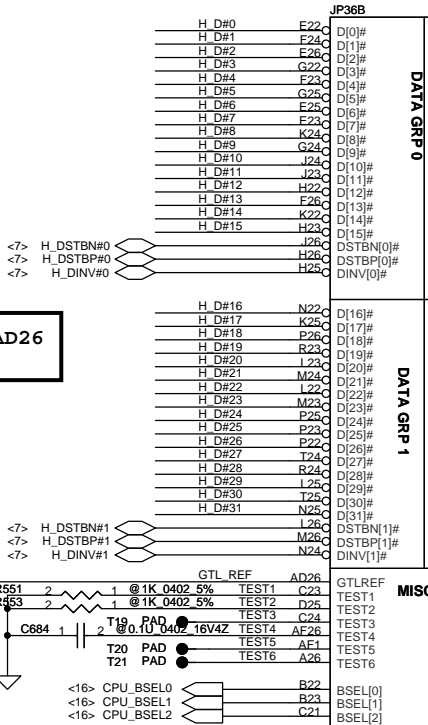
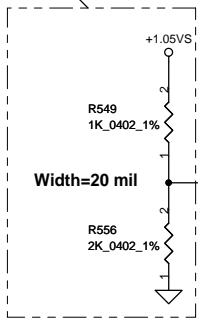
Ra~ R743



Board ID	Rb	Ra	VAD_BID min	VAD_BID typ	VAD_BID max	Ra BOM Structure
1	NA	4.7K +/- 5%	0 V	0 V	0 V	H_14_B@
2	47K(RB@)	4.7K +/- 5%	0.274 V	0.300 V	0.328 V	H_14_C@
3	47K(RB@)	10K +/- 5%	0.553V	0.578 V	0.628 V	H_14_MP@ ✓
4	47K(RB@)	18K +/- 5%	0.849V	0.913V	0.981 V	H_15_B@
5	47K(RB@)	27K +/- 5%	1.129 V	1.204 V	1.282 V	H_15_C@
6	47K(RB@)	39K +/- 5%	1.415 V	1.496 V	1.579 V	H_15_MP@ ✓
7	47K(RB@)	56K +/- 5%	1.712 V	1.794 V	1.876 V	L_14_B@
8	47K(RB@)	82K +/- 5%	2.020V	2.097 V	2.173 V	L_14_C@
9	47K(RB@)	120K +/- 5%	2.303 V	2.371 V	2.437 V	L_14_MP@ ✓
10	47K(RB@)	220K +/- 5%	2.670 V	2.719 V	2.765 V	L_15_B@
11	47K(RB@)	470K +/- 5%	2.972 V	3.000 V	3.026 V	L_15_C@
12	47K(RB@)	NA	3.135 V	3.300 V	3.465 V	NA for L_15_MP@ ✓

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Close to CPU pin AD26
within 500mils.



Place this cap more close to
B26/C26 rather than 10UF

Resistor placed within
0.5" of CPU pin. Trace
should be at least 25
mils away from any other
toggling signal.
COMP[0,2] trace width is
18 mils. COMP[1,3] trace
width is 4 mils.

Length match within 25 mils.
The trace width/space/other is
20/7/25.

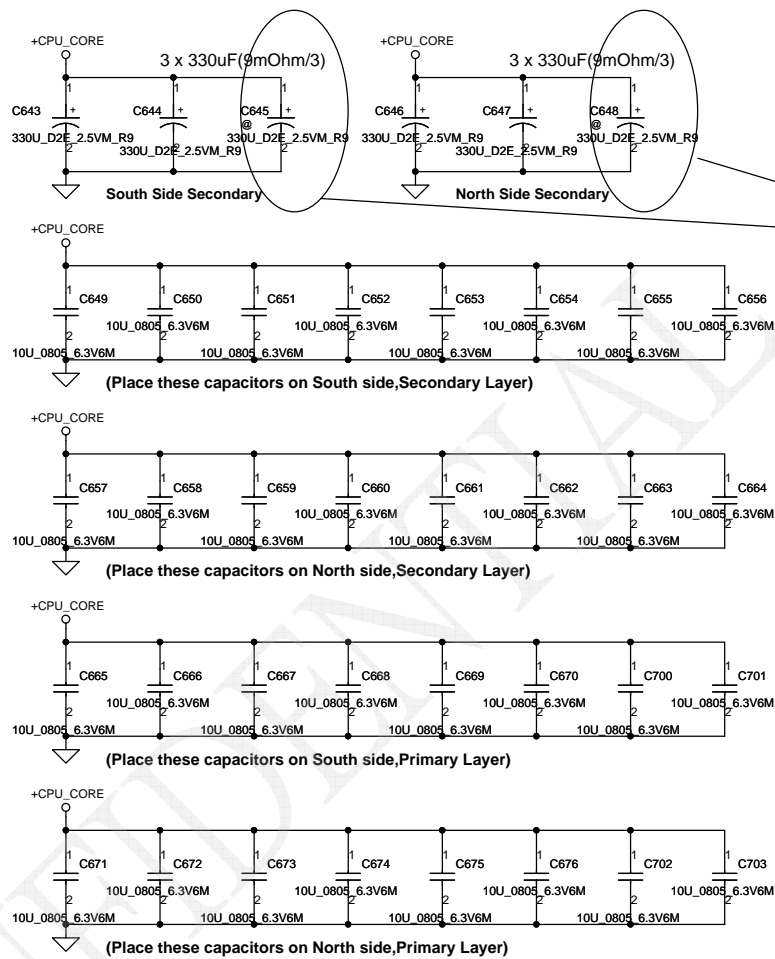
Close to CPU pin
within 500mils.

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

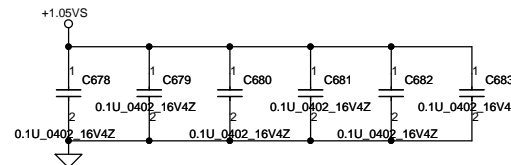
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

JP36D			
A4	VSS[001]	VSS[082]	P6
A8	VSS[002]	VSS[083]	P21
A11	VSS[003]	VSS[084]	P24
A14	VSS[004]	VSS[085]	R2
A16	VSS[005]	VSS[086]	R5
A19	VSS[006]	VSS[087]	R22
A23	VSS[007]	VSS[088]	R25
AE2	VSS[008]	VSS[089]	T1
B6	VSS[009]	VSS[090]	T4
B8	VSS[010]	VSS[091]	T23
B11	VSS[011]	VSS[092]	T26
B13	VSS[012]	VSS[093]	U3
B16	VSS[013]	VSS[094]	U6
B19	VSS[014]	VSS[095]	U21
B21	VSS[015]	VSS[096]	U24
B24	VSS[016]	VSS[097]	V2
C5	VSS[017]	VSS[098]	V5
C8	VSS[018]	VSS[099]	V22
C11	VSS[019]	VSS[100]	V25
C14	VSS[020]	VSS[101]	W1
C16	VSS[021]	VSS[102]	W4
C19	VSS[022]	VSS[103]	W23
C2	VSS[023]	VSS[104]	W26
C22	VSS[024]	VSS[105]	Y3
C25	VSS[025]	VSS[106]	Y6
D1	VSS[026]	VSS[107]	Y21
D4	VSS[027]	VSS[108]	Y24
D8	VSS[028]	VSS[109]	AA5
D11	VSS[029]	VSS[110]	AA8
D13	VSS[030]	VSS[111]	AA11
D16	VSS[031]	VSS[112]	AA14
D19	VSS[032]	VSS[113]	AA16
D23	VSS[033]	VSS[114]	AA19
D26	VSS[034]	VSS[115]	AA22
E3	VSS[035]	VSS[116]	AA25
E6	VSS[036]	VSS[117]	AB1
E8	VSS[037]	VSS[118]	AB4
F11	VSS[038]	VSS[119]	AB8
F14	VSS[039]	VSS[120]	AB11
F16	VSS[040]	VSS[121]	AB13
F19	VSS[041]	VSS[122]	AB16
F21	VSS[042]	VSS[123]	AB19
F24	VSS[043]	VSS[124]	AB23
F5	VSS[044]	VSS[125]	AB26
F8	VSS[045]	VSS[126]	AC3
F11	VSS[046]	VSS[127]	AC6
F13	VSS[047]	VSS[128]	AC8
F16	VSS[048]	VSS[129]	AC11
F19	VSS[049]	VSS[130]	AC14
F2	VSS[050]	VSS[131]	AC16
F22	VSS[051]	VSS[132]	AC19
F25	VSS[052]	VSS[133]	AC21
G4	VSS[053]	VSS[134]	AC24
G1	VSS[054]	VSS[135]	AD2
G23	VSS[055]	VSS[136]	AD5
G26	VSS[056]	VSS[137]	AD8
H3	VSS[057]	VSS[138]	AD11
H6	VSS[058]	VSS[139]	AD13
H21	VSS[059]	VSS[140]	AD16
H24	VSS[060]	VSS[141]	AD19
J2	VSS[061]	VSS[142]	AD22
J22	VSS[062]	VSS[143]	AD25
J25	VSS[063]	VSS[144]	AE1
J25	VSS[064]	VSS[145]	AE4
K1	VSS[065]	VSS[146]	AE8
K4	VSS[066]	VSS[147]	AE11
K23	VSS[067]	VSS[148]	AE14
K26	VSS[068]	VSS[149]	AE16
L3	VSS[069]	VSS[150]	AE19
L6	VSS[070]	VSS[151]	AE23
L21	VSS[071]	VSS[152]	AE26
L24	VSS[072]	VSS[153]	A2
M2	VSS[073]	VSS[154]	AF6
M5	VSS[074]	VSS[155]	AF8
M22	VSS[075]	VSS[156]	AF11
M25	VSS[076]	VSS[157]	AF13
N1	VSS[077]	VSS[158]	AF16
N4	VSS[078]	VSS[159]	AF19
N23	VSS[079]	VSS[160]	AF21
N26	VSS[080]	VSS[161]	A25
P3	VSS[081]	VSS[162]	AF25
		VSS[163]	

Merom Ball-out Rev 1a
conn@

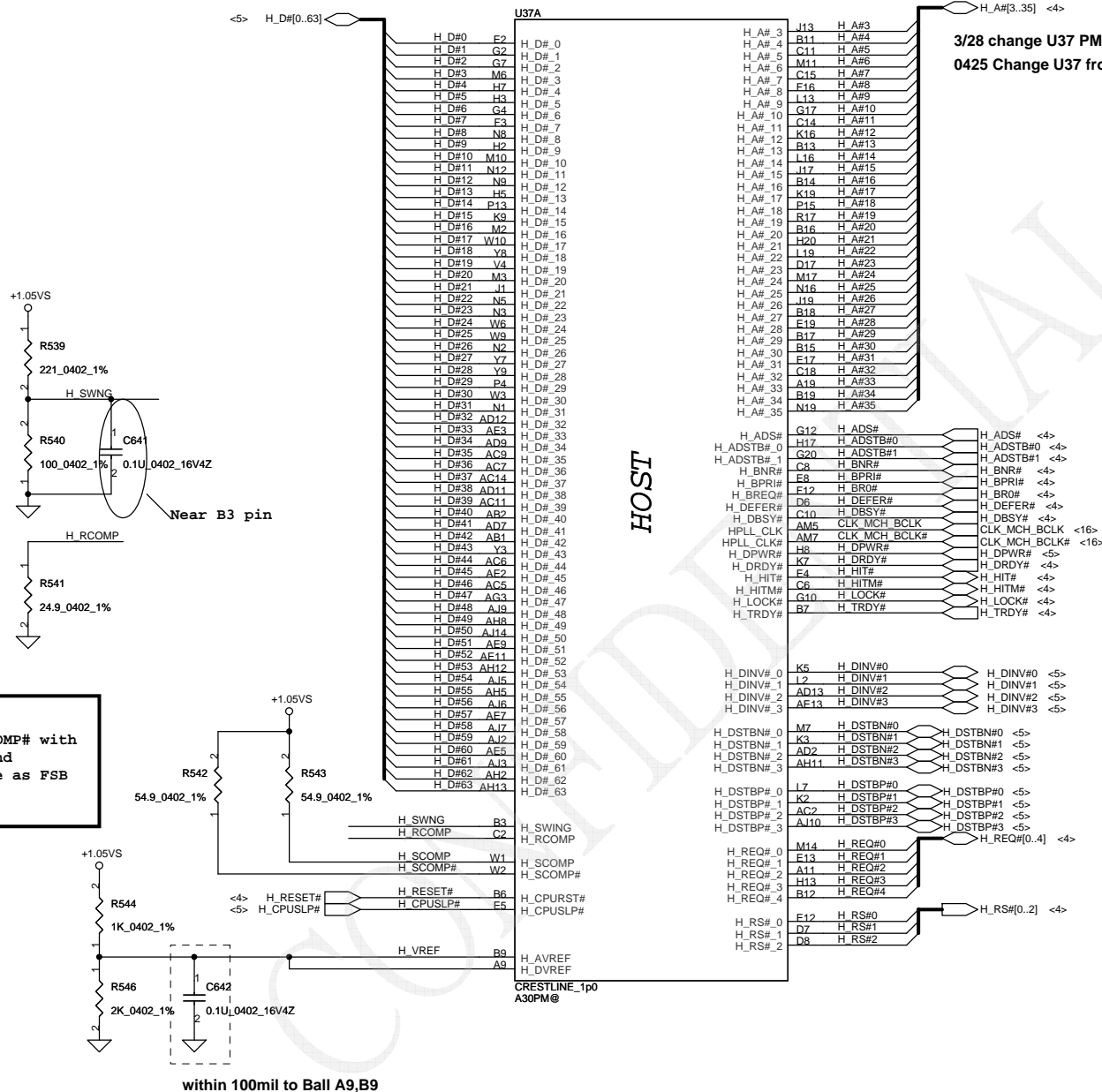


+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



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1/2 change U37 PM part number to SA00001DJ90 3/21 change U37 PM part number to SA00001DJE0



layout note:
Route H_SCOMP and H_SCOMP# with
trace width, spacing and
impedance (55 ohm) same as FSB
data traces

Layout Note:
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20

1/2 change U37 GM part number to SA00000ZW80
3/21 change U37 GM part number to SA00000ZWF0
3/28 change U37 GM part number to SA00000ZWK0 for 030
0425 Change U37 from GM@ to A30GM@

0425 Add U37 part number for HSPM@ , HSGM@

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<14> DDRA_SDQ[0..63] DDRA_SDQ[0..63]
<14> DDRA_SDM[0..7] DDRA_SDM[0..7]
<14> DDRA_SMA[0..13] DDRA_SMA[0..13]

<15> DDRB_SDQ[0..63] DDRB_SDQ[0..63]
<15> DDRB_SDM[0..7] DDRB_SDM[0..7]
<15> DDRB_SMA[0..13] DDRB_SMA[0..13]

U37D
DDRA_SDQ0 AR43 SA_DQ_0
DDRA_SDQ1 AW44 SA_DQ_1
DDRA_SDQ2 BA45 SA_DQ_2
DDRA_SDQ3 AY46 SA_DQ_3
DDRA_SDQ4 AB41 SA_DQ_4
DDRA_SDQ5 AR45 SA_DQ_5
DDRA_SDQ6 AT42 SA_DQ_6
DDRA_SDQ7 AW47 SA_DQ_7
DDRA_SDQ8 BB45 SA_DQ_8
DDRA_SDQ9 BF48 SA_DQ_9
DDRA_SDQ10 BQ47 SA_DQ_10
DDRA_SDQ11 B145 SA_DQ_11
DDRA_SDQ12 BB47 SA_DQ_12
DDRA_SDQ13 BG50 SA_DQ_13
DDRA_SDQ14 BH49 SA_DQ_14
DDRA_SDQ15 BE45 SA_DQ_15
DDRA_SDQ16 AW43 SA_DQ_16
DDRA_SDQ17 BE44 SA_DQ_17
DDRA_SDQ18 BG42 SA_DQ_18
DDRA_SDQ19 BE40 SA_DQ_19
DDRA_SDQ20 BF44 SA_DQ_20
DDRA_SDQ21 BH45 SA_DQ_21
DDRA_SDQ22 BG40 SA_DQ_22
DDRA_SDQ23 BE40 SA_DQ_23
DDRA_SDQ24 AB40 SA_DQ_24
DDRA_SDQ25 AW40 SA_DQ_25
DDRA_SDQ26 AT39 SA_DQ_26
DDRA_SDQ27 AW36 SA_DQ_27
DDRA_SDQ28 BQ42 SA_DQ_28
DDRA_SDQ29 AY41 SA_DQ_29
DDRA_SDQ30 AV38 SA_DQ_30
DDRA_SDQ31 AT38 SA_DQ_31
DDRA_SDQ32 AV33 SA_DQ_32
DDRA_SDQ33 AT13 SA_DQ_33
DDRA_SDQ34 AW11 SA_DQ_34
DDRA_SDQ35 AV11 SA_DQ_35
DDRA_SDQ36 AU15 SA_DQ_36
DDRA_SDQ37 AT11 SA_DQ_37
DDRA_SDQ38 BA13 SA_DQ_38
DDRA_SDQ39 BA11 SA_DQ_39
DDRA_SDQ40 BE10 SA_DQ_40
DDRA_SDQ41 BD10 SA_DQ_41
DDRA_SDQ42 BD8 SA_DQ_42
DDRA_SDQ43 AY9 SA_DQ_43
DDRA_SDQ44 BG10 SA_DQ_44
DDRA_SDQ45 AW9 SA_DQ_45
DDRA_SDQ46 BD7 SA_DQ_46
DDRA_SDQ47 BB9 SA_DQ_47
DDRA_SDQ48 BB5 SA_DQ_48
DDRA_SDQ49 AY7 SA_DQ_49
DDRA_SDQ50 AT5 SA_DQ_50
DDRA_SDQ51 AT7 SA_DQ_51
DDRA_SDQ52 AY6 SA_DQ_52
DDRA_SDQ53 BB7 SA_DQ_53
DDRA_SDQ54 AR5 SA_DQ_54
DDRA_SDQ55 AR8 SA_DQ_55
DDRA_SDQ56 AR9 SA_DQ_56
DDRA_SDQ57 AN3 SA_DQ_57
DDRA_SDQ58 AM8 SA_DQ_58
DDRA_SDQ59 AN10 SA_DQ_59
DDRA_SDQ60 AT9 SA_DQ_60
DDRA_SDQ61 AN9 SA_DQ_61
DDRA_SDQ62 AM9 SA_DQ_62
DDRA_SDQ63 AN11 SA_DQ_63

DDR SYSTEM MEMORY A

SA_BS_0 BB19 DDRA_SBS0 <14>
SA_BS_1 BK19 DDRA_SBS1 <14>
SA_BS_2 BE29 DDRA_SBS2 <14>
SA_CAS# BL17 DDRA_SCAS# <14>
SA_DM_0 AT45 DDRA_SDM0
SA_DM_1 BD44 DDRA_SDM1
SA_DM_2 BD42 DDRA_SDM2
SA_DM_3 AW38 DDRA_SDM3
SA_DM_4 AW13 DDRA_SDM4
SA_DM_5 BG8 DDRA_SDM5
SA_DM_6 AY5 DDRA_SDM6
SA_DM_7 AN6 DDRA_SDM7
SA_DQS_0 AT46 DDRA_SDQS0 DDRA_SDQS0 <14>
SA_DQS_1 BE48 DDRA_SDQS1 DDRA_SDQS1 <14>
SA_DQS_2 BB43 DDRA_SDQS2 DDRA_SDQS2 <14>
SA_DQS_3 BC37 DDRA_SDQS3 DDRA_SDQS3 <14>
SA_DQS_4 BB16 DDRA_SDQS4 DDRA_SDQS4 <14>
SA_DQS_5 BH6 DDRA_SDQS5 DDRA_SDQS5 <14>
SA_DQS_6 BB2 DDRA_SDQS6 DDRA_SDQS6 <14>
SA_DQS_7 AP3 DDRA_SDQS7 DDRA_SDQS7 <14>
SA_DQS#_0 AT47 DDRA_SDQS0# DDRA_SDQS0# <14>
SA_DQS#_1 BD47 DDRA_SDQS1# DDRA_SDQS1# <14>
SA_DQS#_2 BC41 DDRA_SDQS2# DDRA_SDQS2# <14>
SA_DQS#_3 BA37 DDRA_SDQS3# DDRA_SDQS3# <14>
SA_DQS#_4 BA16 DDRA_SDQS4# DDRA_SDQS4# <14>
SA_DQS#_5 BH7 DDRA_SDQS5# DDRA_SDQS5# <14>
SA_DQS#_6 BC1 DDRA_SDQS6# DDRA_SDQS6# <14>
SA_DQS#_7 AP2 DDRA_SDQS7# DDRA_SDQS7# <14>
SA_MA_0 B119 DDRA_SMA0
SA_MA_1 BD20 DDRA_SMA1
SA_MA_2 BK27 DDRA_SMA2
SA_MA_3 BH28 DDRA_SMA3
SA_MA_4 BL24 DDRA_SMA4
SA_MA_5 BK28 DDRA_SMA5
SA_MA_6 BJ27 DDRA_SMA6
SA_MA_7 BJ25 DDRA_SMA7
SA_MA_8 BL28 DDRA_SMA8
SA_MA_9 BA28 DDRA_SMA9
SA_MA_10 BC19 DDRA_SMA10
SA_MA_11 BE28 DDRA_SMA11
SA_MA_12 BG30 DDRA_SMA12
SA_MA_13 BJ16 DDRA_SMA13
SA_RAS# RE18 DDRA_SRAS# <14>
SA_RCVEN# AY20 SA_RCVEN# PAD T18
SA_WE# BA19 DDRA_SWE# <14>

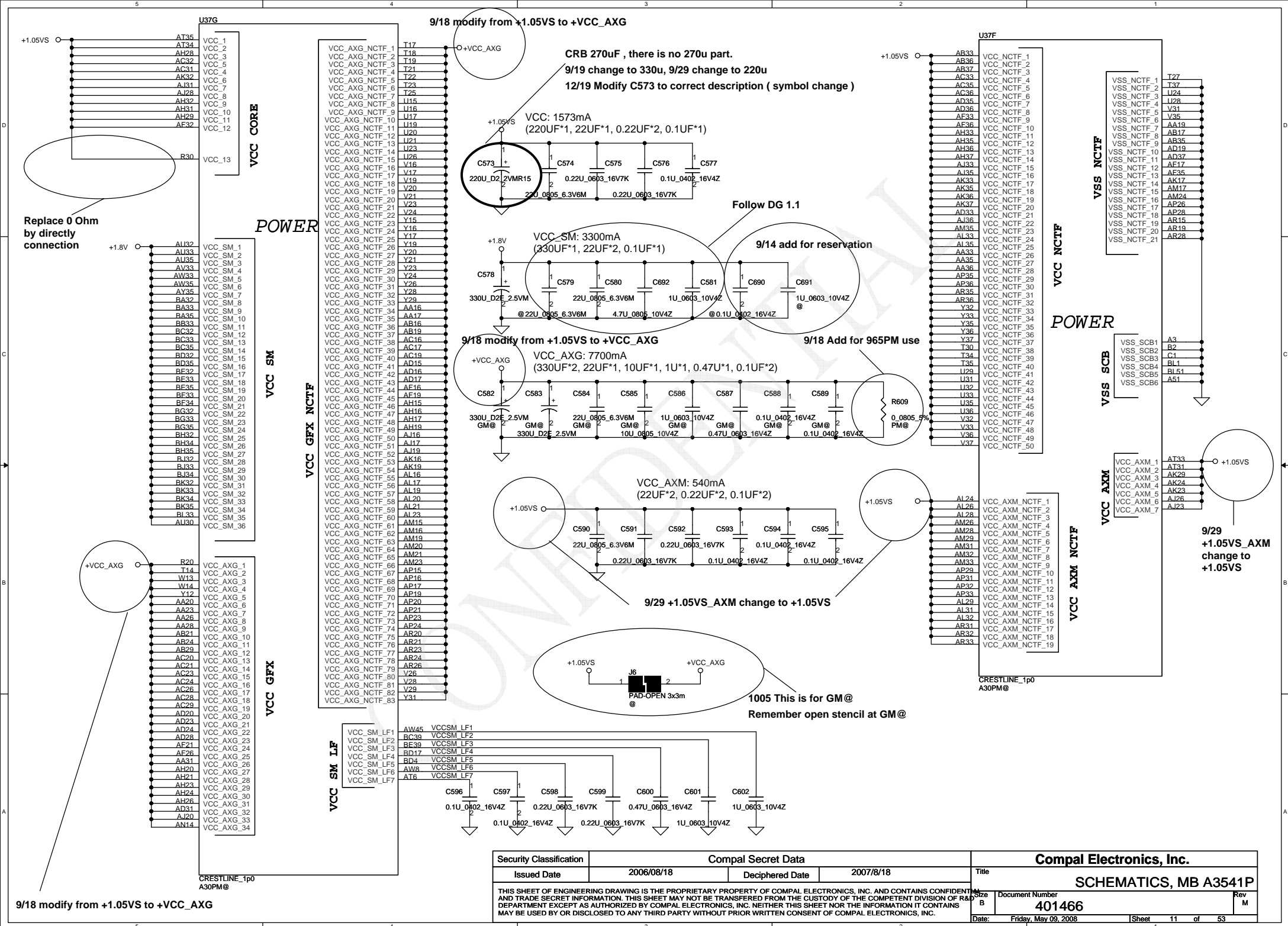
CRESTLINE_1p0
A30PM@

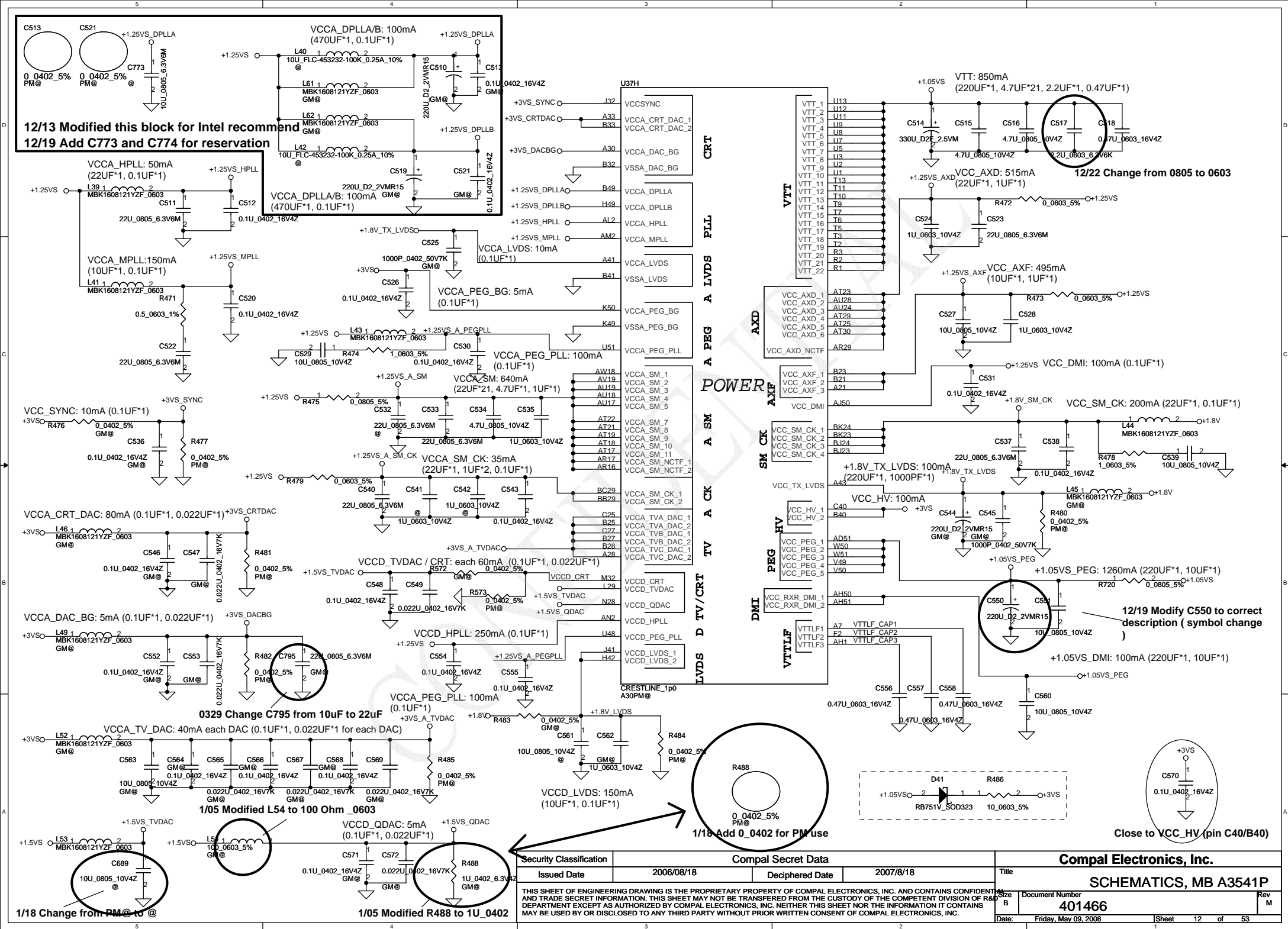
U37E
DDRB_SDQ0 AP49 SB_DQ_0
DDRB_SDQ1 AR51 SB_DQ_1
DDRB_SDQ2 AW50 SB_DQ_2
DDRB_SDQ3 AW51 SB_DQ_3
DDRB_SDQ4 AN50 SB_DQ_4
DDRB_SDQ5 AN51 SB_DQ_5
DDRB_SDQ6 AV50 SB_DQ_6
DDRB_SDQ7 AV49 SB_DQ_7
DDRB_SDQ8 BA50 SB_DQ_8
DDRB_SDQ9 BB50 SB_DQ_9
DDRB_SDQ10 BA49 SB_DQ_10
DDRB_SDQ11 BE50 SB_DQ_11
DDRB_SDQ12 BA51 SB_DQ_12
DDRB_SDQ13 AY49 SB_DQ_13
DDRB_SDQ14 BE50 SB_DQ_14
DDRB_SDQ15 BF49 SB_DQ_15
DDRB_SDQ16 BJ50 SB_DQ_16
DDRB_SDQ17 BJ44 SB_DQ_17
DDRB_SDQ18 BJ43 SB_DQ_18
DDRB_SDQ19 BJ43 SB_DQ_19
DDRB_SDQ20 BK47 SB_DQ_20
DDRB_SDQ21 BK49 SB_DQ_21
DDRB_SDQ22 BK43 SB_DQ_22
DDRB_SDQ23 BK42 SB_DQ_23
DDRB_SDQ24 BJ41 SB_DQ_24
DDRB_SDQ25 BJ41 SB_DQ_25
DDRB_SDQ26 BJ37 SB_DQ_26
DDRB_SDQ27 BJ36 SB_DQ_27
DDRB_SDQ28 BK41 SB_DQ_28
DDRB_SDQ29 BJ40 SB_DQ_29
DDRB_SDQ30 BJ35 SB_DQ_30
DDRB_SDQ31 BK37 SB_DQ_31
DDRB_SDQ32 BK13 SB_DQ_32
DDRB_SDQ33 BE11 SB_DQ_33
DDRB_SDQ34 BK11 SB_DQ_34
DDRB_SDQ35 BC11 SB_DQ_35
DDRB_SDQ36 BC13 SB_DQ_36
DDRB_SDQ37 BE12 SB_DQ_37
DDRB_SDQ38 BC12 SB_DQ_38
DDRB_SDQ39 BG12 SB_DQ_39
DDRB_SDQ40 BJ10 SB_DQ_40
DDRB_SDQ41 BJ9 SB_DQ_41
DDRB_SDQ42 BK5 SB_DQ_42
DDRB_SDQ43 BL5 SB_DQ_43
DDRB_SDQ44 BK9 SB_DQ_44
DDRB_SDQ45 BK10 SB_DQ_45
DDRB_SDQ46 BJ8 SB_DQ_46
DDRB_SDQ47 BJ6 SB_DQ_47
DDRB_SDQ48 BF4 SB_DQ_48
DDRB_SDQ49 BH5 SB_DQ_49
DDRB_SDQ50 BC1 SB_DQ_50
DDRB_SDQ51 BC2 SB_DQ_51
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DDRB_SDQ53 BE4 SB_DQ_53
DDRB_SDQ54 BD3 SB_DQ_54
DDRB_SDQ55 BJ2 SB_DQ_55
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DDRB_SDQ57 BR3 SB_DQ_57
DDRB_SDQ58 AR1 SB_DQ_58
DDRB_SDQ59 AT3 SB_DQ_59
DDRB_SDQ60 AY2 SB_DQ_60
DDRB_SDQ61 AY3 SB_DQ_61
DDRB_SDQ62 AU2 SB_DQ_62
DDRB_SDQ63 AT2 SB_DQ_63
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SB_BS_1 BG18 DDRB_SBS1 <15>
SB_BS_2 BG36 DDRB_SBS2 <15>
SB_CAS# BE17 DDRB_SCAS# <15>
SB_DM_0 AR50 DDRB_SDM0
SB_DM_1 BD49 DDRB_SDM1
SB_DM_2 BK45 DDRB_SDM2
SB_DM_3 BL38 DDRB_SDM3
SB_DM_4 BH12 DDRB_SDM4
SB_DM_5 BJ7 DDRB_SDM5
SB_DM_6 BE3 DDRB_SDM6
SB_DM_7 AW2 DDRB_SDM7
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SB_DQS_2 BK46 DDRB_SDQS2 DDRA_SDQS2 <15>
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SB_DQS_4 BJ12 DDRB_SDQS4 DDRA_SDQS4 <15>
SB_DQS_5 BL7 DDRB_SDQS5 DDRA_SDQS5 <15>
SB_DQS_6 BE2 DDRB_SDQS6 DDRA_SDQS6 <15>
SB_DQS_7 AV2 DDRB_SDQS7 DDRA_SDQS7 <15>
SB_DQS#_0 AU50 DDRB_SDQS0# DDRA_SDQS0# <15>
SB_DQS#_1 BC50 DDRB_SDQS1# DDRA_SDQS1# <15>
SB_DQS#_2 BL45 DDRB_SDQS2# DDRA_SDQS2# <15>
SB_DQS#_3 BK38 DDRB_SDQS3# DDRA_SDQS3# <15>
SB_DQS#_4 BK12 DDRB_SDQS4# DDRA_SDQS4# <15>
SB_DQS#_5 BK7 DDRB_SDQS5# DDRA_SDQS5# <15>
SB_DQS#_6 BE2 DDRB_SDQS6# DDRA_SDQS6# <15>
SB_DQS#_7 AV3 DDRB_SDQS7# DDRA_SDQS7# <15>
SB_MA_0 BC18 DDRB_SMA0
SB_MA_1 BG28 DDRB_SMA1
SB_MA_2 BG25 DDRB_SMA2
SB_MA_3 AW17 DDRB_SMA3
SB_MA_4 BE25 DDRB_SMA4
SB_MA_5 BA28 DDRB_SMA5
SB_MA_6 BC28 DDRB_SMA6
SB_MA_7 AY28 DDRB_SMA7
SB_MA_8 BD37 DDRB_SMA8
SB_MA_9 BC17 DDRB_SMA9
SB_MA_10 BE37 DDRB_SMA10
SB_MA_11 BA38 DDRB_SMA11
SB_MA_12 BG13 DDRB_SMA12
SB_MA_13
SB_RAS# AV16 DDRB_SRAS# <15>
SB_RCVEN# AY18 SB_RCVEN# PAD T17
SB_WE# BC17 DDRB_SWE# <15>

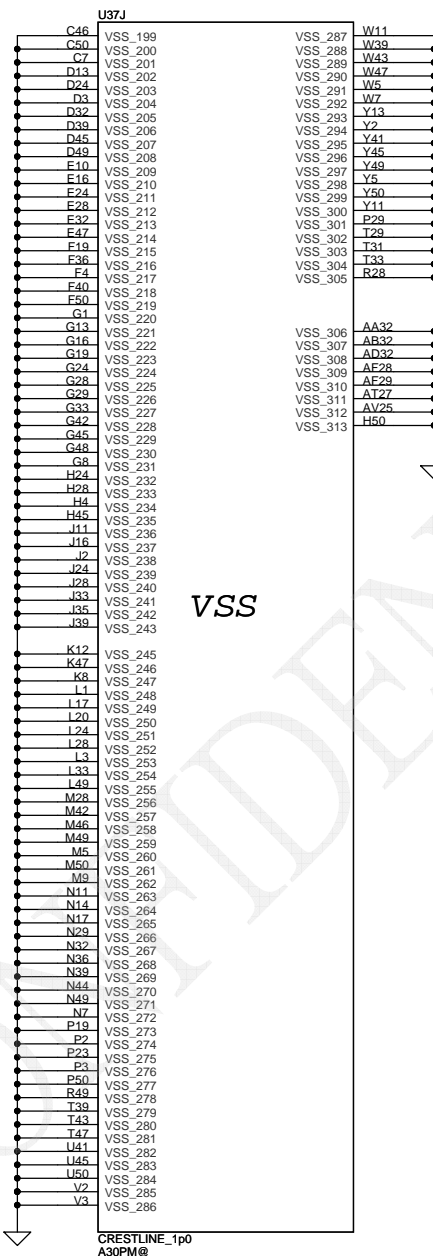
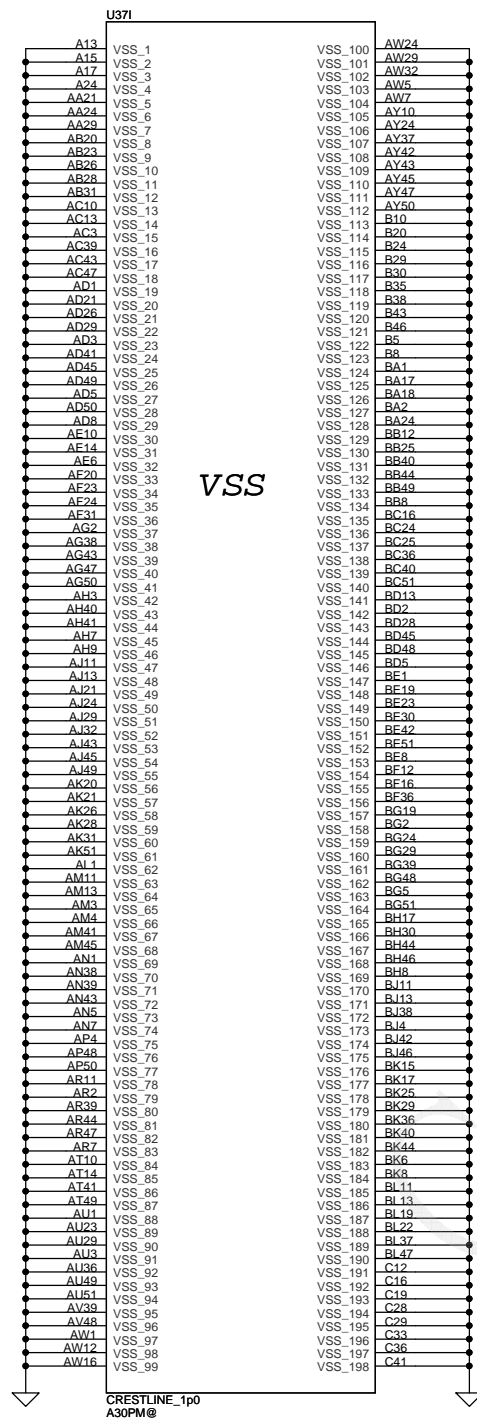
DDR SYSTEM MEMORY B

CRESTLINE_1p0
A30PM@

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Size	B	Document Number	401466	Rev	M
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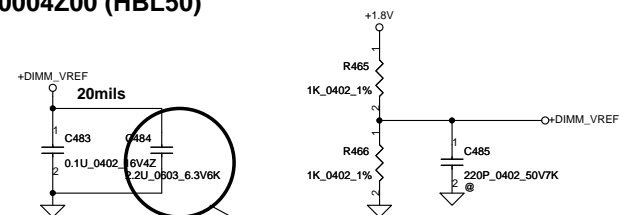
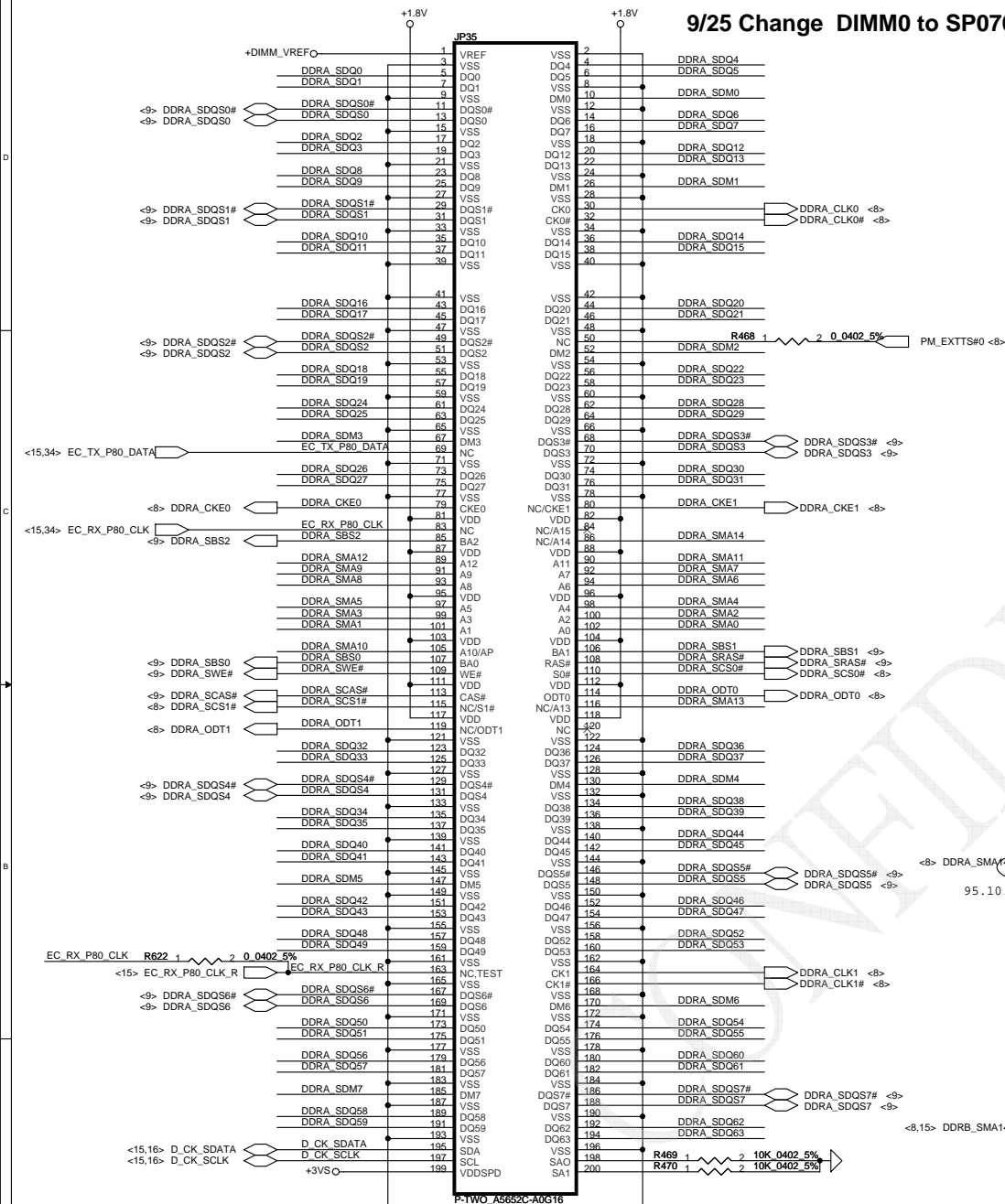






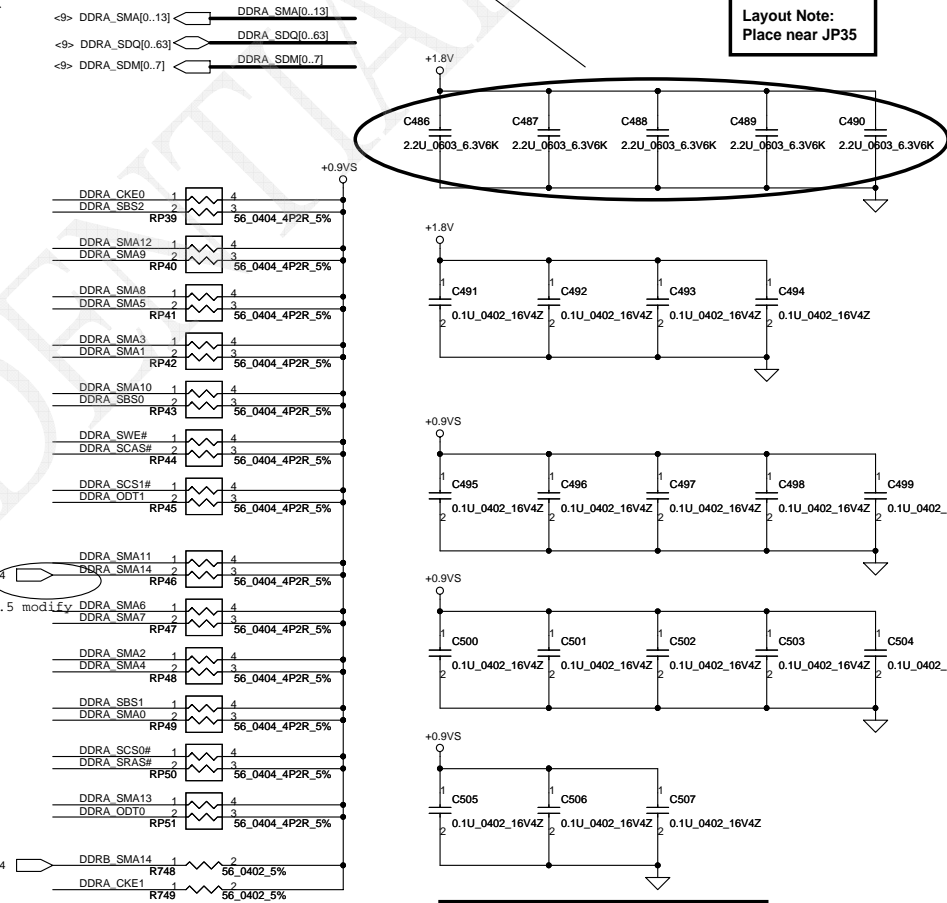
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	SCHEMATICS, MB A3541P
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9/25 Change DIMM0 to SP070004Z00 (HBL50)



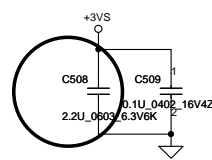
12/22 Change from 0805 to 0603

Layout Note:
Place near JP35



Layout Note:
Place these resistor
closely JP35,all
trace length Max=1.5

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



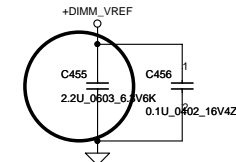
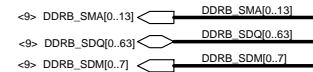
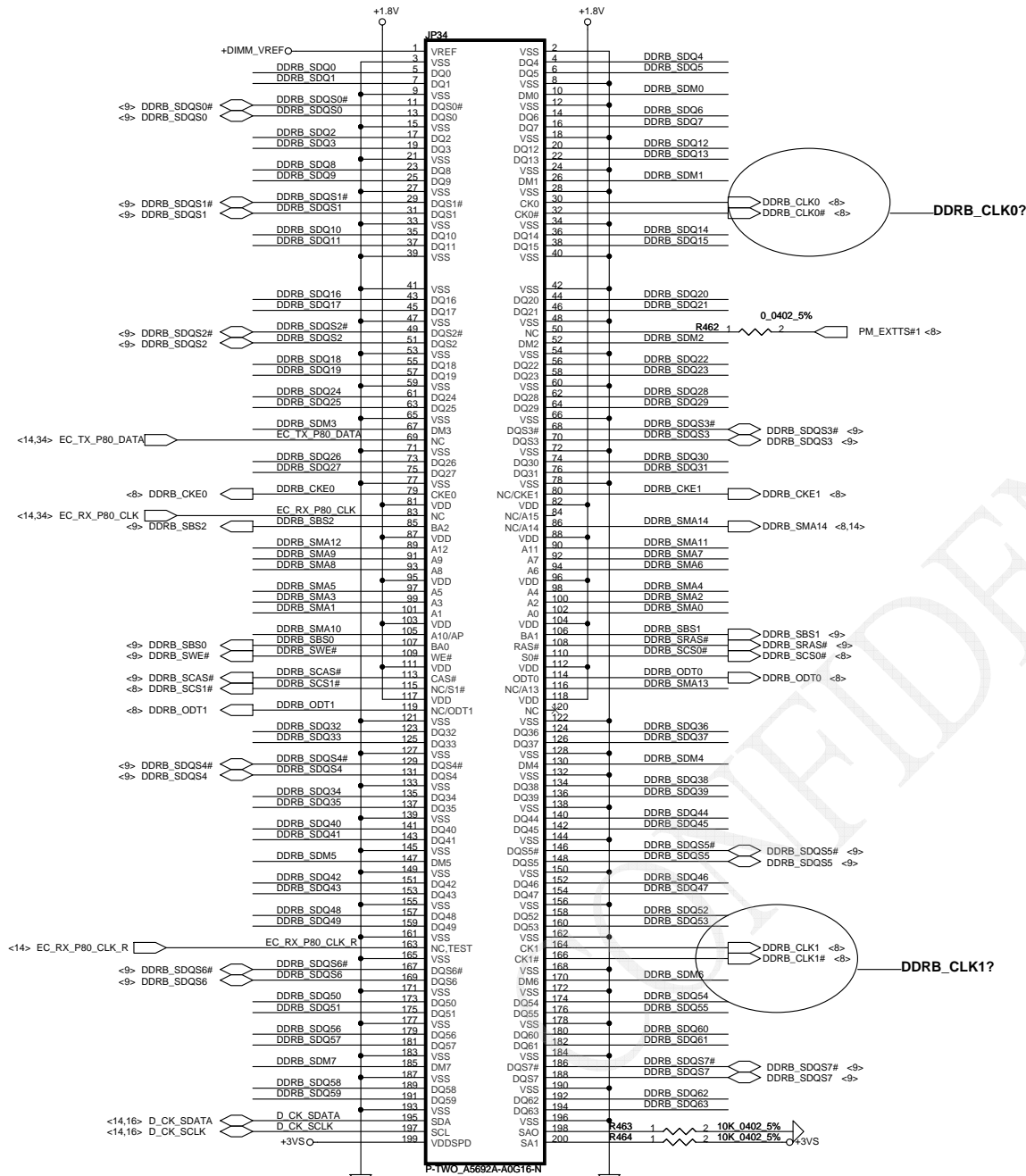
Change PCB Footprint

DIMM0 STD H:5.2mm (BOT)

12/22 Change from 0805 to 0603

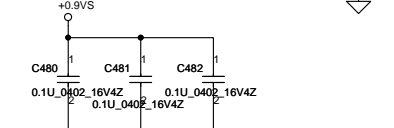
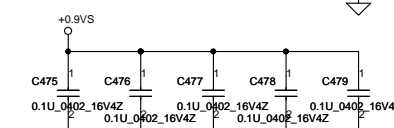
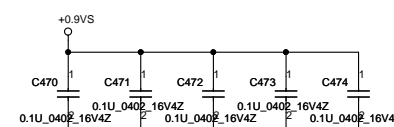
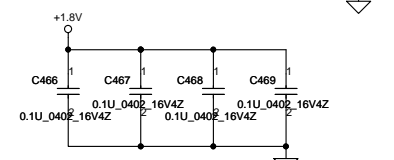
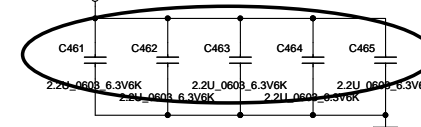
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Issued Date	2006/08/18	Deciphered Date	2007/8/18			SCHEMATICS, MB A3541P	
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				401466		M	
				Date:	Friday, May 09, 2008	Sheet	14 of 53

9/25 Change DIMM1 to SP070006F00



12/22 Change from 0805 to 0603

Layout Note:
Place near JP34



Layout Note:
Place these resistor
closely JP35,all
trace length Max=1.5"

Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS

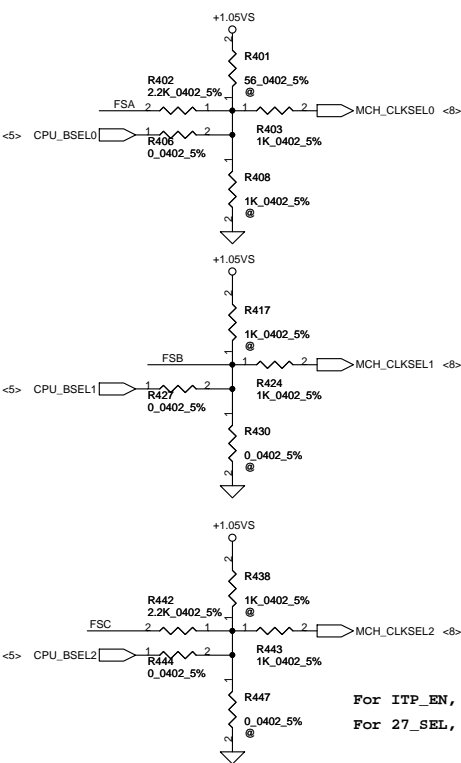
DIMM1 STD H:9.2mm (BOT)

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FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	1	0	200	100	33.3
0	1	1	166	100	33.3

FSB Frequency Selet:

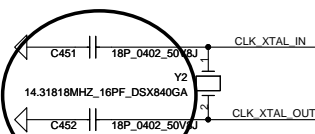
CPU Driven	Stuff							
*(Default)	No Stuff	R401	R408	R417	R430	R438	R447	
667MHz	Stuff	R401	R417	R447				
	No Stuff	R408	R430	R438				
800MHz	Stuff	R408	R417	R447				
	No Stuff	R401	R430	R438				



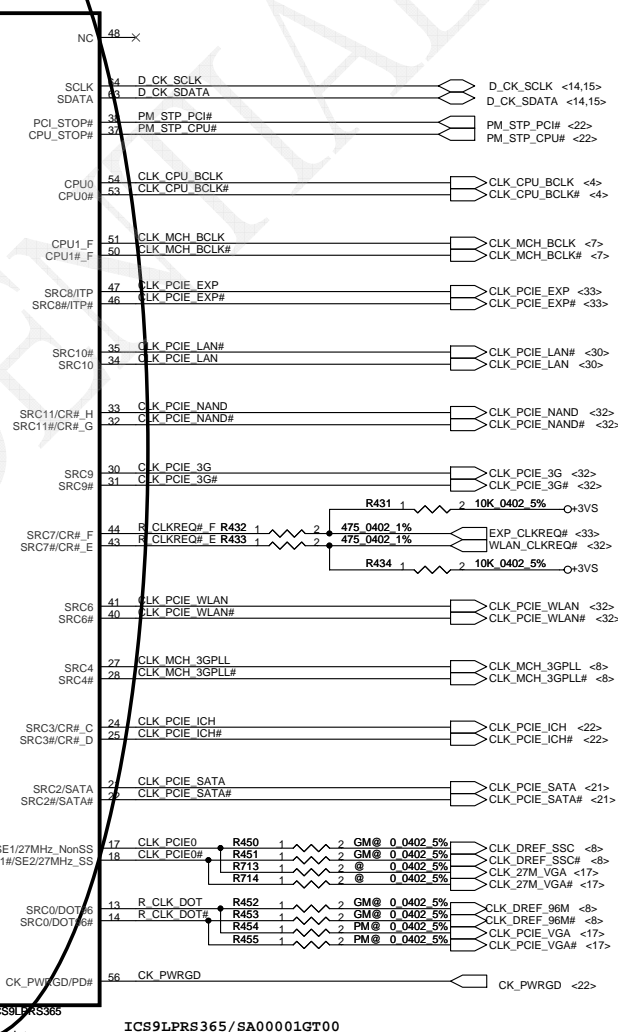
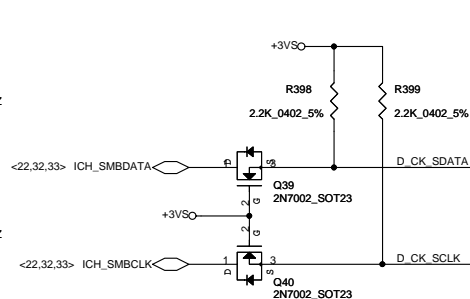
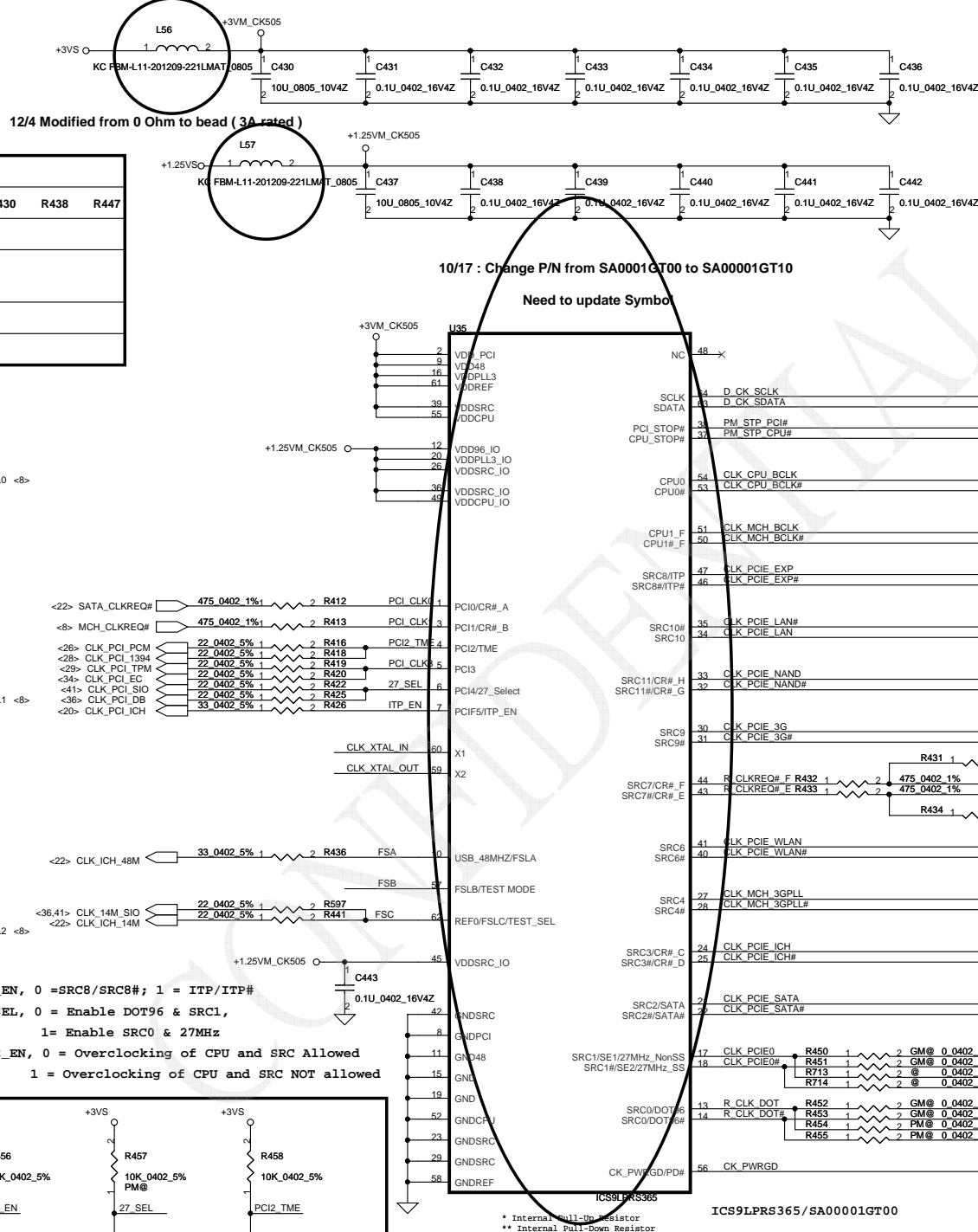
For ITP_EN, 0 = SRC8/SRC9#; 1 = ITP/ITP#

For 27_SEL, 0 = Enable DOT96 & SRC1,
1 = Enable SRC0 & 27MHz

For PCI2_EN, 0 = Overclocking of CPU and SRC Allowed
1 = Overclocking of CPU and SRC NOT allowed



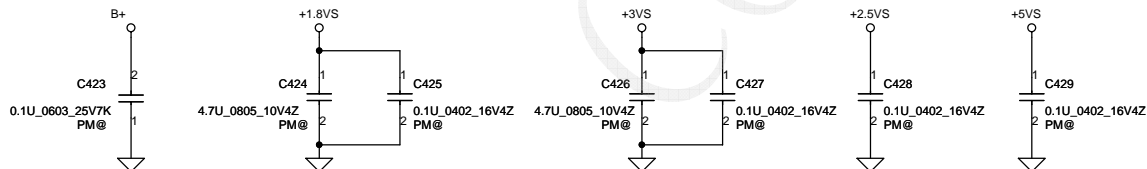
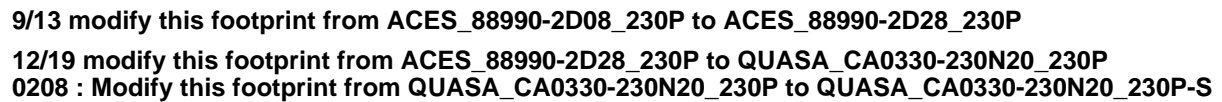
Routing the trace at least 10mil



C444	2	1 CLK_ICH 48M
		@ 5P_0402_50V8C
C445	2	1 CLK_ICH 14M
		@ 4P_0402_50V8C
C446	2	1 CLK_PCI_ICH
		@ 47P_0402_50V8C
C447	2	1 CLK_14M_SIO
		@ 47P_0402_50V8C
C448	2	1 CLK_PCI_PCM
		@ 47P_0402_50V8C
C449	2	1 CLK_PCI_EC
		@ 47P_0402_50V8C
C450	2	1 CLK_PCI_SIO
		@ 47P_0402_50V8C

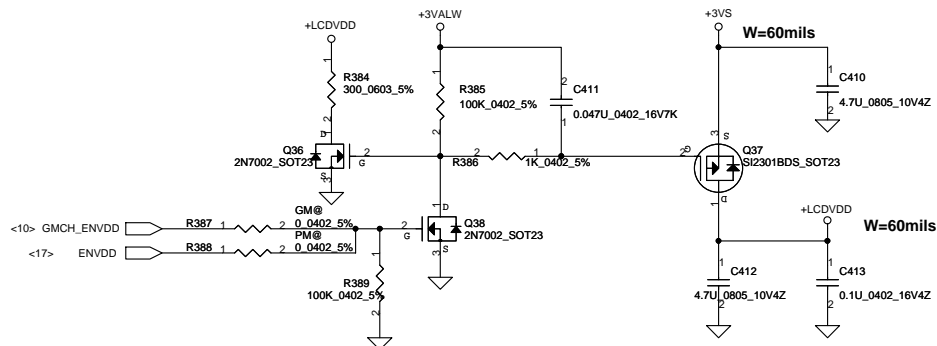
Place close to U35

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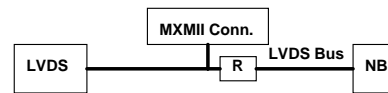


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				Custom	401466	M
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LCD POWER CIRCUIT

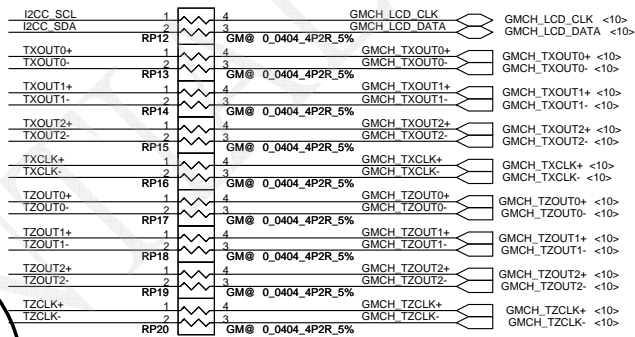
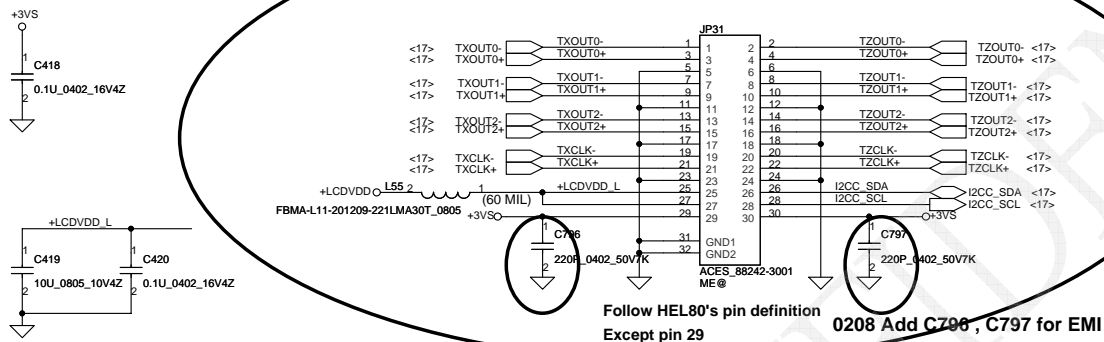


Routing Diagram

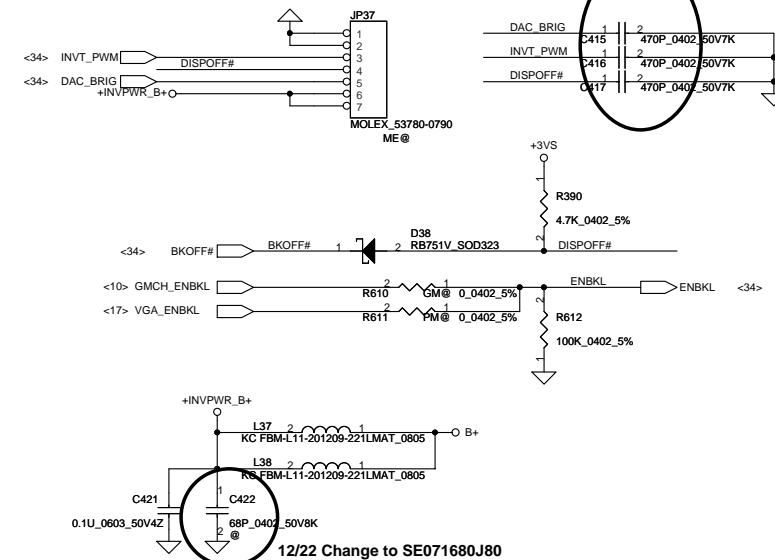


Use Daisy chain to route

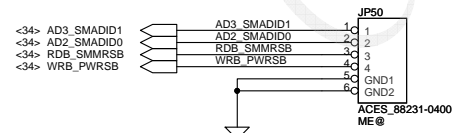
LCD/PANEL BD. Conn.



INVERTER Conn.

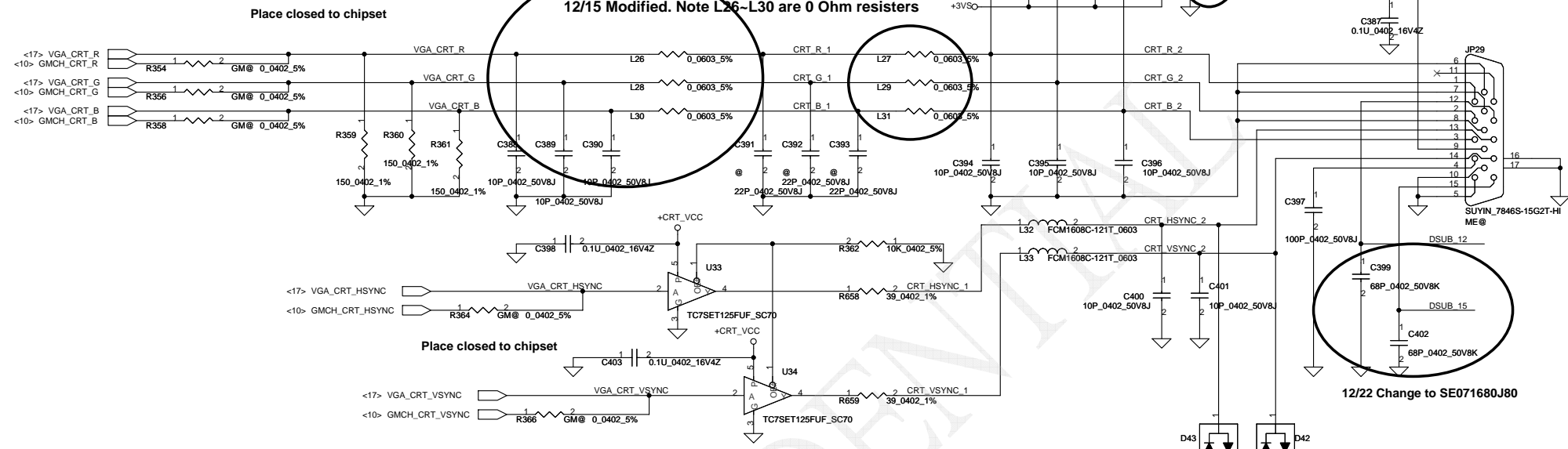


JEPICO Conn.

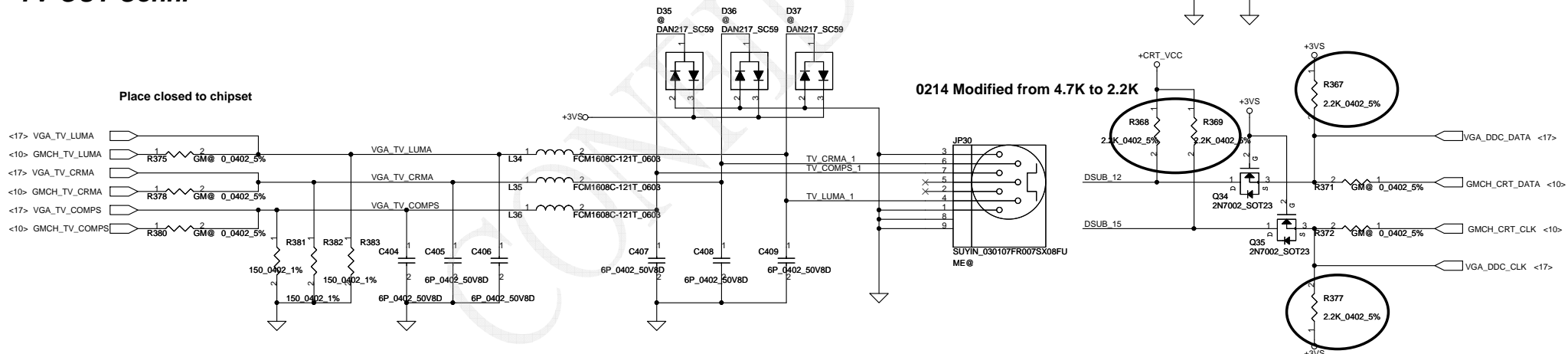


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				Sheet	18 of 53

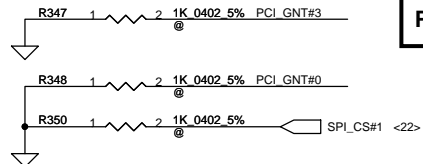
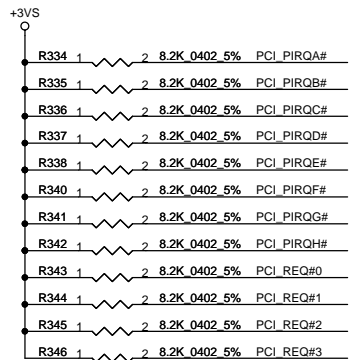
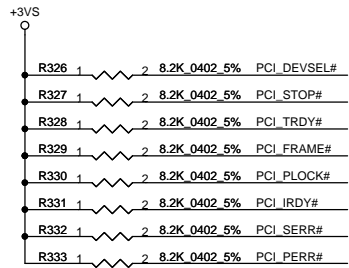
CRT Connector



TV-OUT Conn.



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										M	
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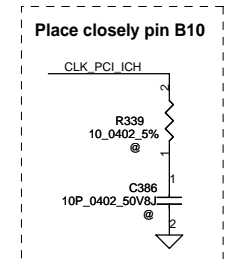
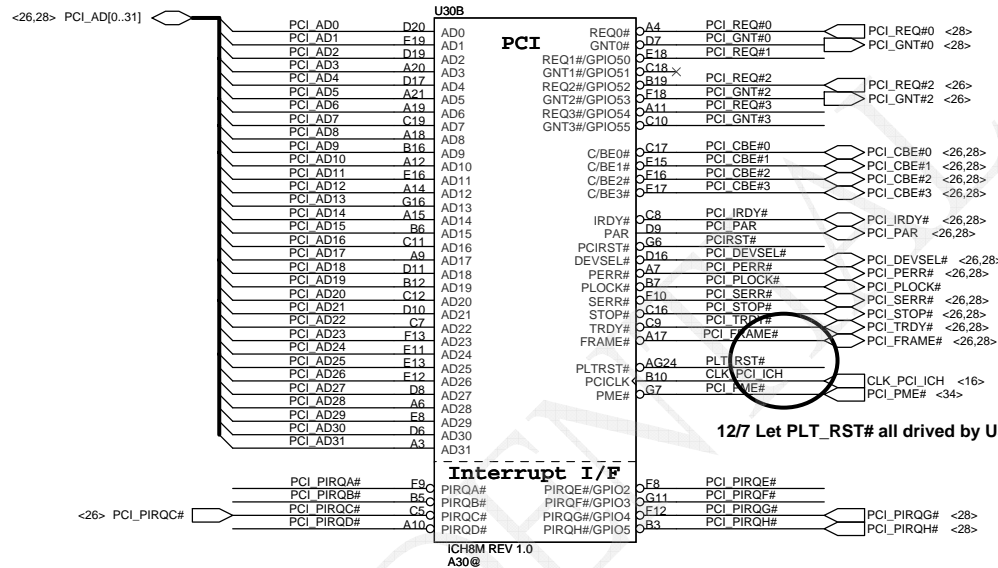
A16 Swap Override Strap		
PCI_GNT#3	Low= A16 swap override Enable High= Default*	

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*

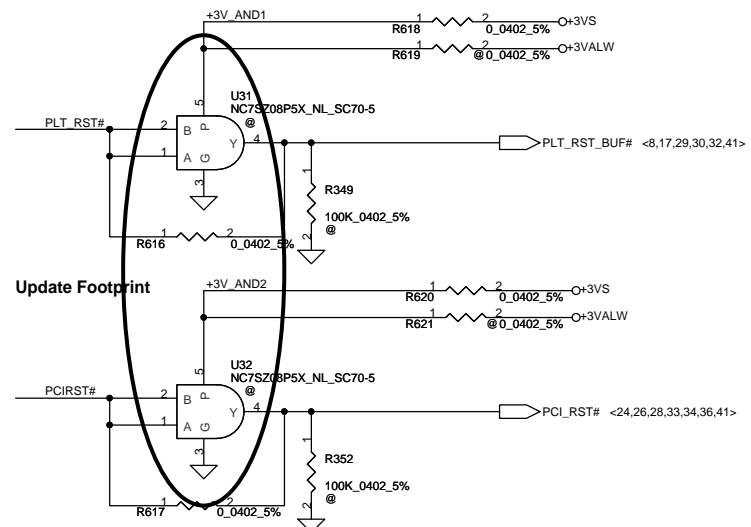
10/17 : Change P/N from SA000010G00 to SA00001JU10
 10/17 : FootPrint : SA000010G00
 BOM : SA00001JU10
 1/2 : Change U30 part number to SA00001JU80
 3/21 : Change U30 part number to SA00001JUA0
 3/28 : Change U30 part number to SA00001JUD0 for 030
 0425 Change U30 from mount to A30@

U30
 ICH8M REV 1.0
 HS@

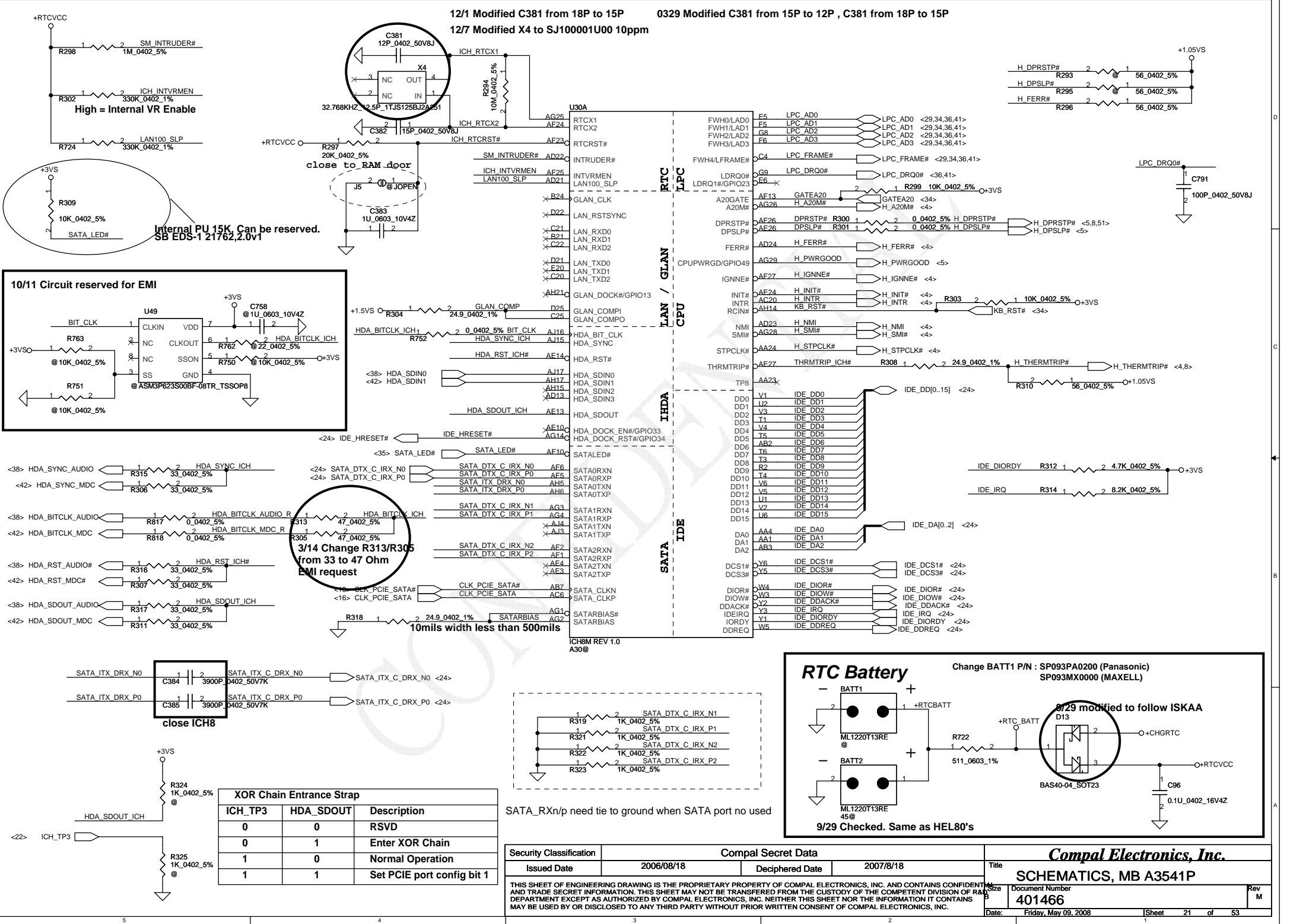
0425 Add U30 part number to SA00001JUA0 for HS@

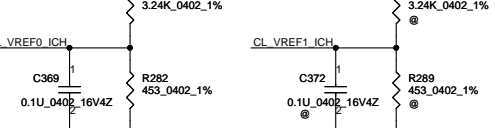
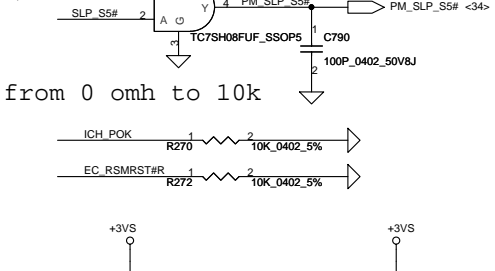
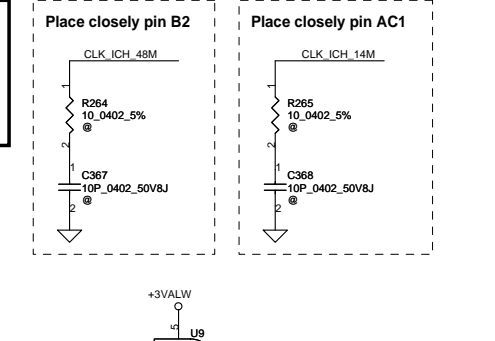


12/7 Let PLT_RST# all driven by U31

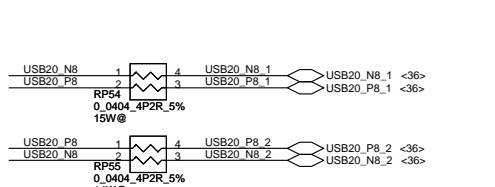


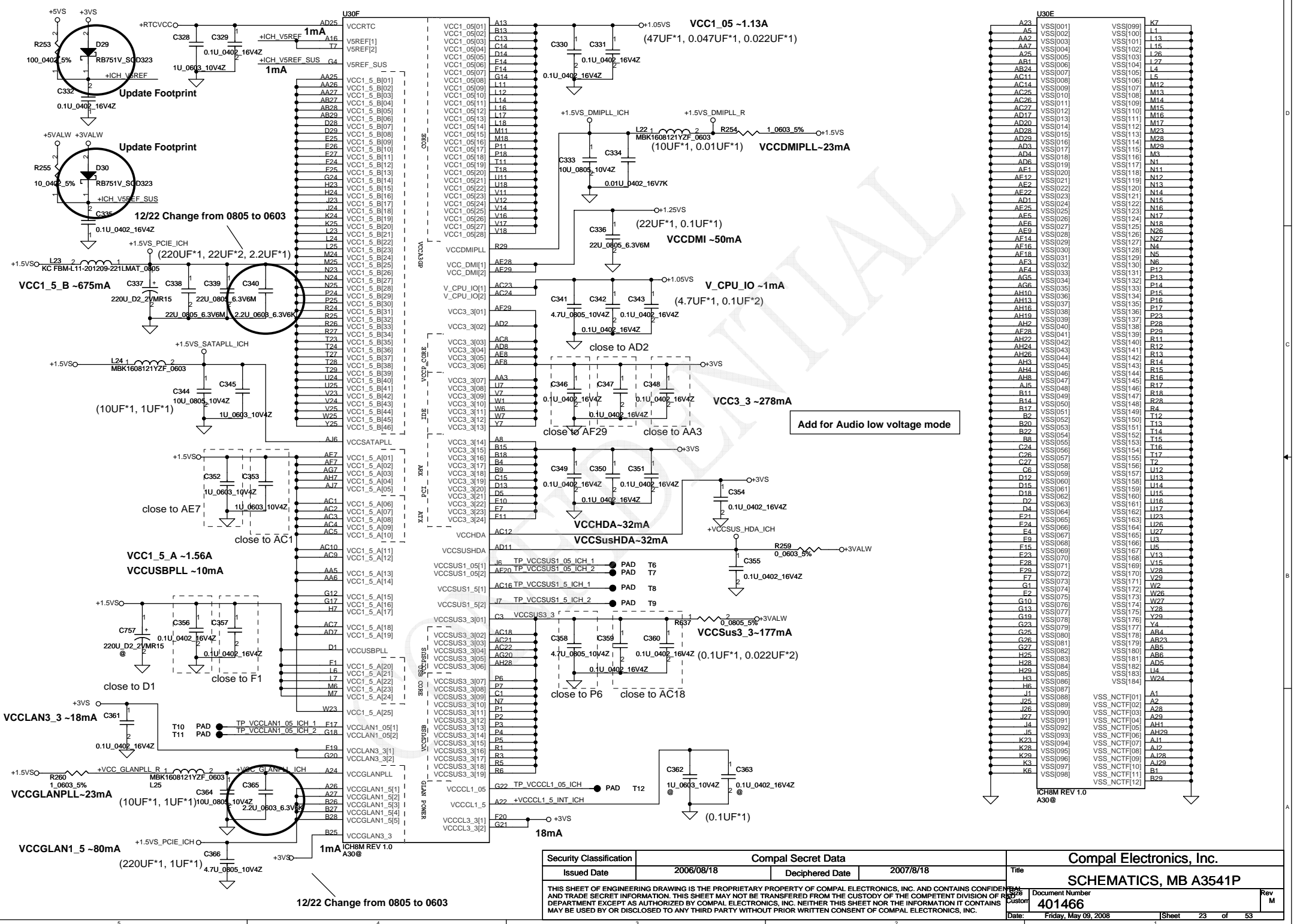
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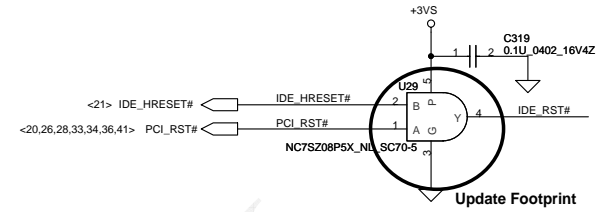
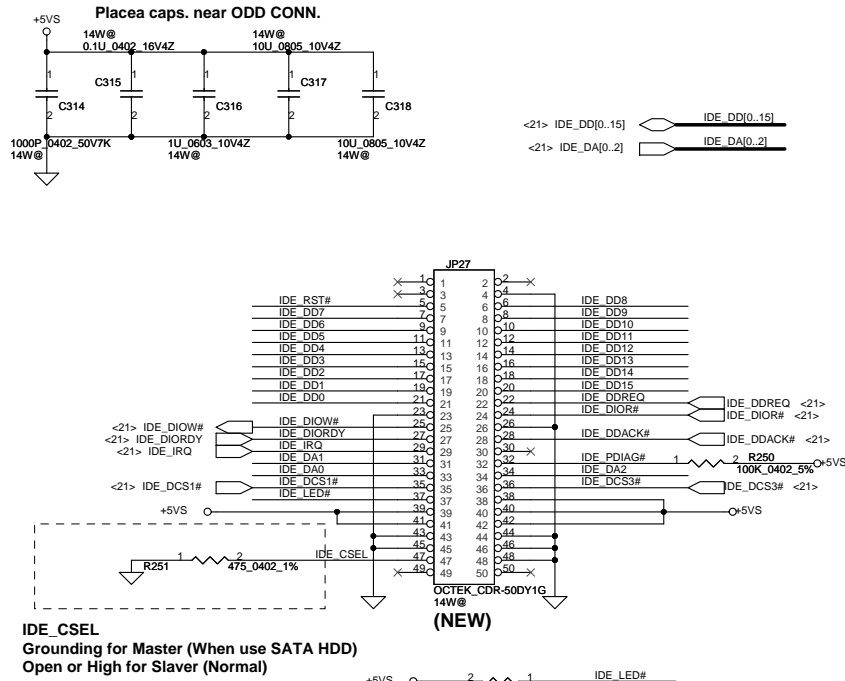
Compal Electronics, Inc.			
Title			
SCHEMATICS, MB A3541P			
NEW R29 Custom	Document Number		Rev
	40146		M
Doc#	U6000	1000	00



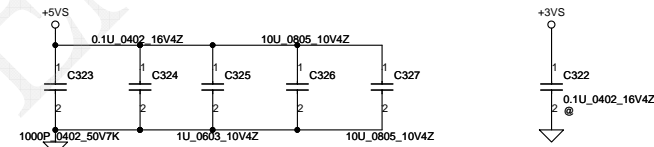


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								Document Number		Rev	
								401466		M	
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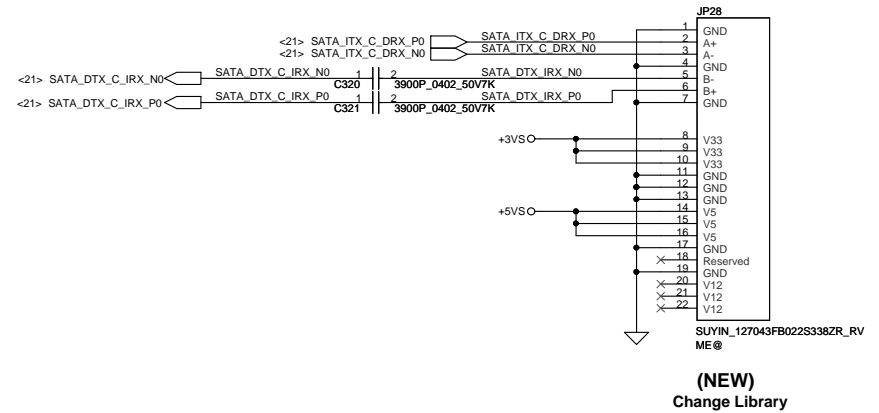
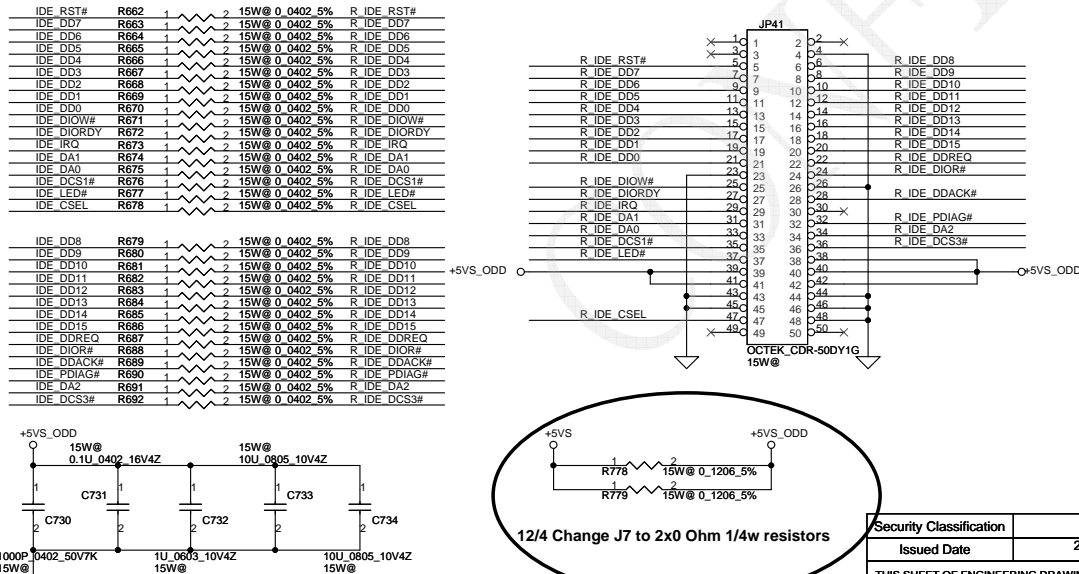
14W ODD Conn.



SATA HDD Conn.



15W ODD Conn.



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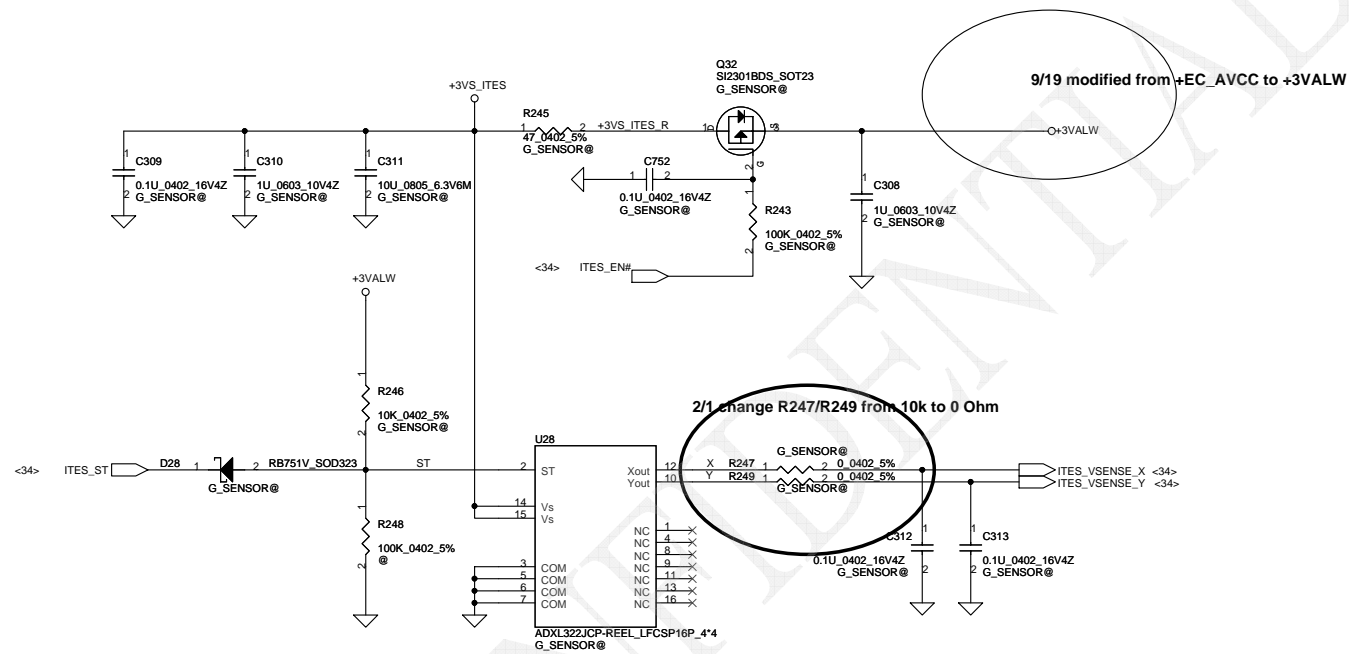
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401466

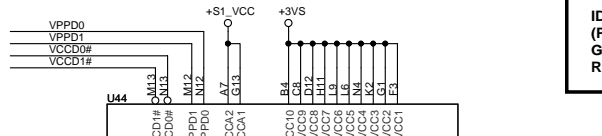
Friday, May 03, 2008

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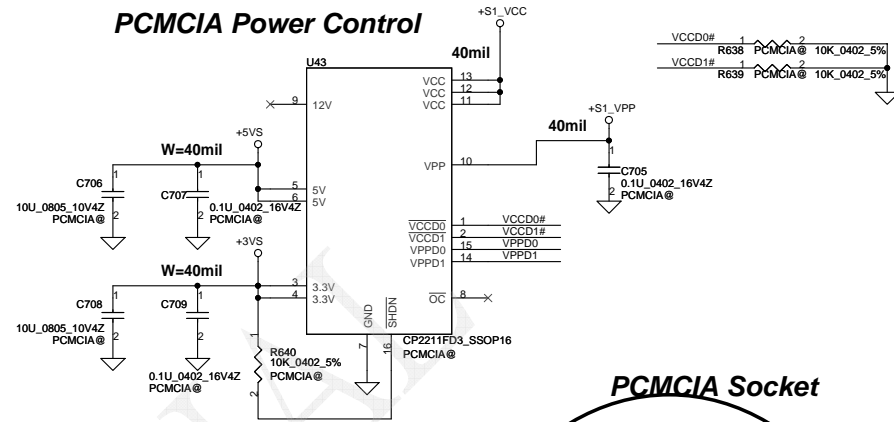
0206 => Note : Change BOM structure from HS@ to G-SENSOR@



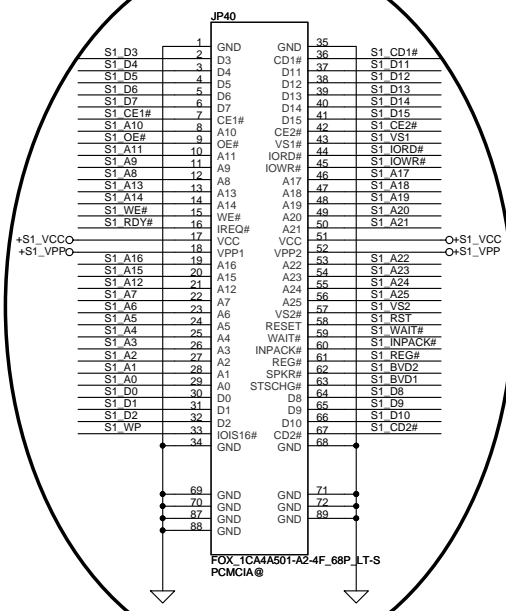
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				Docu	401466	
				Date	Friday, May 09, 2008	Sheet 25 of 53



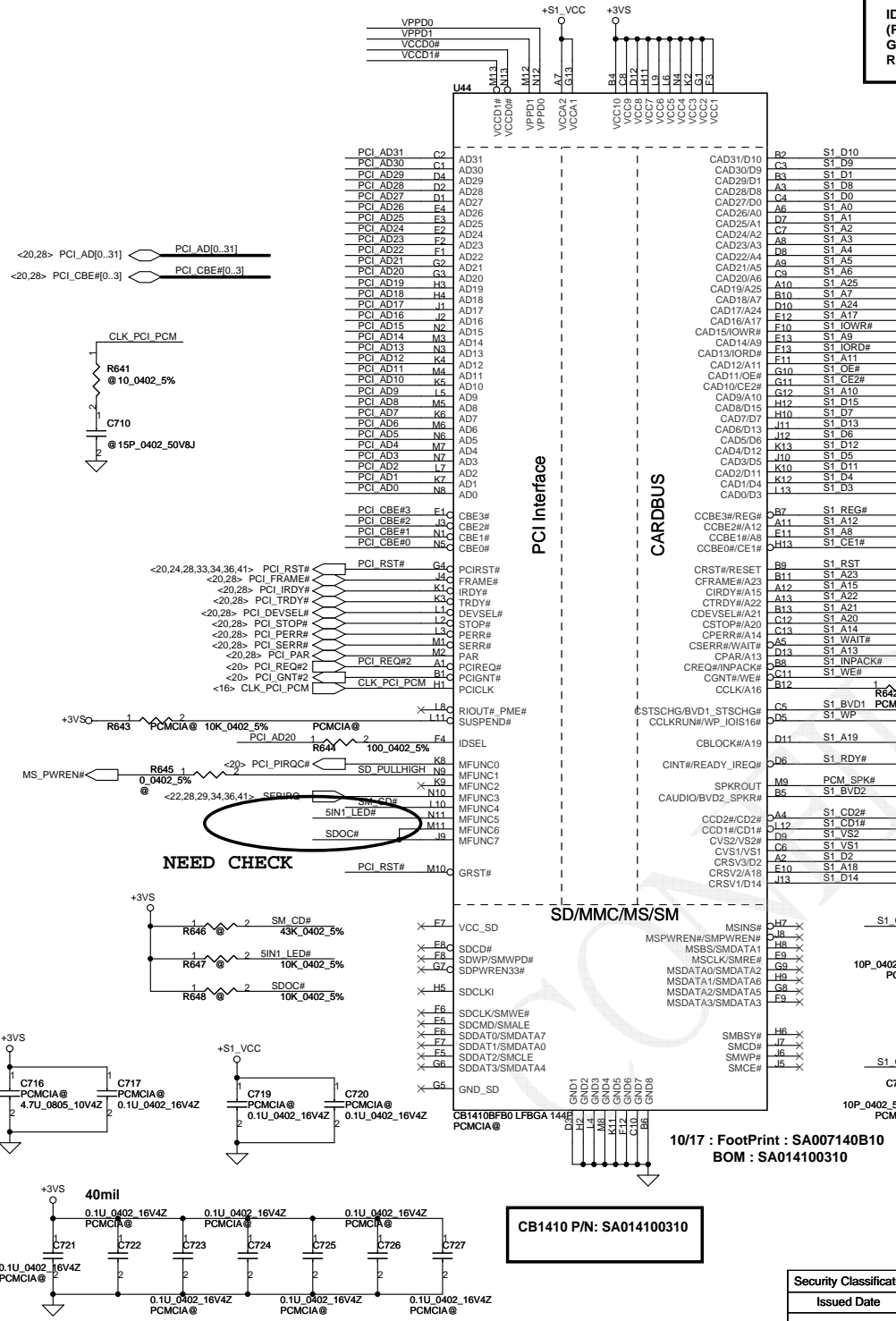
PCMCIA Power Control



PCMCIA Socket



12/27 change JP40 footprint to FOX_1CA4A501-A2-4F_68P_LT-S
04/17 Symbol Add Pin 87,88,89



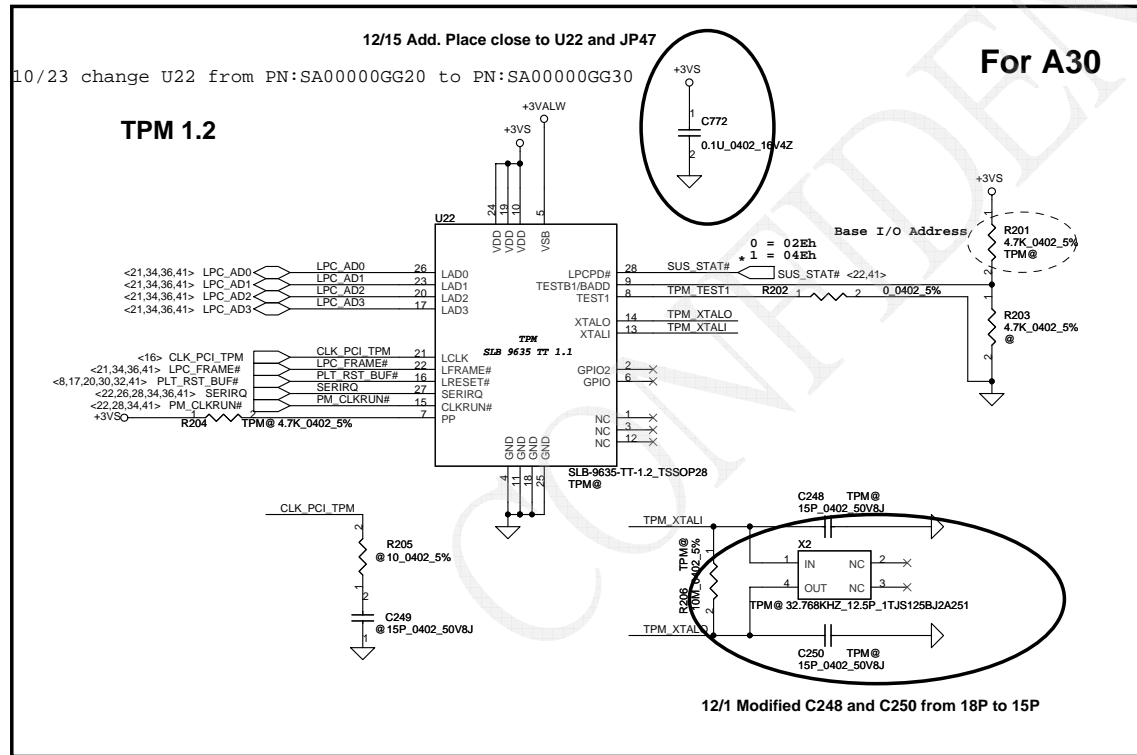
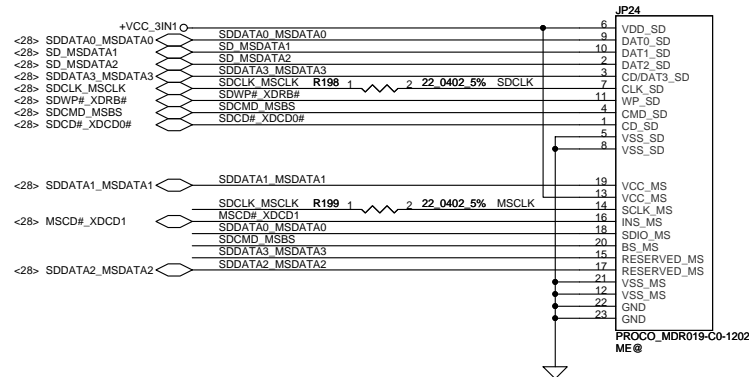
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Issued Date	2006/08/04	Deciphered Date	2006/10/06	Rev	M
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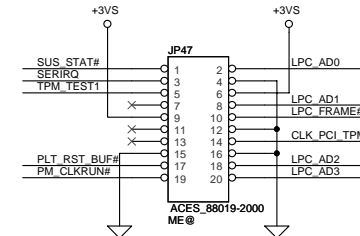
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Title SCHEMATICS, MB A3541P			
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3 in 1 Card Reader



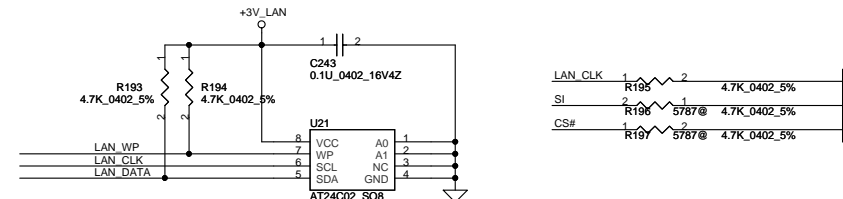
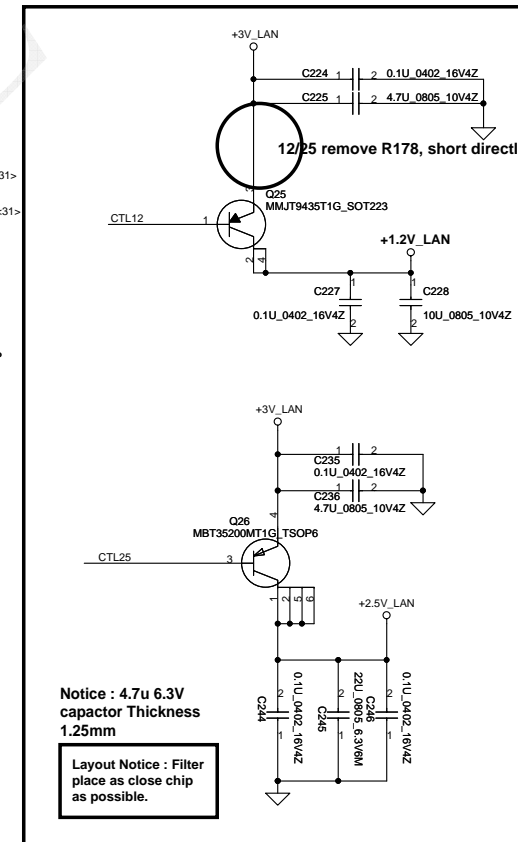
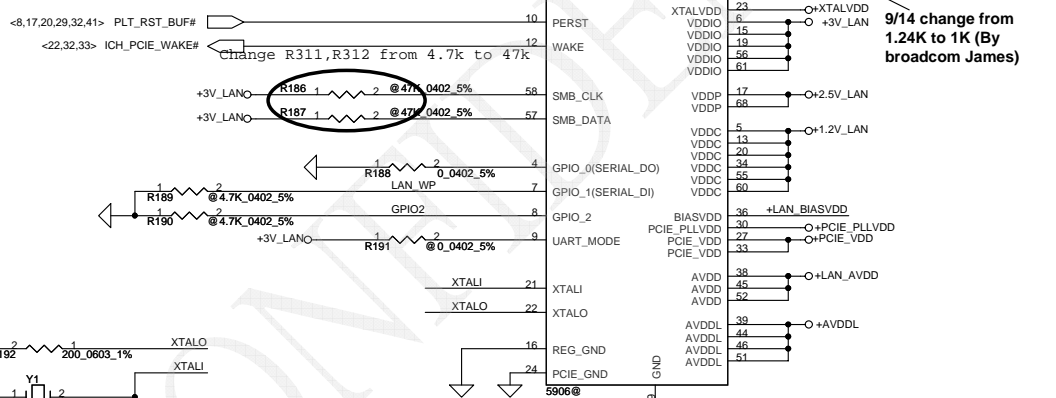
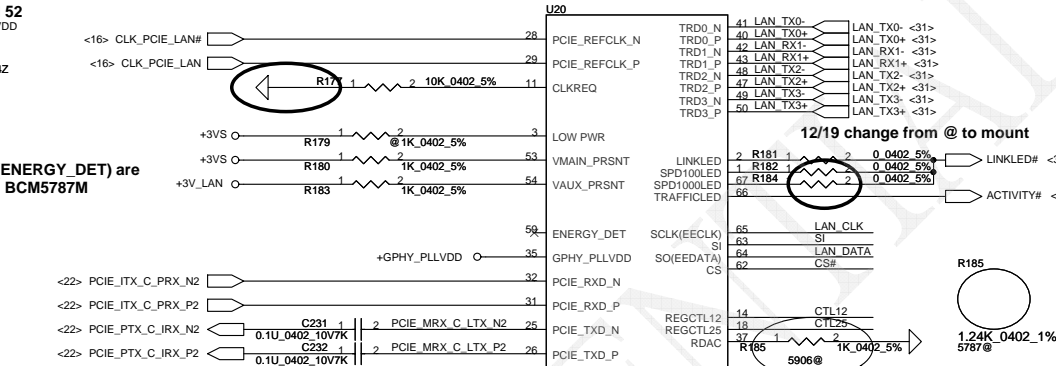
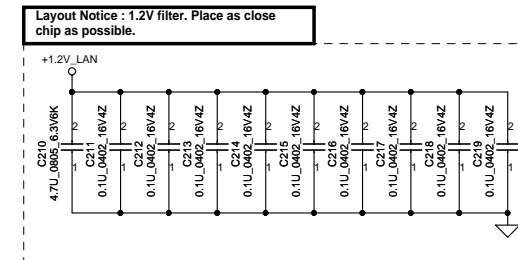
For A30

TPM Conn. For C38



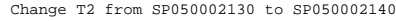
Place this cap close to pin 6 and pin 9
12/15 Modified C739 to @

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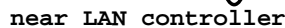


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12/27 Add R815

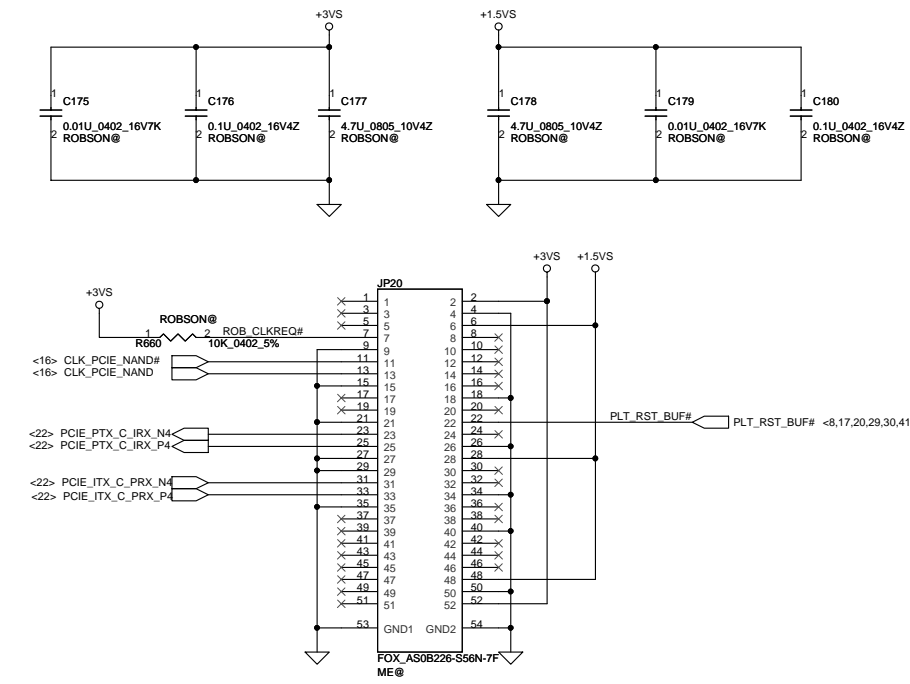


Change C468,C470,C473,C474,C475,C476 from 0.01uF to 0.1uF

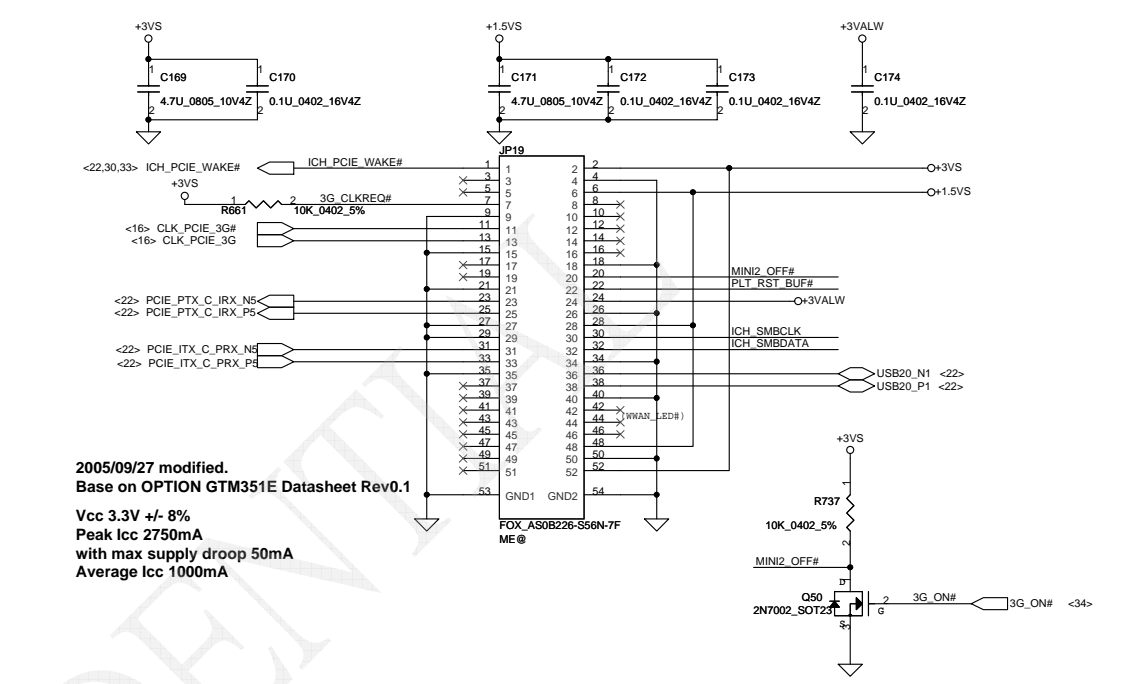


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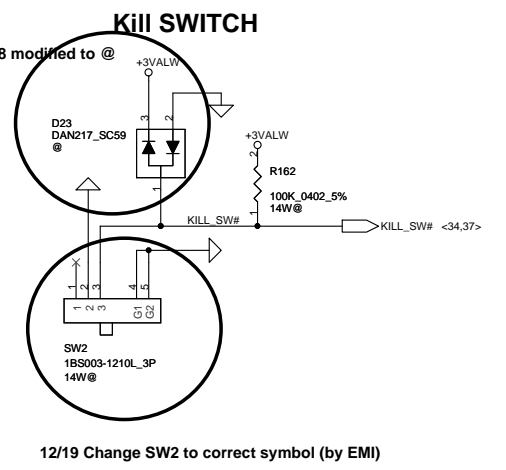
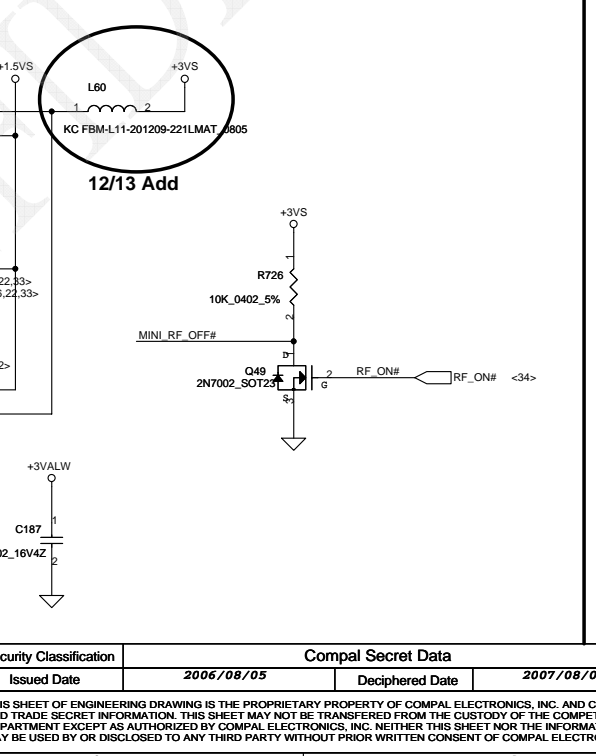
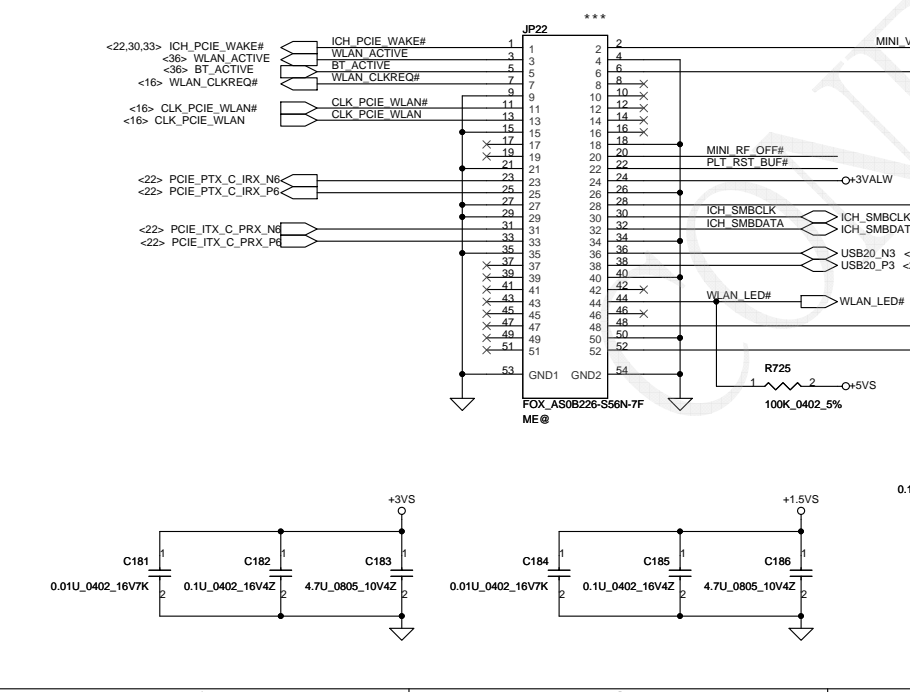
NAND mini Card(Robson support)



Mini-Express Card for 3G Or TV Tuner

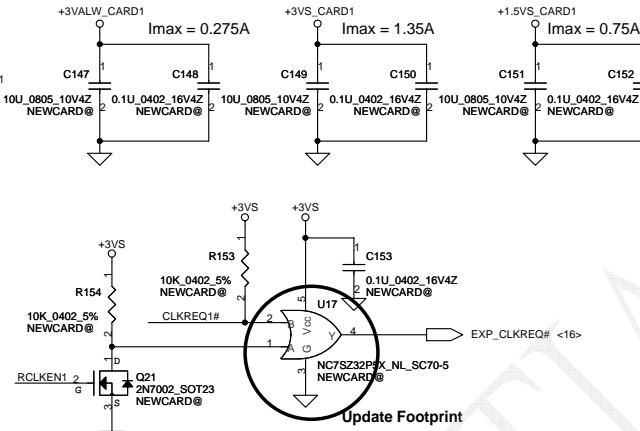
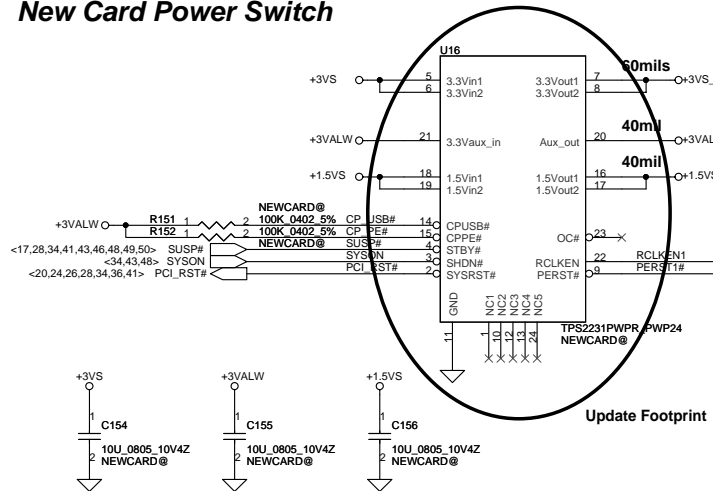


Mini-Express Card for WLAN

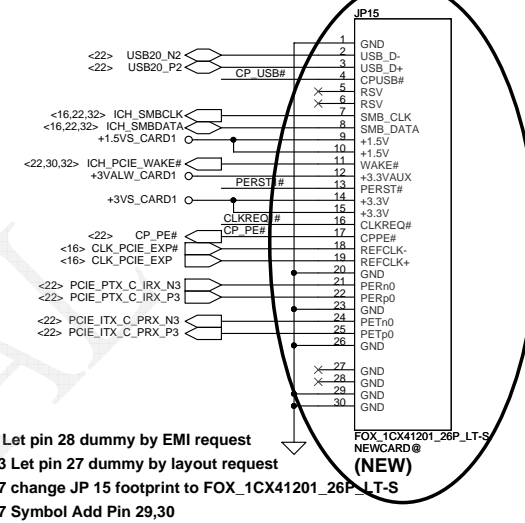


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New Card Power Switch

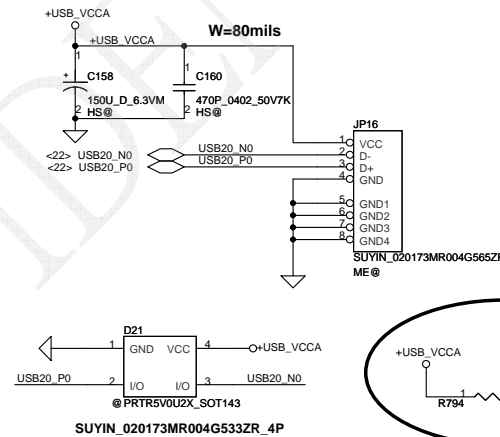


New Card Socket (Left/TOP)

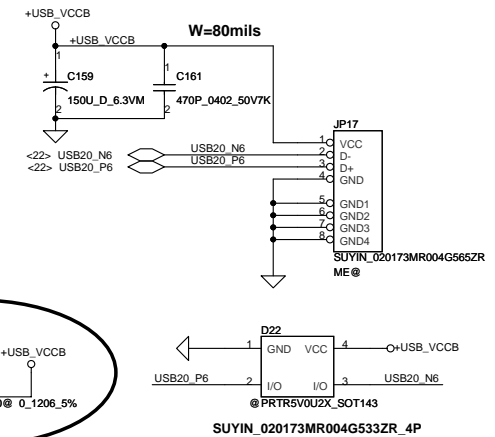


12/7 Let pin 28 dummy by EMI request
 12/13 Let pin 27 dummy by layout request
 12/27 change JP 15 footprint to FOX_1CX41201_26P_LT-S
 04/17 Symbol Add Pin 29,30

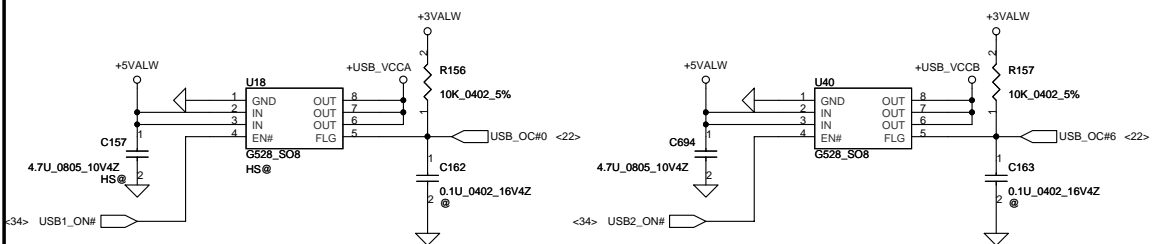
USB CONN. 1



USB CONN. 2

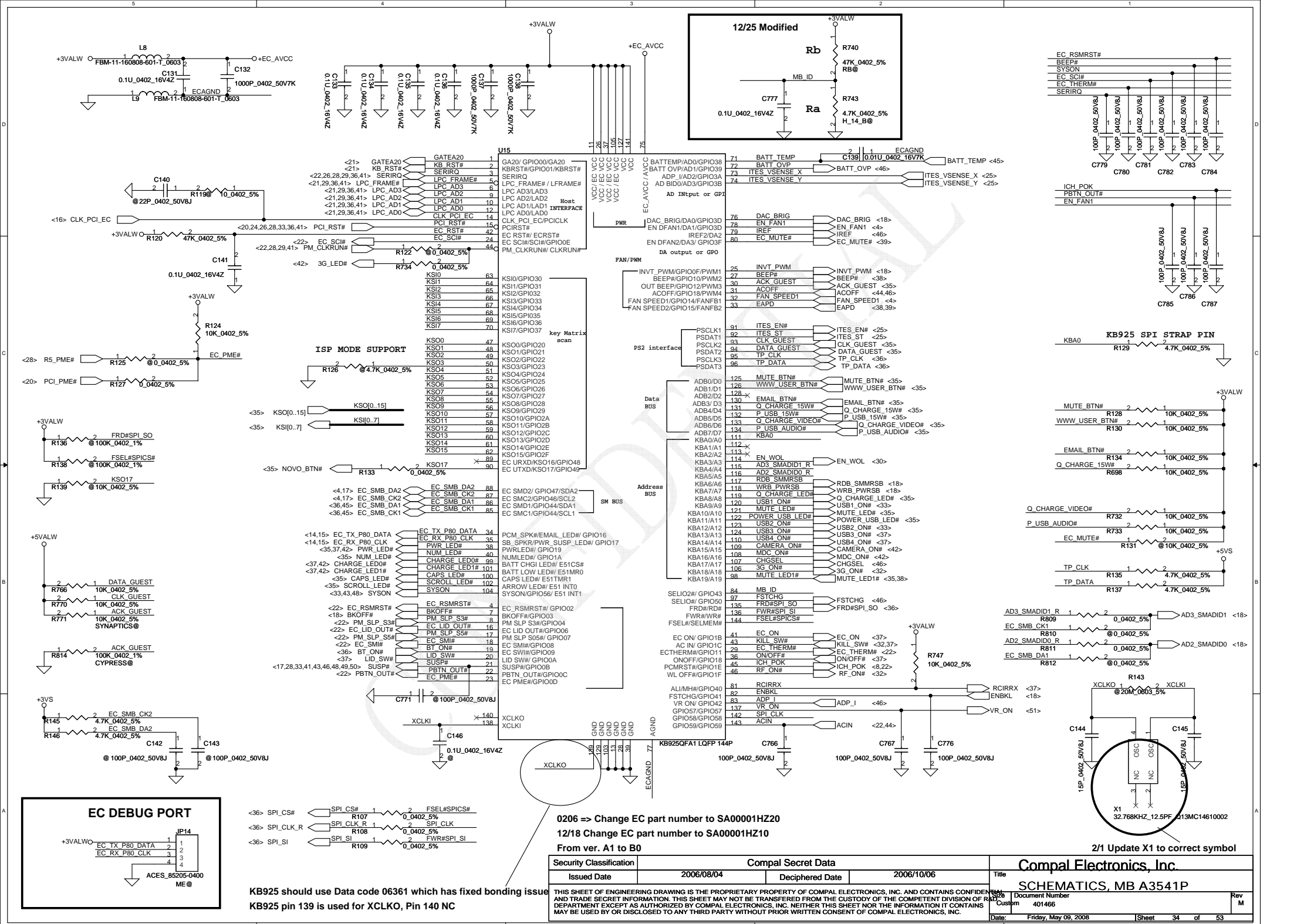


12/19 Add



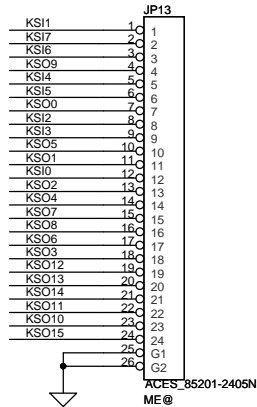
9/17 modified this block

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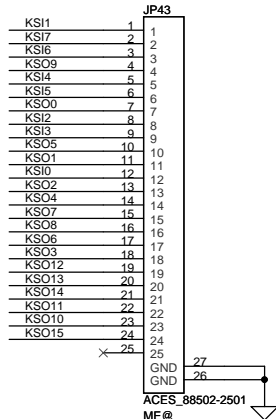


INT_KBD Conn.

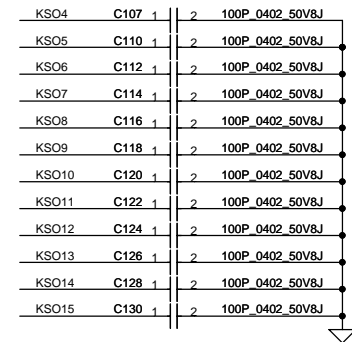
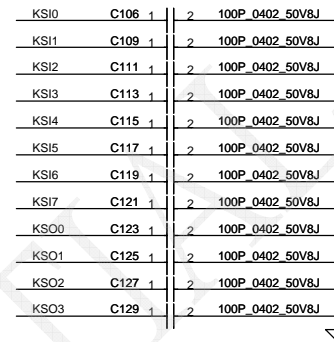
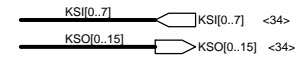
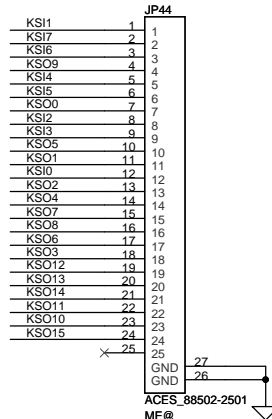
For IFT10



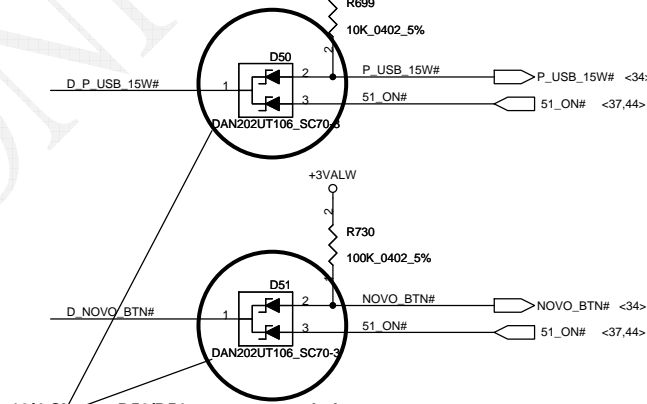
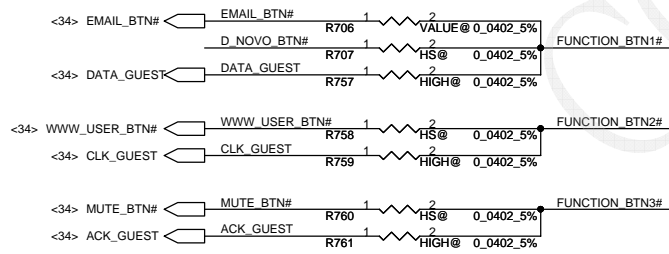
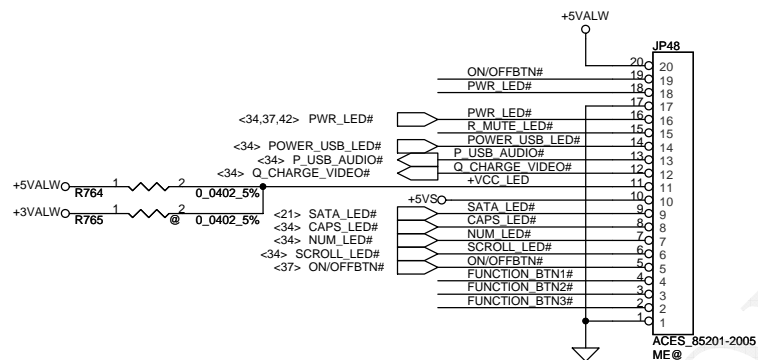
For IFL90



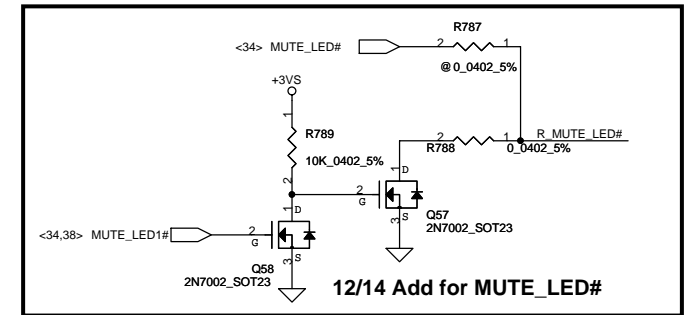
For IFT00



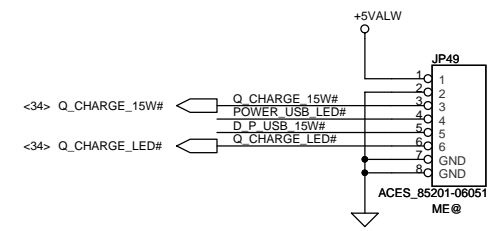
Switch Board Conn.



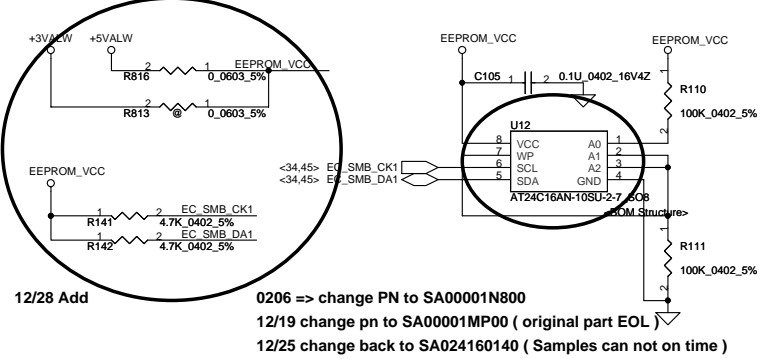
12/4 Change D50/D51 to correct symbols



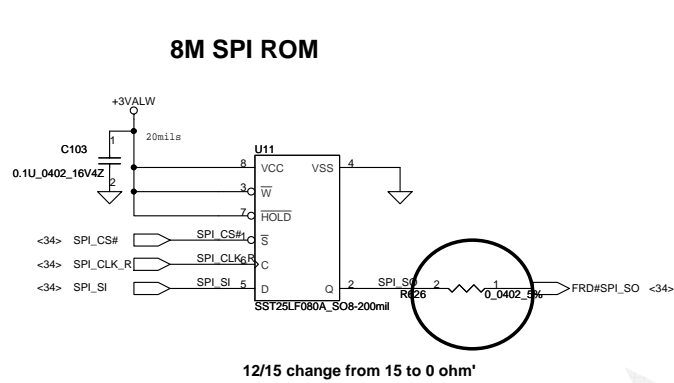
Video Switch Board Conn.



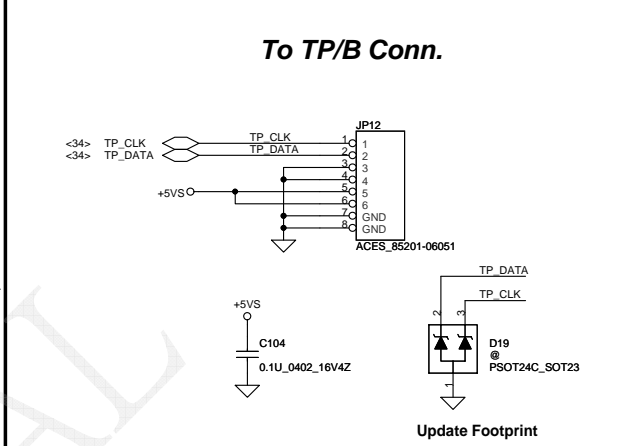
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12/28 Add
0206 => change PN to SA00001N800
12/19 change pn to SA00001MP00 (original part EOL)
12/25 change back to SA024160140 (Samples can not on time)



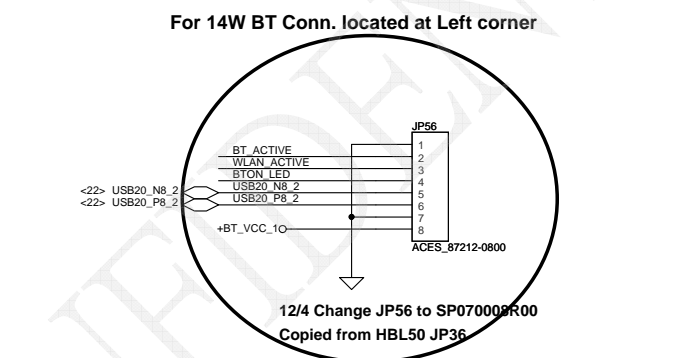
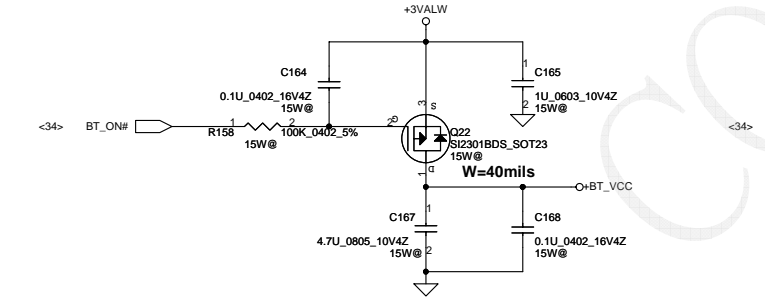
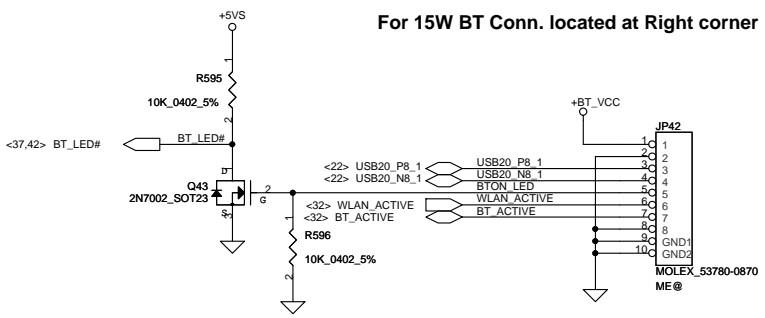
12/15 change from 15 to 0 ohm'



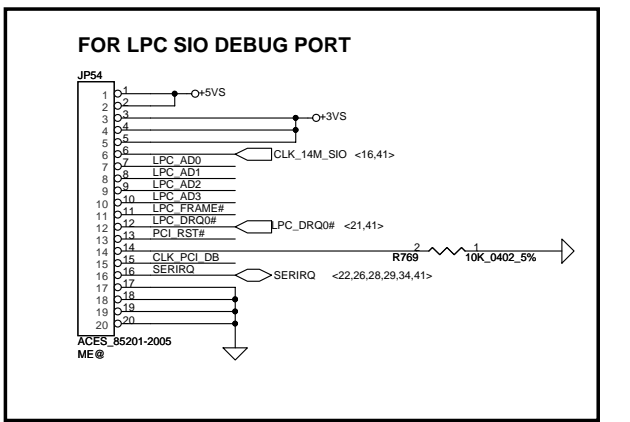
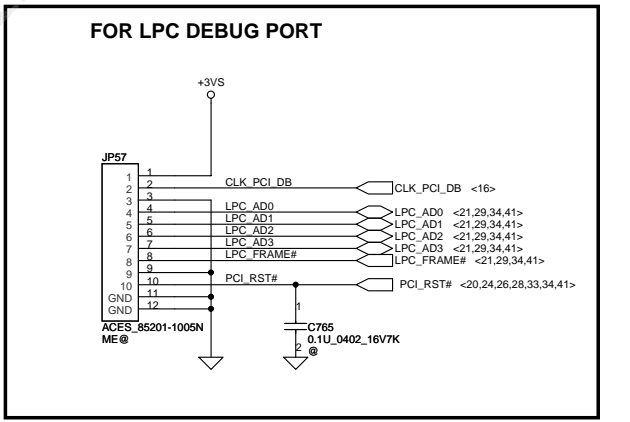
Update Footprint

Bluetooth Conn.

Need to check BT pin definition again!
9/20 modified this block

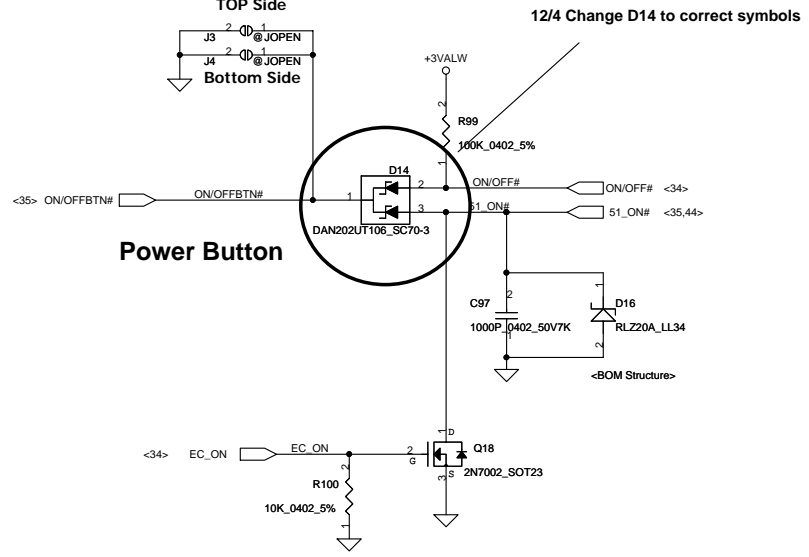


12/4 Change JP56 to SP070000R00
Copied from HBL50 JP36

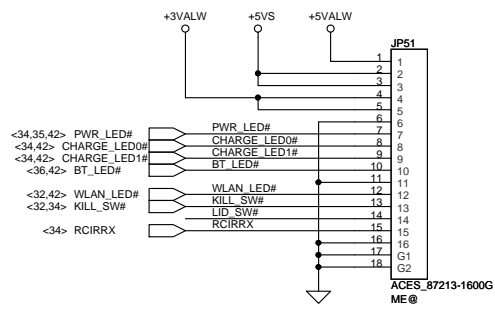


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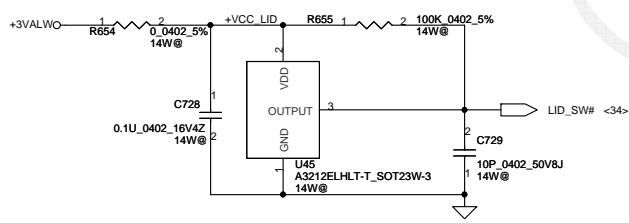
ON/OFF switch



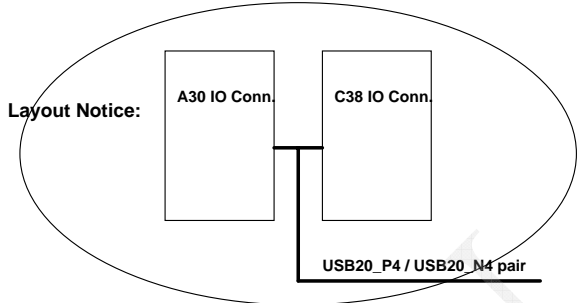
Front LED Board



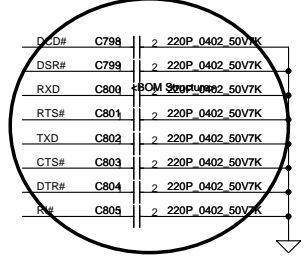
Lid Switch



Layout Notice:

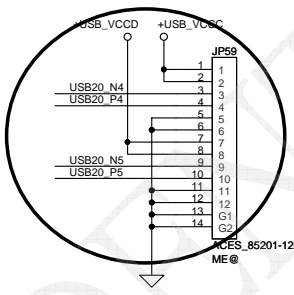


0208 Add 220pF for EMI

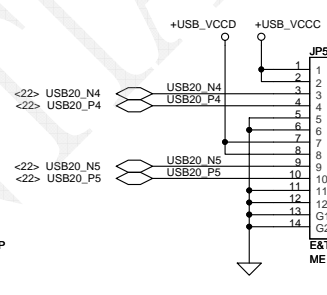


0207 Add JP59 0209 Change Symbol for GND PAD

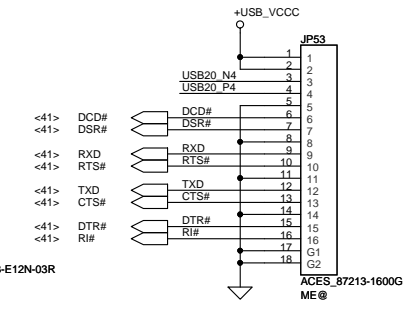
For 15W IO Conn.



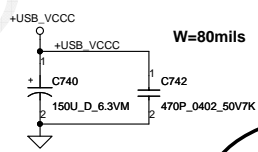
For 14W IO Conn.



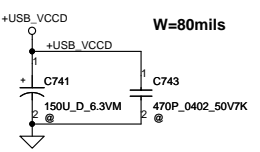
For C38 IO Conn.



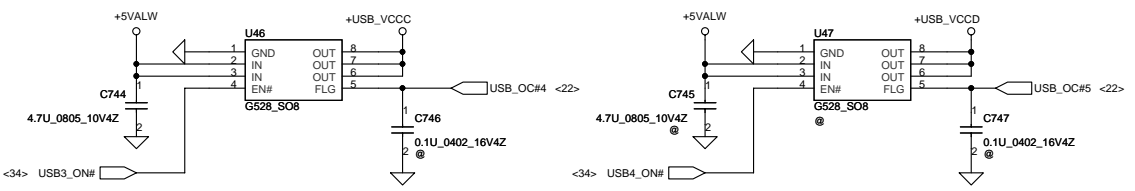
To USB CONN. 3



To USB CONN. 4

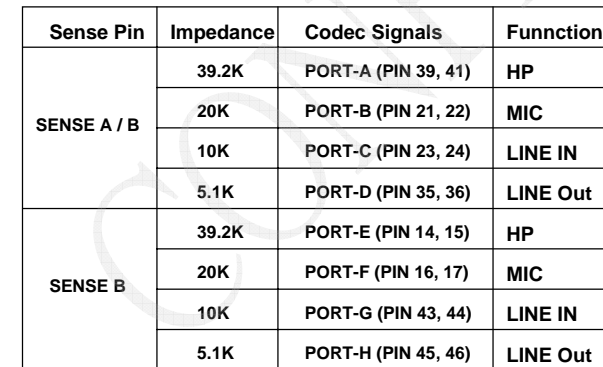


12/19 Add
12/27 modified to A30@



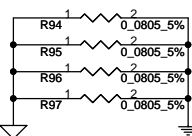
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C				D				E			

+AVDD_AC97 +3VS_DVDD

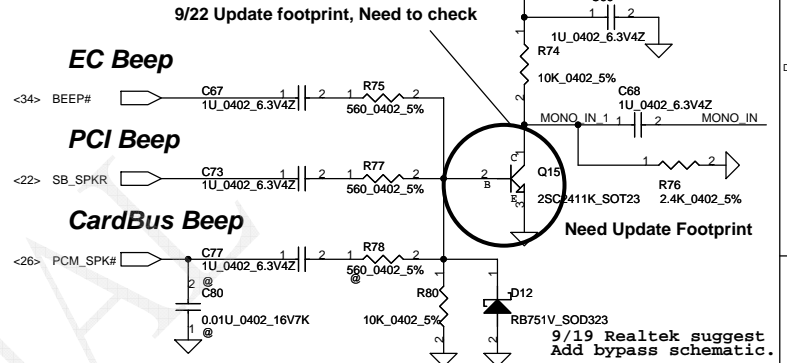


SENSE FOR Solo Int. Mic.

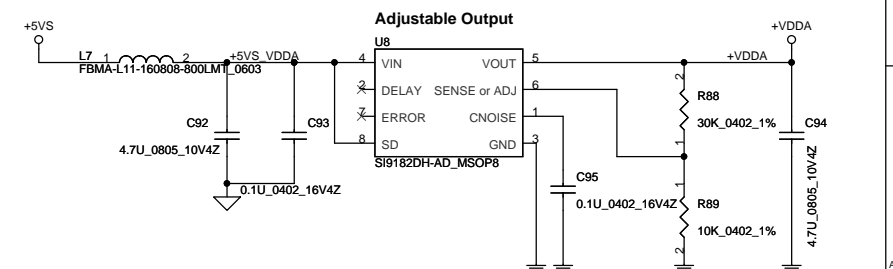
SENSE FOR HP



CardBus Beep

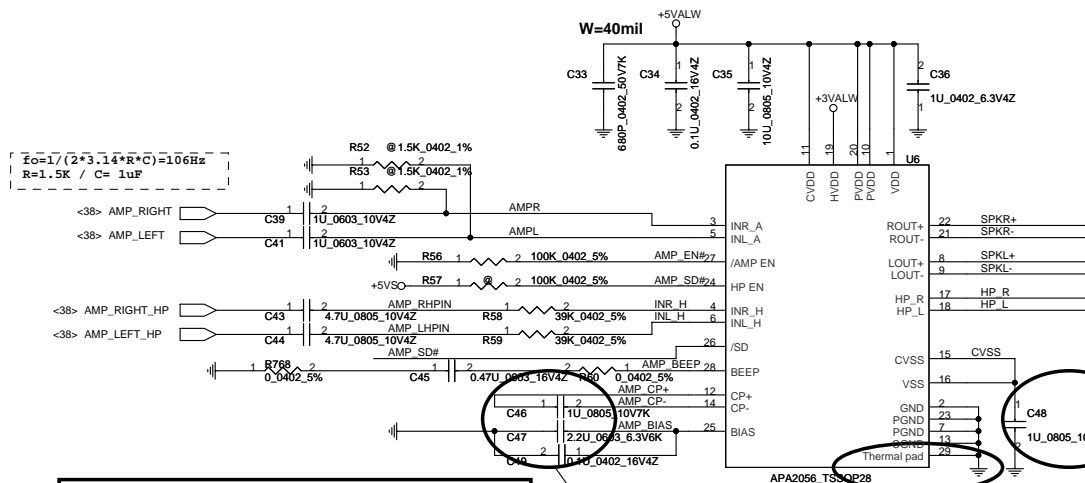


Regulator for CODEC



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APA2056 SPK/HP Amplifier



**9/5 If implement AMP BEEP, Swap C155 and R79.
R79 change from 0 Ohm to 47K**

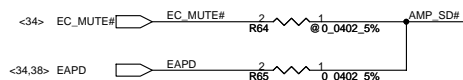
IN_A Gain = 10dB (Internal Speaker)
IN_H Gain = 0dB (Headphone)

12/1 Modified to X7R

12/27 C46 change PN to SE092105K80

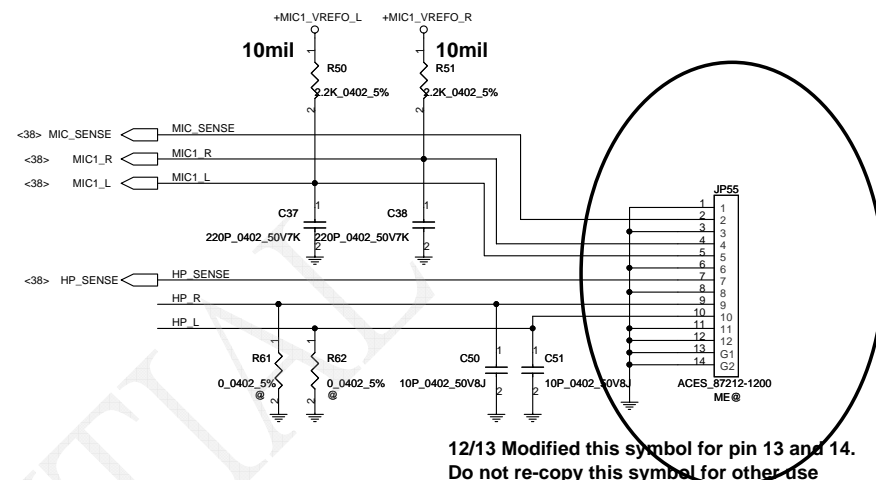
12/1 Modified to X7R

12/27 C48 change PN to SE092105K80



4/19 Modified this symbol to add pin29 for thermal pad use.

Do not re-copy this symbol for other use



12/13 Modified this symbol for pin 13 and 14.
Do not re-copy this symbol for other use

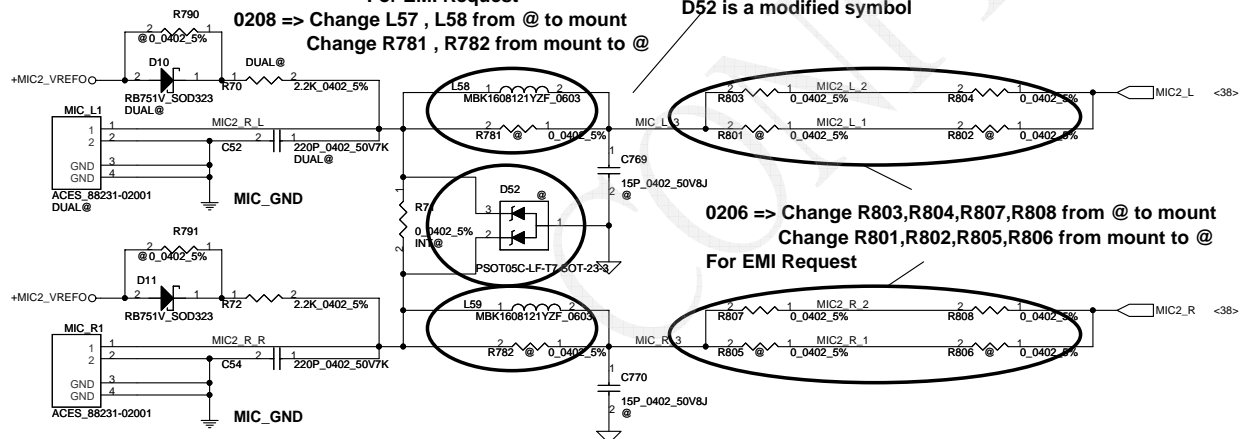


For EMI Request

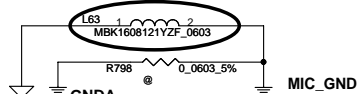
0208 => Change L57 , L58 from @ to mount
Change R781 , R782 from mount to

2/01 Add D52 for INT MIC use(PN:SCD0T05CA20)

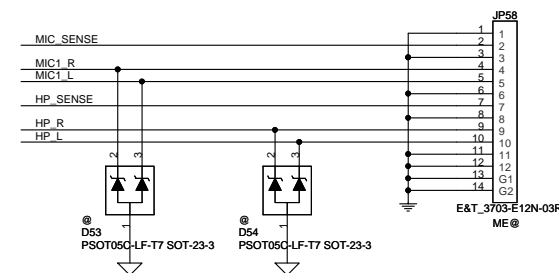
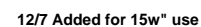
D52 is a modified symbol



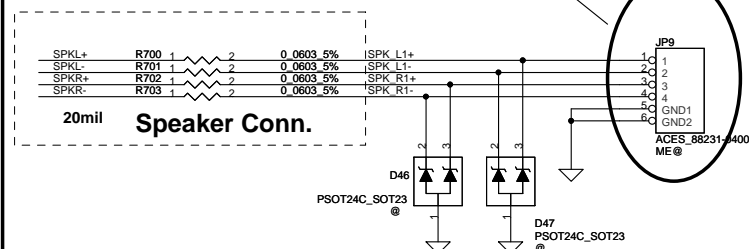
0208 => Remove R797 , Add L63 For EMI Request



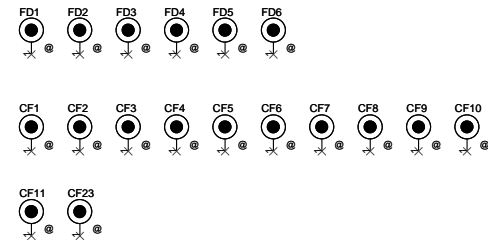
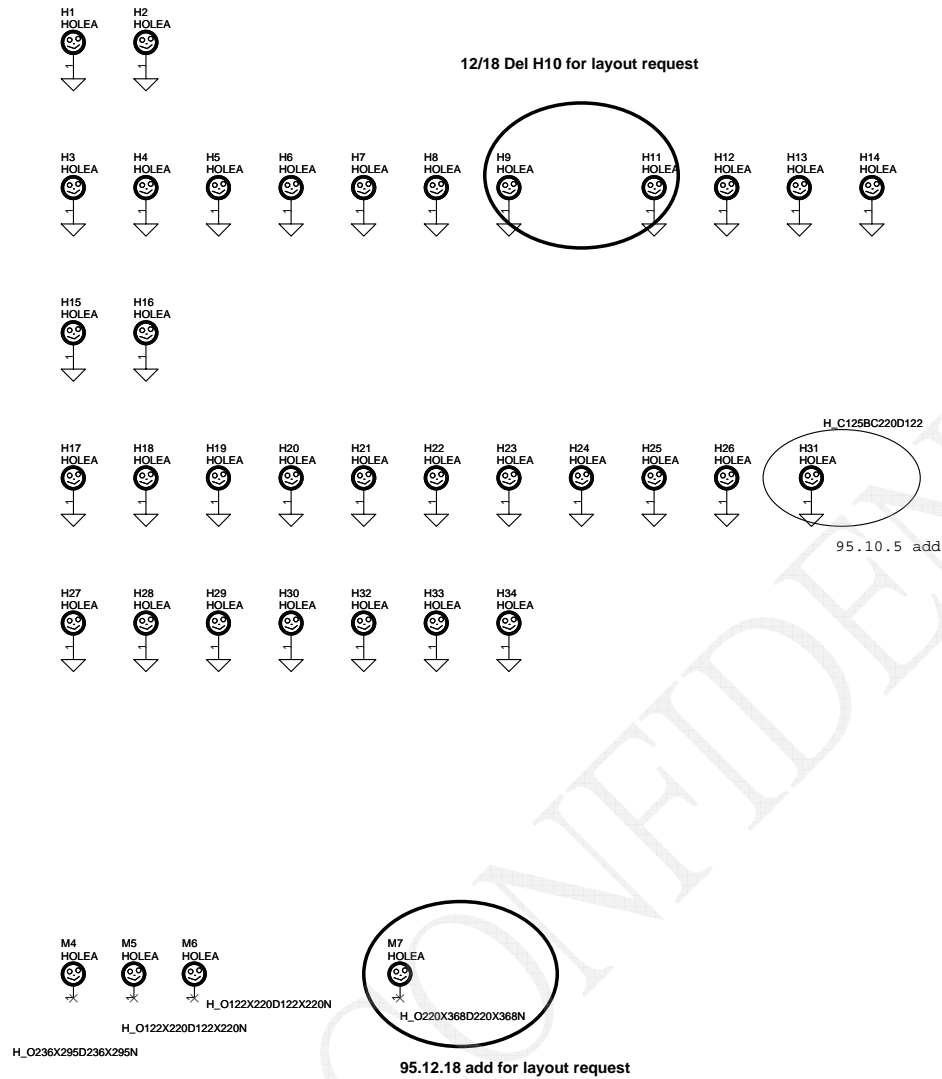
12/21 Place these parts close to CODEC (U7)



1/31 change JP9 following JP50

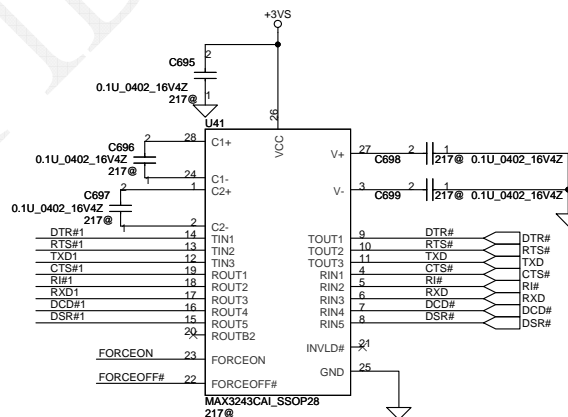
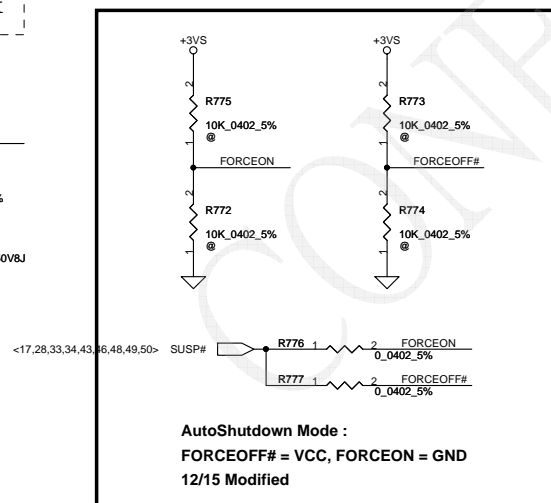
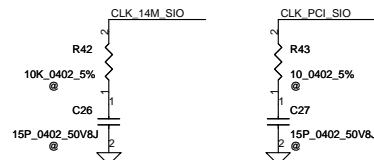
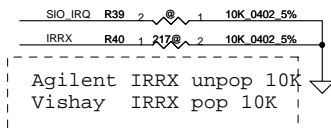
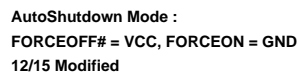


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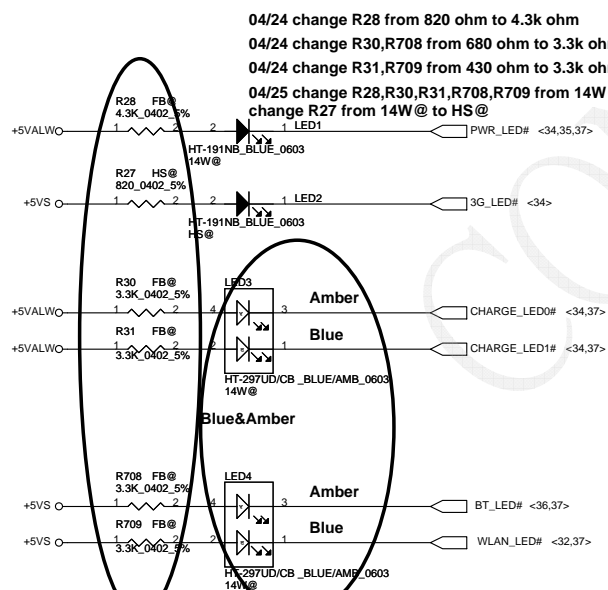
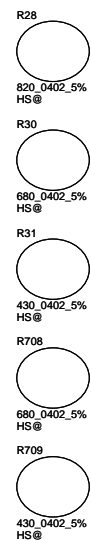
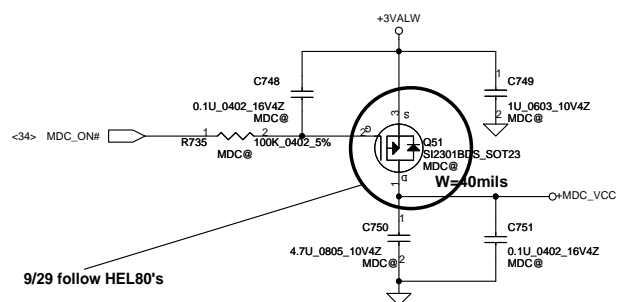
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9/18 modify this page following IGT1x



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LED

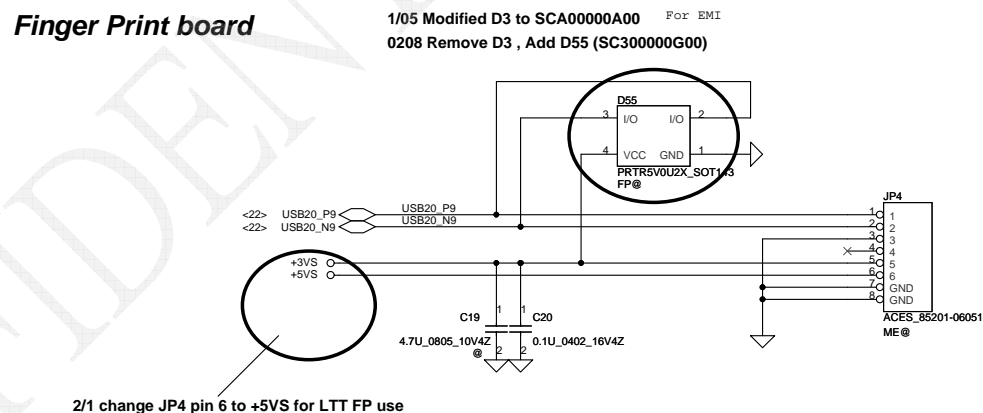
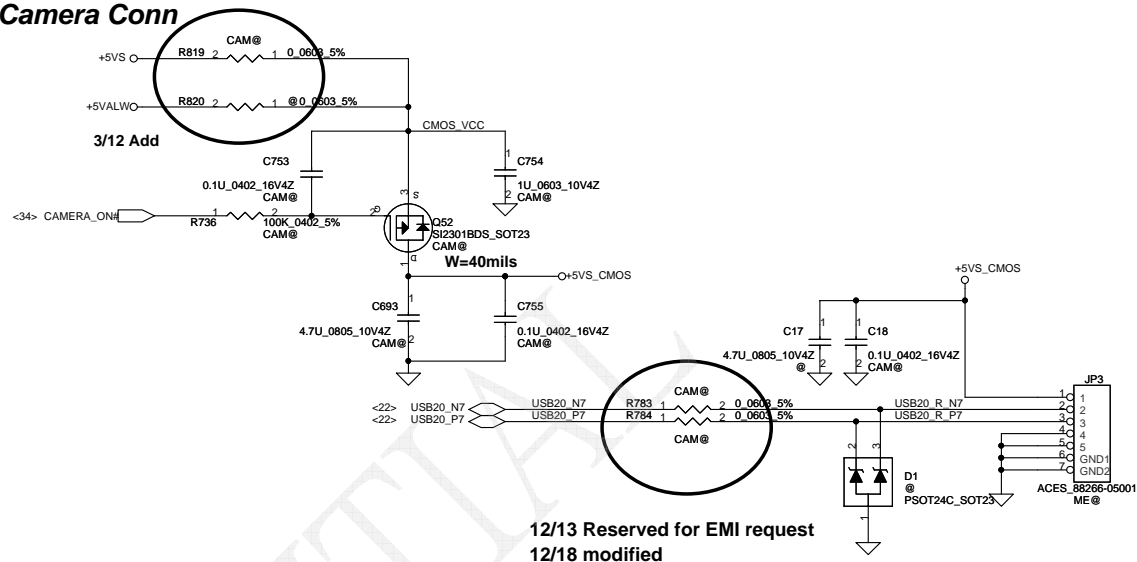


04/24 change R28 from 820 ohm to 4.3k ohm
04/24 change R30,R708 from 680 ohm to 3.3k ohm
04/24 change R31,R709 from 430 ohm to 3.3k ohm
04/25 change R28,R30,R31,R708,R709 from 14W @ to A30 @ ,
change R27 from 14W @ to H5 @

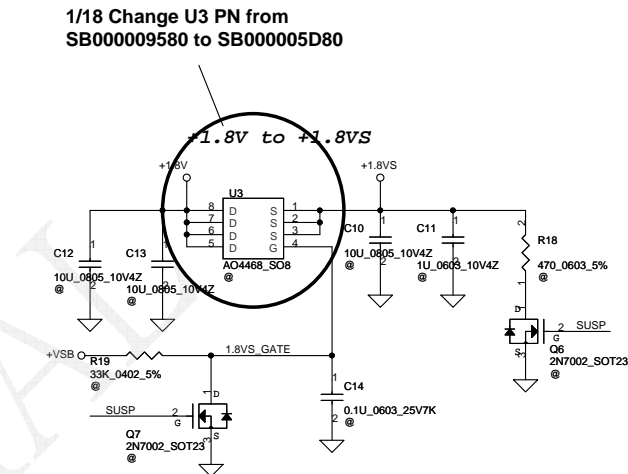
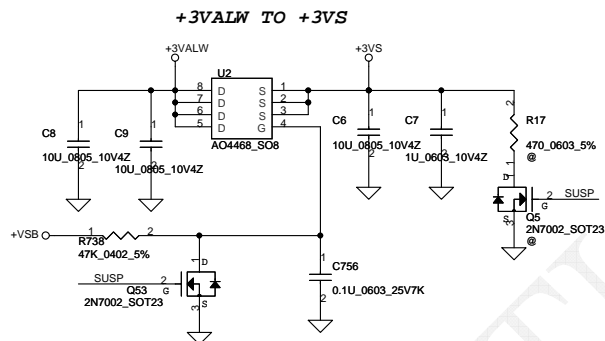
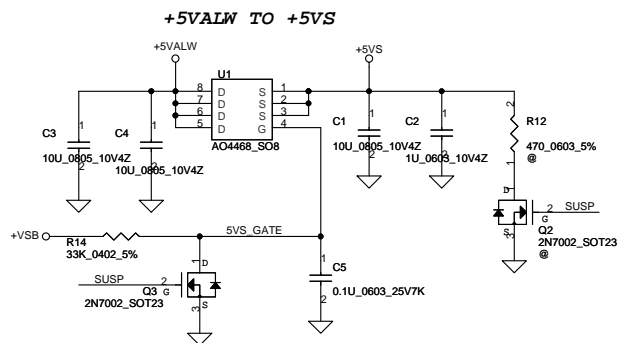
04/25 Add R28,R30,R31,R708,R709 for HS@

12/7 Modified LED footprint to LED_HT-297UD-CB_4P
12/15 Modified to correct LED symbol!

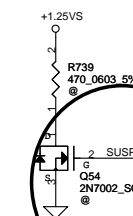
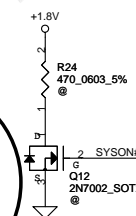
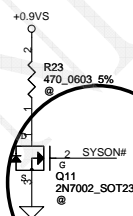
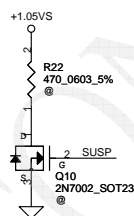
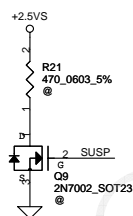
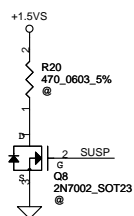
Finger Print board



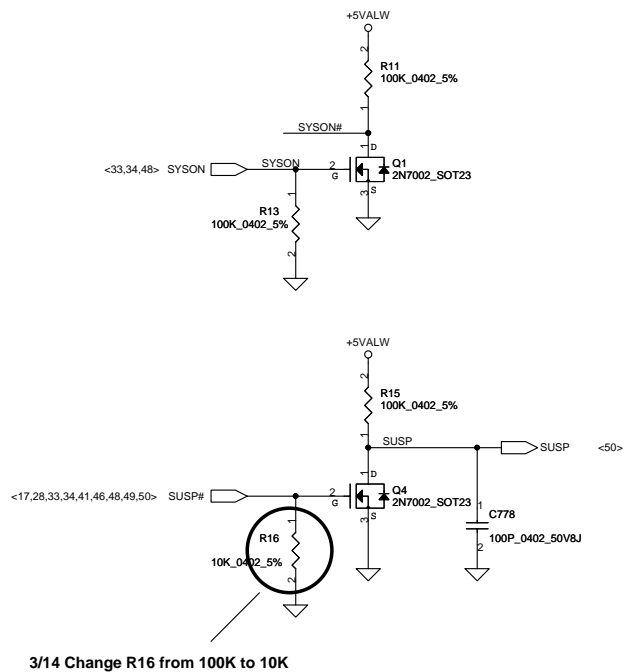
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0409 Change U3,Q7,R19,C10,C11,C12,C13,C14 from PM@ to @@



12/7 Modified

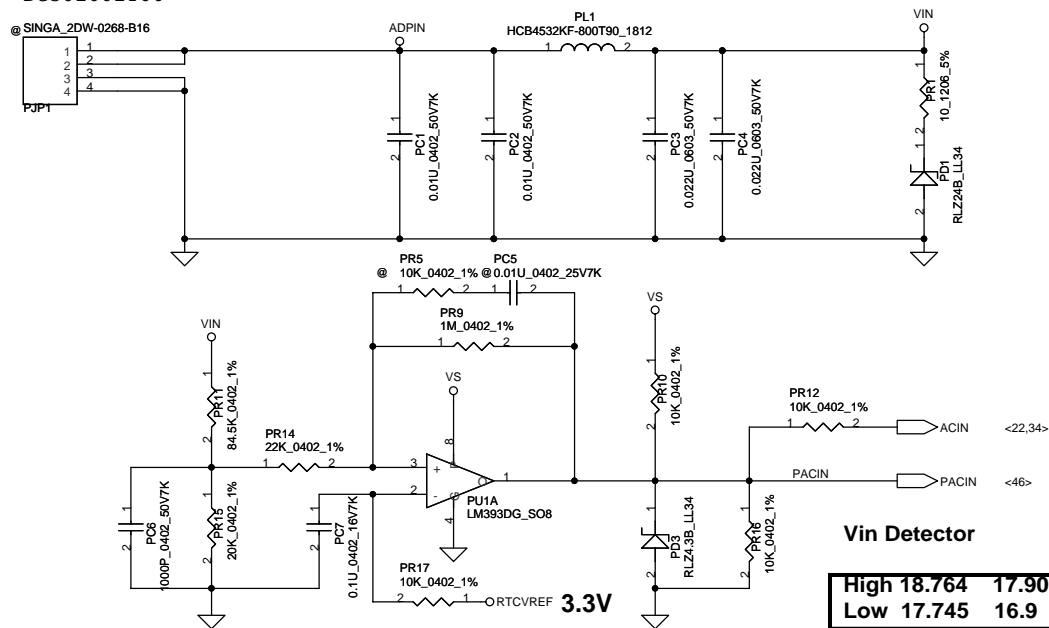


3/14 Change R16 from 100K to 10K

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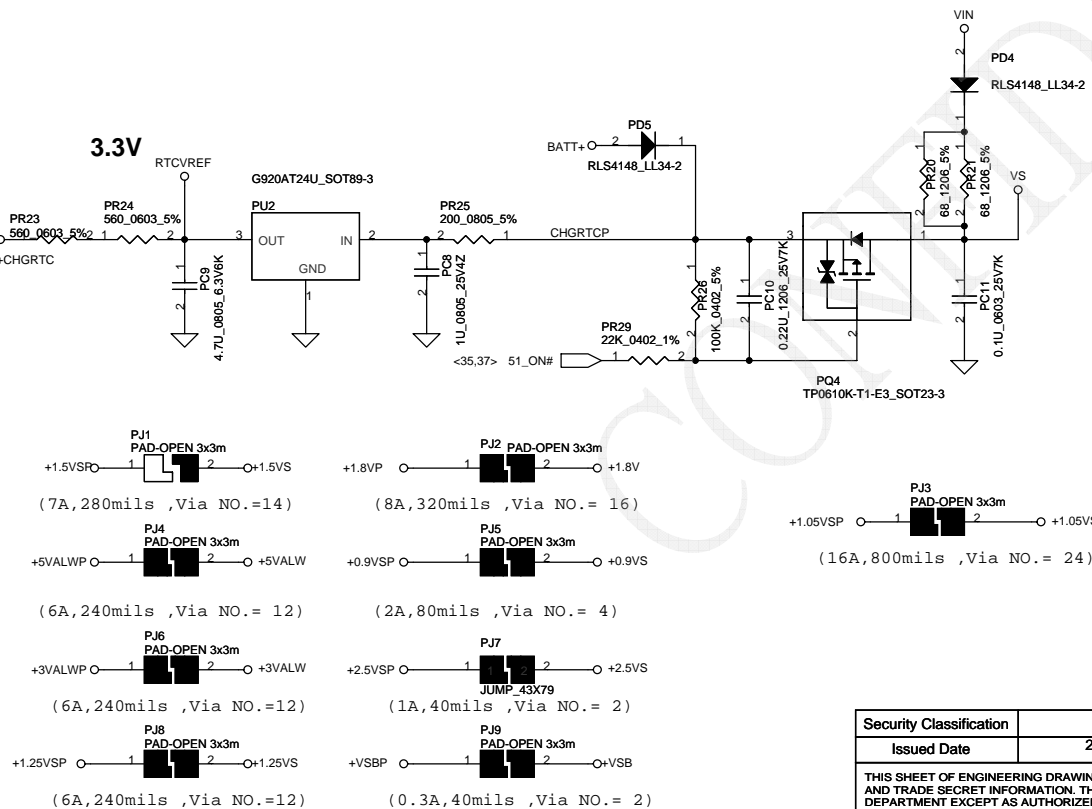
DC301001Y00

@ SINGA_2DW-0268-B16



Vin Detector

High	18.764	17.901	17.063
Low	17.745	16.9	16.03



ACIN

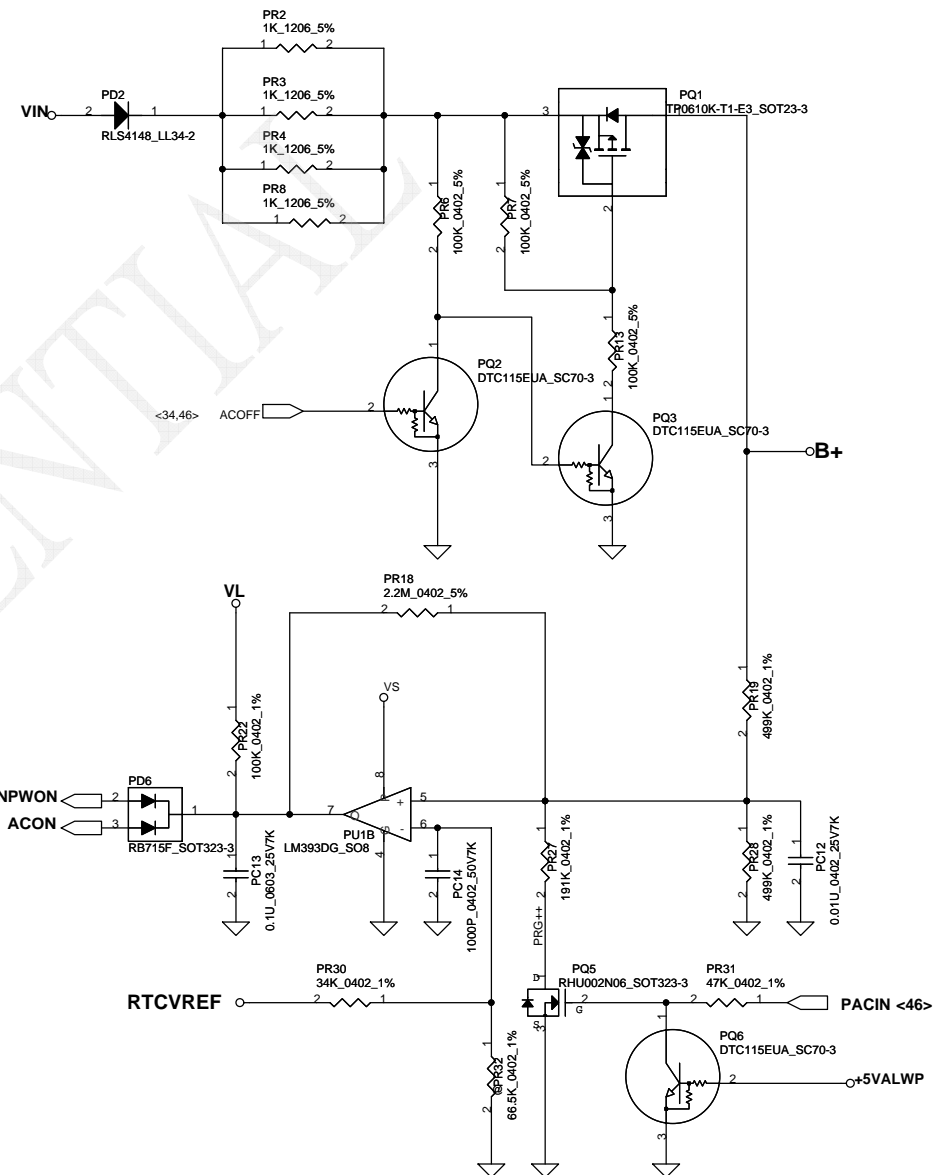
Precharge detector

	Min.	typ.	Max
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

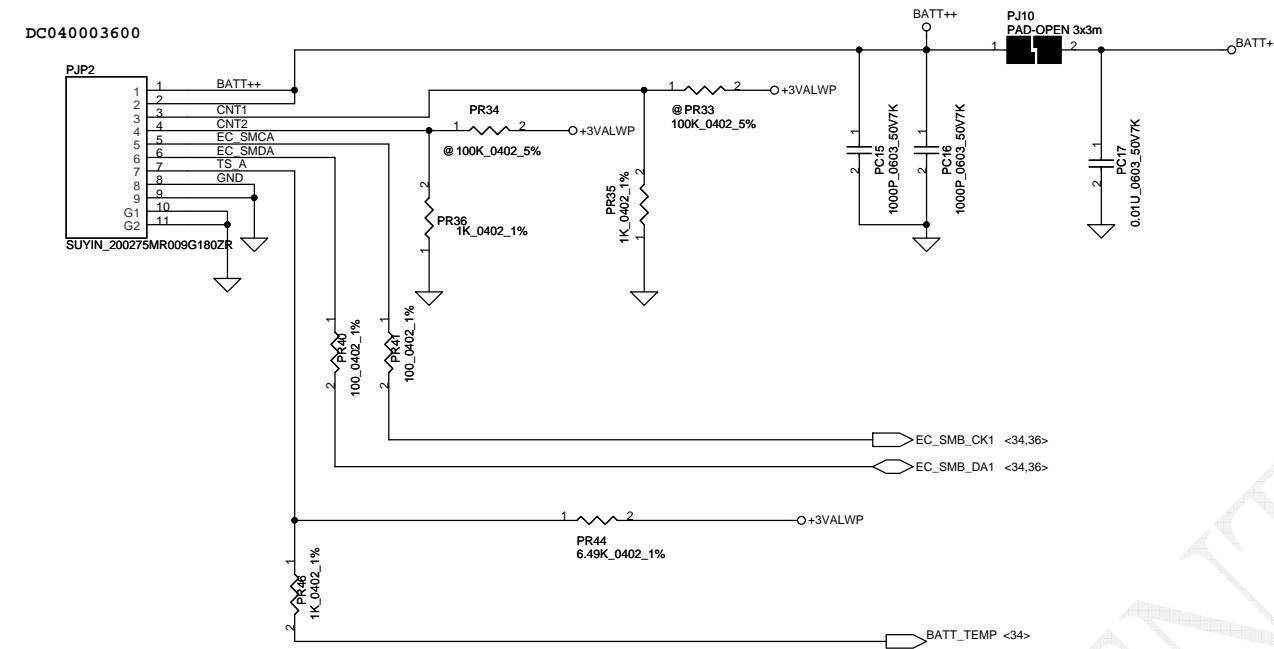
BATT ONLY

Precharge detector

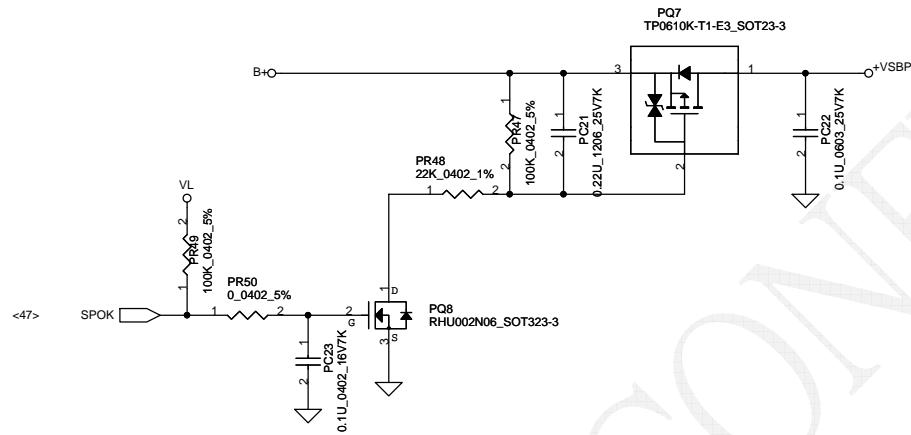
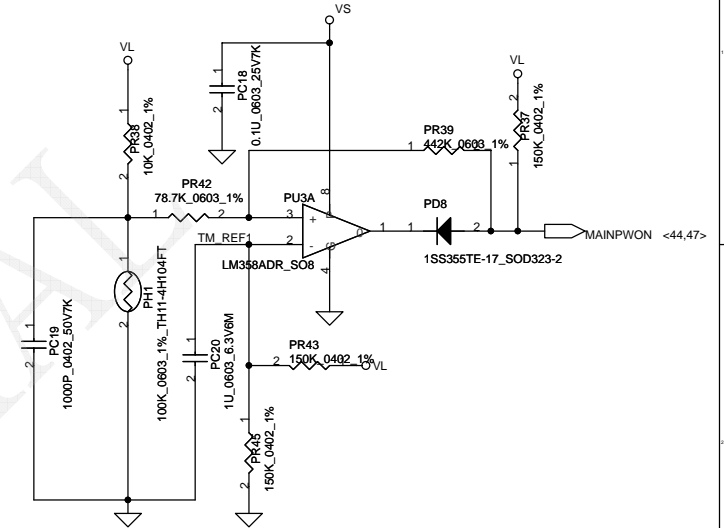
	Min.	typ.	Max
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V



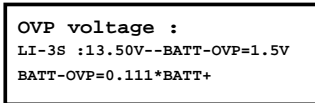
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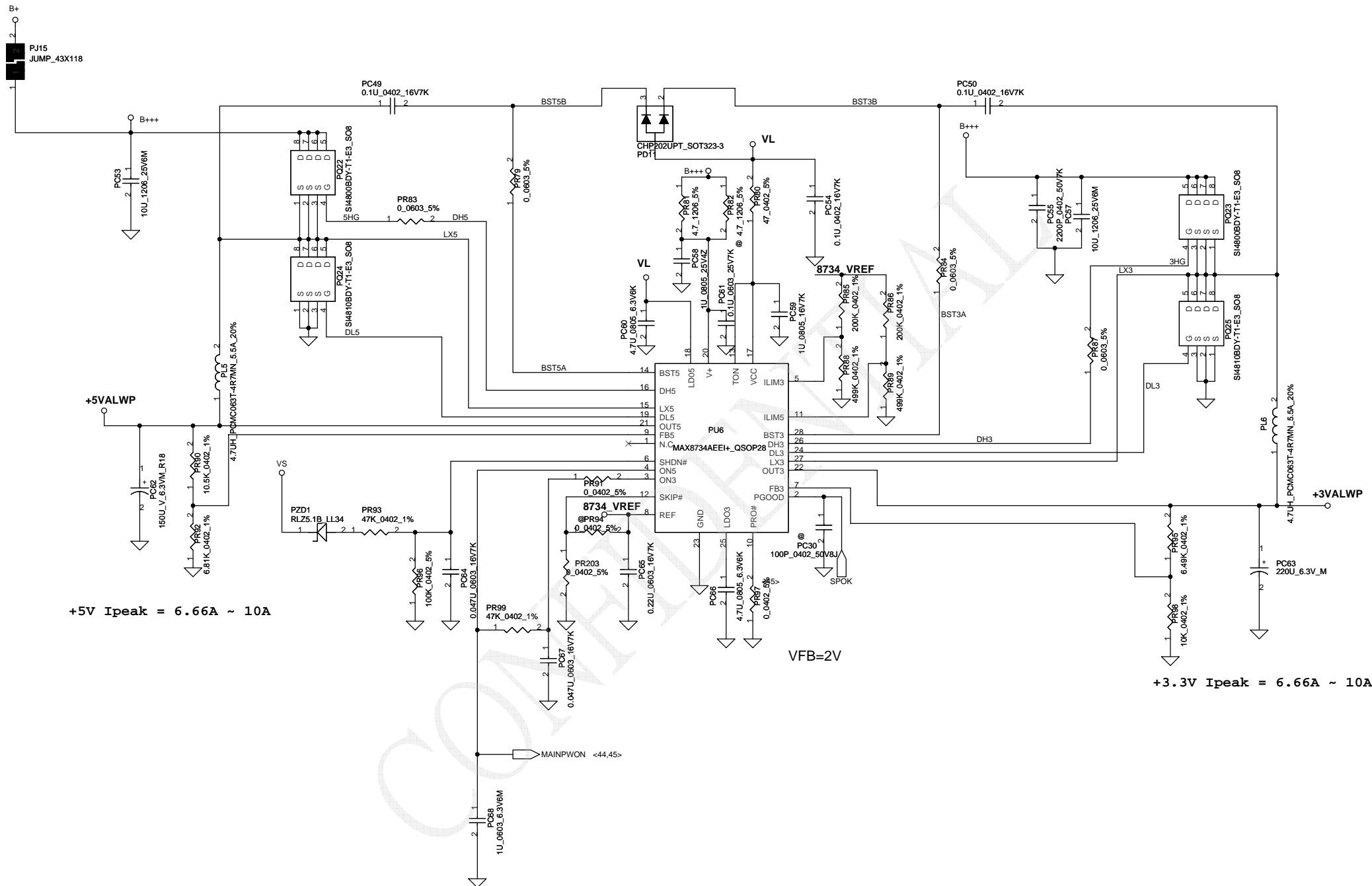
PH1 under CPU bottom side :
CPU thermal protection at 85 degree C
Recovery at 70 degree C



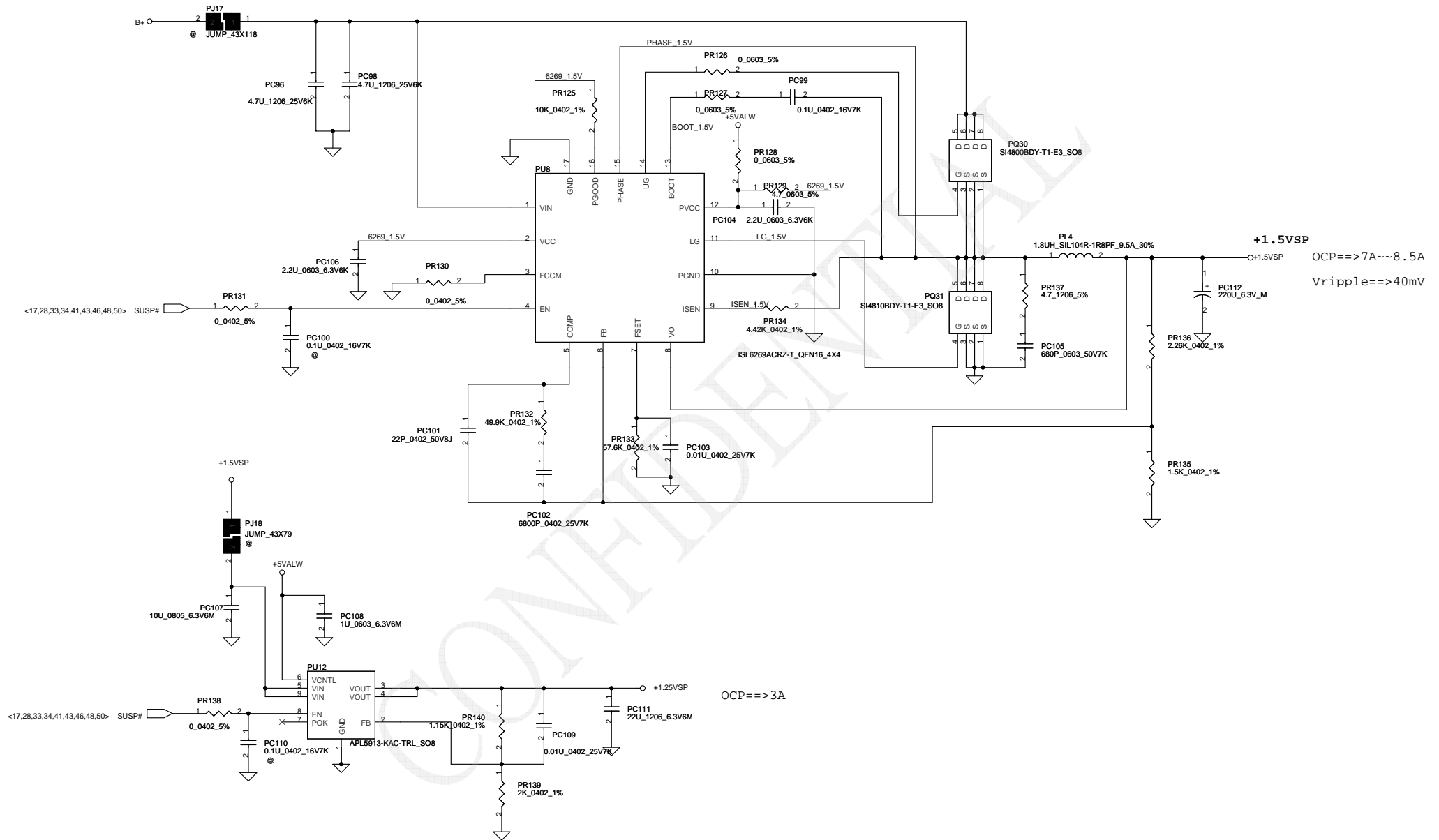
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$$ADP_I = 19.9 \cdot I_{\text{adapter}} \cdot R_{\text{sense}}$$


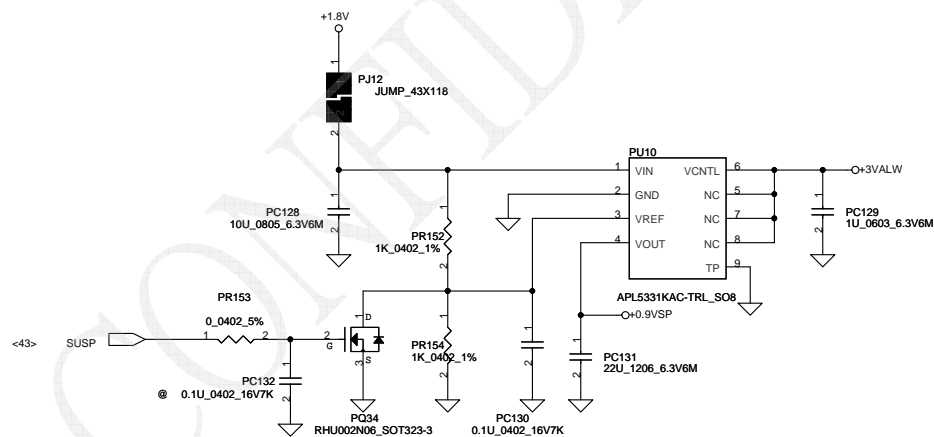
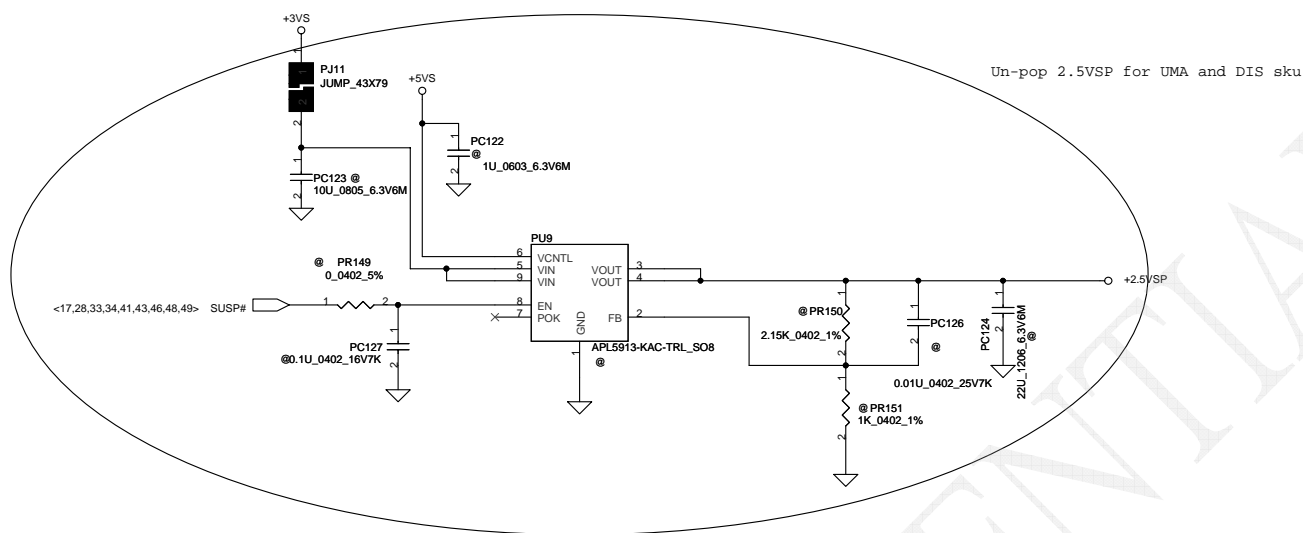
BATT Type	Charging Voltage (0x15)	CHGSEL	CV mode
2800mAH 3S pack	13050mV	LOW	12.90V
Normal 3S LI-ON Cells	12600mV	HIGH	12.60V



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	page	Reason for change	Modify list																																
DVT	Pre EVT	P50	For H/W 0.9V sequence deamd	Delete PQ34																															
			Modify Bead to Jump for costdown	PL1,PL2,PL4,PL7,PL10																															
			Modify 10UH/X6S to 10UH/X5R for common source	PC53,PC57,PC96,PC116,PC134,PC135,PC136,PC152,PC153,PC154																															
			Modify CH751H to RB751V for common source	PD10																															
	95/12/28		Keep Batt_OVP to 1.5V	Change PR78 form 150K to 105K																															
			Take out PC148 & PC150 form VTT tool test	Delete PC148 &PC150																															
			Adjust PR183 to 39.2K for loadline	PR183																															
			Modify CPU_High side form SI7840 to SI7686 for vender shortage	PQ35,PQ38																															
			Modify PosCAP to Alu CAP for cost	PC63,PC87,PC99																															
			DFX footprint issue, Modify RLS4148_LLDS2 to LL34	PD2,PD4																															
			Add skip mode function form skip pin of 3/5V IC	PR203																															
			ADD Battery in function in page 45	PR204,PR205,PR206,PR207,PR208,PC51,PC52,PQ41																															
			Defence charger IC leakage current in page 46	PR57,PR209,PR210,PR211,PR212,PC118,PC97,PC56,PD16,PD17,PQ42,PQ43,PQ44																															
			ADD Battery in and DC-IN Bead	PL1,PL2																															
			ADD 100PF in SPOK PIN for noise but unpop	PC30																															
			ADD CPU high side gate resister 2.2 OHM for EMI demand	PR159,PR195																															
	96/01/03			Change PR137 to L/F	PR137																														
				Change PR95 form 6.81K to 6.49K for power loss	PR95																														
			Disable battery in function, EC control	PR204,PR205,PR206,PR207,PR208,PC51,PC52,PQ41																															
			Modify 0.01U_0402 to 1000P_0402	PC1,PC4																															
			Remove PR1 & PD1 for cost	PR1,PD1																															
			Modify AO4407 to FDS4435 for UMA cost	PQ10,PQ11,PQ9																															
			Modify RB751V to 1SS355 for cost	PD12,PD13,PD14,PD15,PD10																															
			Remove 2.5VSP function for UMA	PR149,PR150,PR151,PC122,PC123,PC124,PC126,PC127,PU9																															
			Change 1.05VSP High/Low side MOS for cost	PQ26,PQ27																															
			Change 0.9UH to 1.8uH for 1.05vsp cost	PL8																															
			Change PC72 330U/R9 to 330U/R15. and del PC88	PC72,PC88																															
			Add PR207 280K_0402 and delete PR202	PR207,PR202																															
			Modify PC139 for 100uH at 3000hurs	PC139																															
			Modify charge Low side gate to SI4800BDY	PQ19																															
<table><tr><td>Security Classification</td><td colspan="3">Compal Secret Data</td><td colspan="2">Compal Electronics, Inc.</td></tr><tr><td>Issued Date</td><td>2005/10/17</td><td>Deciphered Date</td><td>2006/10/17</td><td>Title</td><td></td></tr><tr><td colspan="4">THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</td><td>Document Number</td><td>Rev</td></tr><tr><td colspan="4"></td><td>401466</td><td>M</td></tr><tr><td colspan="4">Date: Friday, May 09, 2008</td><td>Sheet</td><td>52 of 53</td></tr></table>					Security Classification	Compal Secret Data			Compal Electronics, Inc.		Issued Date	2005/10/17	Deciphered Date	2006/10/17	Title		THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev					401466	M	Date: Friday, May 09, 2008				Sheet	52 of 53	
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page	Reason for change	Modify list
96/01/03 DVT	Disable battery in function, EC control	PR204,PR205,PR206,PR207,PR208,PC51,PC52,PQ41
	Modify 0.01U_0402 to 1000P_0402 for common design	PC1,PC4
	Remove PR1 & PD1 for common design	PR1,PD1
	Modify AO4407 to FDS4435 for UMA	PQ10,PQ11,PQ9
	Modify RB751V to 1SS355 for common design	PD12,PD13,PD14,PD15,PD10
	Remove 2.5VSP function for UMA sku	PR149,PR150,PR151,PC122,PC123,PC124,PC126,PU9
	Change 1.05VSP High/Low side MOS for rating	PQ26(SI4800),PQ27(Si4810)
	Change 0.9UH to 1.8uH for 1.05vsp rating	PL8
	Change PC72 form 330U/R9 to 330U/R15. and del PC88 for rating	PC72,PC88
	Add PR107 280K_0402 and delete PR202 for 1.05VSP OCP	PR107,PR202
	Modify PC75 form 4700P to 3300P for 1.05VSP OCP	PC75
	Modify PC139 for 100uH at 3000hurs	PC139
	Modify charge Low MOS gate to SI4800BDY	PQ19
96/01/19 DVT-2	Disable CC-CV overshoot function , need verify it.	PQ44
	0.9V sequence for H/W deamd	Add PQ34
	Change CPU low side mos to SI4856	PQ36,PQ37,PQ39,PQ40
96/01/19 PVT	Chage 1.5V/1.25V dual to single and LDO portion	DEL PR141,PR143,PR144,PR145,PR146,PR148,PC110,PC113,PC114,PC115,PC116,PC117,PC120,PC121,PL11,PL12, PQ32,PQ33,PD14,PD15 ADD PR125,PR126,PR136,PU12,PL4 Modify PR128,PR129,PR130,PR131,PR132,PR133,PR134,PR135,PR136,PR137,PR138,PR139,PR140 PC96,PC98,PC99,PC101,PC102,PC103,PC104,PC105,PC106,PC107,PC108,PC109,PC111,PC112 PU8 Del PU5,ADD PD8 PD5 PC49,PC50,PC74,PC84,PC81 Remove PC147 for cost PC147 Change PC128 form 10U_1206 to 10U_0805 for cost PC128
96/02/16 PVT 96/03/14 PVT-2	Modify CPU OTP 85 degree C to 89 degree C for thermal request	PR42_78.7K, PR38_10K
	Add CC-CV overshoot function	Add PR213,PR214, Modify PC34,PC37,PR62 Del PC118,PC32,PR211,PR212
	Modify PR125 for common source	PR125
96/03/19 Pre-MP	Modify PC1,PC2,PC3,PC4 for EMI request	PC1,PC2=>0.01uF PC3,PC4=>0.022uF
	Modify PC139 form 100uf to 220uf for nosie issue in IFT1X	PC139
	Modify PC3,PC4 to 0.022uF_0603_50V	PC3,PC4
	Modify PR141 to 0603 size	PR141
	Add PR1,PD1 to prevent P2 high voltage	PR1,PD1
96/04/22 Pre-MP	Modify PR35 to 1K ,prevent ID pin short gnd directly	PR35
96/05/30 ECO	Adjust loadline	DEL PC133, Modify PR168 and PR199 to 4.02K Modify PC145 and PC159 to 0.1U, PR183 to 3.92K

Add PC148 and PC150 to 1000PF	Security Classification	Compal Secret Data		Compal Electronics, Inc.	
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