COMP 421 MPU Design Guidelines

MINIMUM Design Requirements

1. 2 bidirectional I/O port registers
2. 8-bit data bus
3. 16-bit address bus
4. Dual Data format
    a. Signed Integer and BCD format
5. ALU
    a. Arithmetic
        i. ADD, SUB (both for integer and BCD)
        ii. INC, DEC
        iii. L-SHIFT, R-SHIFT
    b. Logic
        i. AND
        ii. OR
        iii. XOR
        iv. NOT
6. Register Set[1]
    a. Accumulator
    b. Status (Flag) Register
        i. Sign
        ii. Zero
        iii. Carry
        iv. Overflow
        v. Half-Carry
    c. General Purpose Registers (minimum of 2, accumulator NOT INCLUDED)
    d. Program Counter
    e. Instruction Register
    f. Stack Pointer
    g. Extended Register pair/s
    h. Index Register[2]
7. Control Unit Design (Hardwired Control Unit)[3]
    a. Instruction Decoder / State Counter
    b. State Decoder
    c. Control Logic
    d. Timing Circuits

- The internal architecture of the memory module is NOT INCLUDED in the design. However, external interface pins (data, address, and control) to and from the microprocessor MUST be included in the design.
- The designer must use TTL logic family only. Device specification sheets MUST be included in the documentation.

- Include design computations in the appendix.
  - Noise margin
  - Device fan-out
  - Timing considerations (propagation delay, maximum clock speed)
  - Power dissipation
- Include a final bill of materials

Total: 30% of Final Grade (see Grading system)

- Group with the highest score gets a **50 point bonus**.
- Deduction for late submissions: 5 pts per day of delay (including weekends)

NO DESIGN AND/OR NO DOCUMENTATION = NO DEFENSE

Notes:
[1] The microprocessor's instruction set MUST be based on the minimum register set
[2] Register index instructions are REQUIRED
[3] Control unit is microsequencer-based (see Carpinelli)