$=X_{L2}/2$, and is clear that the optimum occurs at any

be calculated respectively.

(12.93)

(12.94)

(12.95)

(12.96)

be calculated, respectively.

$$X_{L1} = \omega L_1 = \frac{R_s(Q_L^2 + 1)}{Q_L - \sqrt{\frac{R_s(Q_L^2 + 1)}{R_s} - 1}}.$$
 (12.98)

This circuit can match resistances

$$\frac{R_i}{Q_L^2 + 1} < R_s < R_i. ag{12.99}$$

Suboptimum operation takes place for

$$R_{s(sub)} > R_s \tag{12.100}$$

and therefore for

$$R_{i(sub)} < R_i. \tag{12.101}$$

12.7 DESIGN EXAMPLE

EXAMPLE 12.1

Design the Class E ZVS inverter of Fig. 12.1(a) to satisfy the following specifications: $V_I = 100 \text{ V}$, $P_{Rimax} = 80 \text{ W}$, and f = 1.2 MHz. Assume D = 0.5.

Solution: It is sufficient to design the inverter for the full power. Using (12.48), the full-load resistance is

$$R_i = \frac{8}{\pi^2 + 4} \frac{V_I^2}{P_{Ri}} = 0.5768 \times \frac{100^2}{80} = 72.1 \,\Omega. \tag{12.102}$$

From (12.41), the DC resistance of the inverter is

$$R_{DC} = \frac{\pi^2 + 4}{8}R_i = 1.7337 \times 72.1 = 125 \,\Omega. \tag{12.103}$$

The amplitude of the output voltage is computed from (12.46)

$$V_{Rim} = \frac{4}{\sqrt{\pi^2 + 4}} V_I = 1.074 \times 100 = 107.4 \text{ V}.$$
 (12.104)

The maximum voltage across the switch and the shunt capacitor can be calculated from (12.43) as

$$V_{SM} = 3.562V_I = 3.562 \times 100 = 356.2 \text{ V}.$$
 (12.105)