BM

Brief Manual of MiDAS3.0 Family

FLASH / ISP / IAP
8-bit Turbo Microcontrollers

V1.8

October 2008

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Contents

1. Product Overviews

- **CORERIVER's MiDAS3.0 Family is a group of fast 80C52 compatible microcontrollers**
- **The instruction execution of MiDAS3.0 is max. 3 times faster than that of traditional 80C52.**
  - ✓ **1 Machine cycle = 4 clocks vs. 12 clocks**
- **Additional peripherals of MiDAS3.0 Family:**
  - ✓ **10 bit ADC / 12 PWM outputs in two 6-module PCA's / Extra UART / WDT / POR.**
- **Power saving modes**
- **Noise tolerant scheme**
- **Supports ISP / IAP of FLASH memory**
- **Provides User-Friendly MDS environment with on-chip HW debugging engine**
- **The Brief Manual contents could be updated at any time. Please check update contents from CORERIVER Web page (http://www.coreriver.com)**

1. Product Overview

A. MiDAS3.0 Family - GC80L590A Series (ISP Flash MCU)

Product	Mask-ROM (byte)	Flash (byte)	EEPROM (byte)	RAM (Byte)	Volt (V)	Freq. (MHz)	T/C (16bits)	Serial I/O	WDT	ADC (bit x ch)	PWM (bit x ch)	Package	Others	Available Time
GC89L591A0		64K	(2K)	16K + 256	1.6 ~ 2.0 (Core) 3.0 ~ 3.6 (I/O)	100	3	2 UART	1	10X32 10X21	8x12 Or 16X6 8x6 Or 16X3	44-PQFP 44-MQFP 44-LQFP 32-LQFP 32-MLF 32-QFN	ISP/IAP I2C EJTAG LVD POR	**Now**
GC81L591A0	64K													
GC89L581A0		32K	(2K)											
GC81L581A0	32K													
GC89L541A0		16K	(2K)											
GC81L591A0	16K													

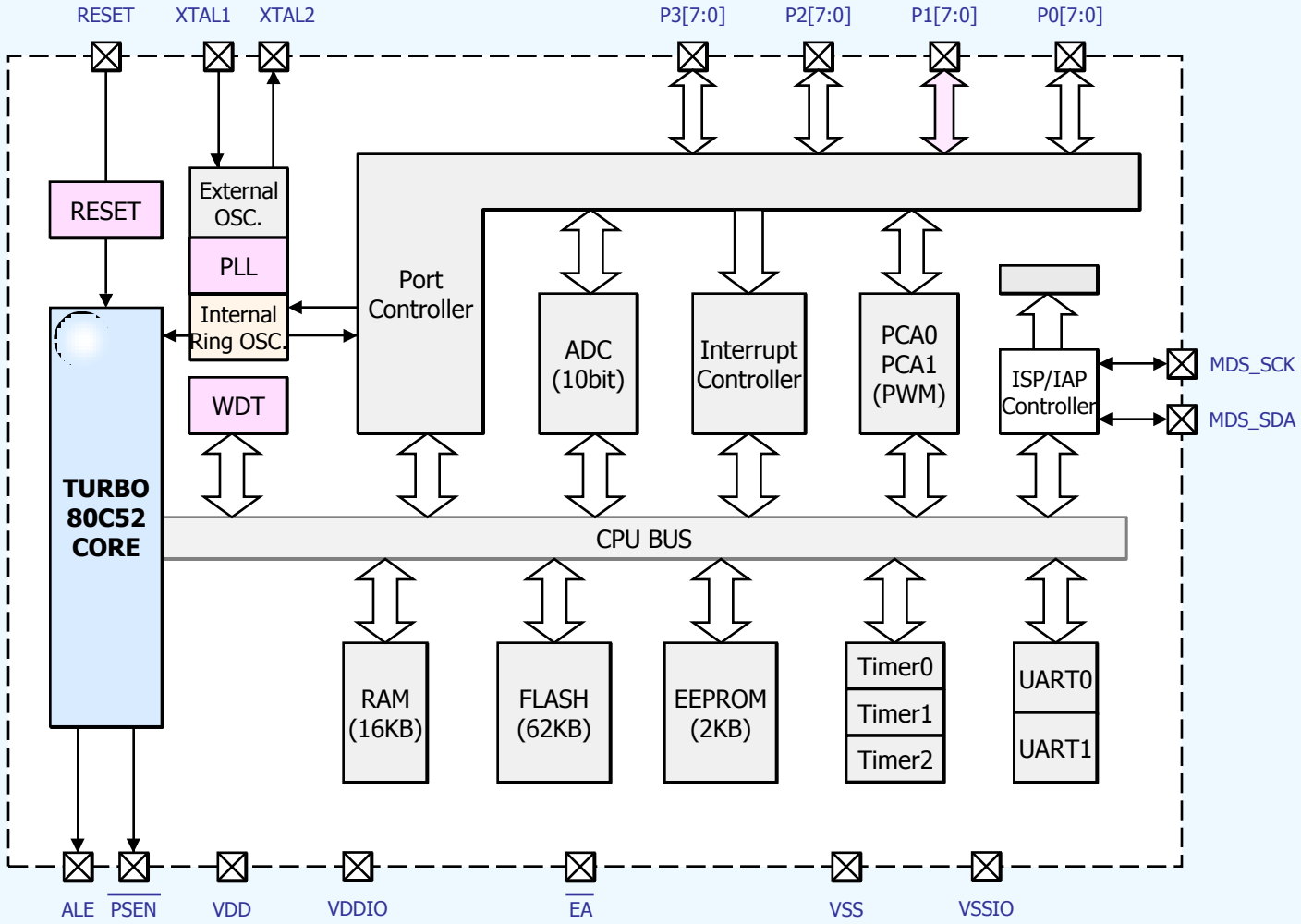
2. Features

- CPU
  - ✓ 8-bit turbo 80C52 architecture
  - ✓ 4 cycles/1 machine cycle
  - ✓ Pin/instruction level compatible with Intel 80C52
- 62 KBytes on-chip FLASH ROM
  - ✓ ISP by serial interface
  - ✓ IAP and virtual EEPROM for data (2KByte)
  - ✓ Endurance : Typ. 50,000 write/erase cycles.
    Min. 10,000 write/erase cycles.
- 16 KBytes on-chip RAM
  - ✓ 256 bytes IRAM
  - ✓ 16,384 bytes AUXRAM (Accessed with `MOVX`)
- Max. 32 programmable I/O pins
  - ✓ Open-drain Intel compatible ports : P0
  - ✓ Quasi-bidirectional Intel compatible ports : P1 ~ P3
  - ✓ Push-pull type ports : P0 ~ P3
  - ✓ Input/Output and pull-up control : P0 ~ P3
  - ✓ TTL & CMOS compatible logic levels : P0 ~ P3
  - ✓ All ports are initialized during power-on reset.
- EMI reduction mode : Inhibit ALE
- 27-bit Programmable Watchdog Timer
- 10-bit 32-channel ADC
- Three 16-bit Timer/Counters
- Two Full-Duplex UART
  - ✓ Automatic address recognition
- Two Programmable Counter Arrays
  - ✓ 8-bit/16-bit dynamic PWM (12 channels).
  - ✓ 16-bit Compare/Capture counter (12 channels).
  - ✓ High Speed Output (12 channels).
- 16 interrupt sources (with 6 external sources)
  - ✓ Timer0/1/2, UART0/1, PCA0/1, WDT, ADC, I2C and 6 External
  - ✓ Four/Two-level interrupt priority

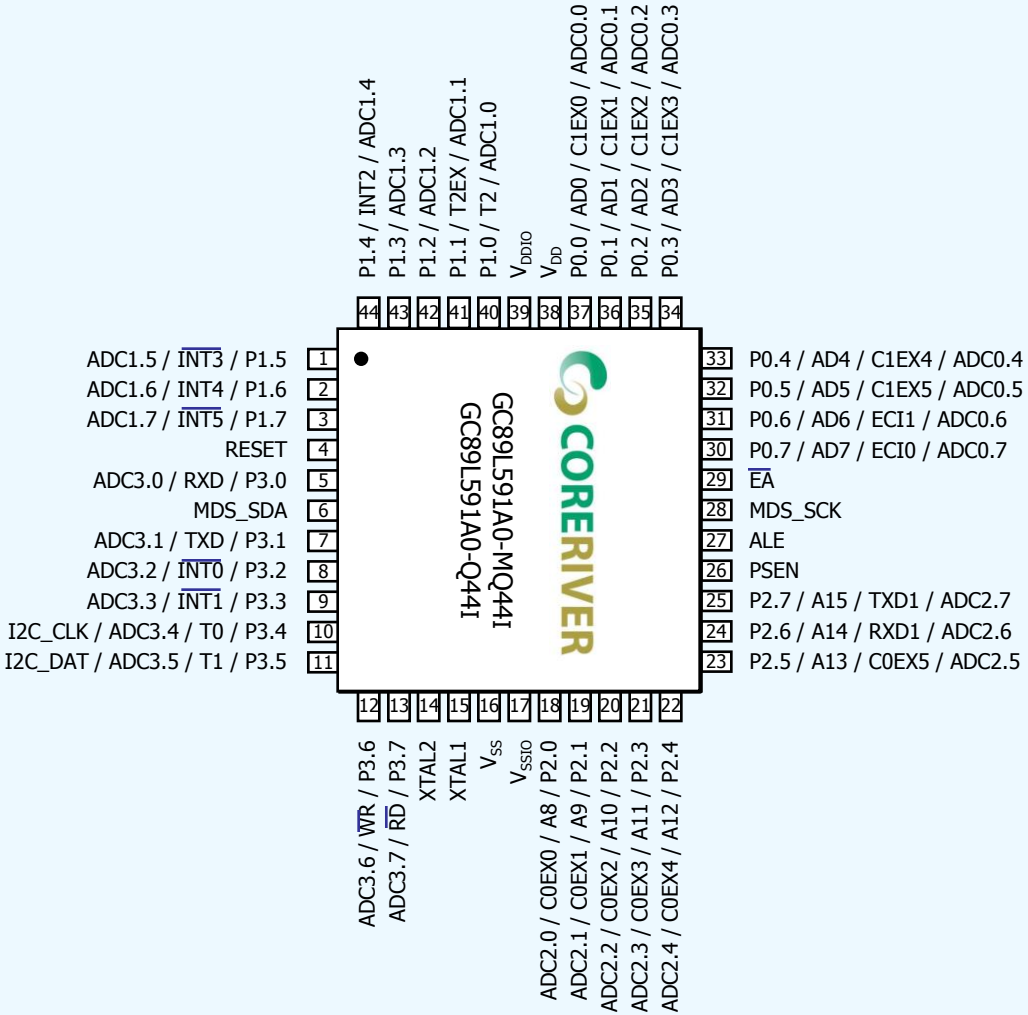
2. Features (Cont'd)

- Wake-up from power-down mode
  - ✓ On-chip power-on-reset
  - ✓ External reset
  - ✓ External interrupt 0/1/2/3/4/5
  - ✓ WDT interrupt or reset
- Reset scheme
  - ✓ On-chip power-on-reset
  - ✓ External reset
  - ✓ Low voltage detector reset
  - ✓ Watchdog timer reset if enabled
- Internal delay for power stabilization
  - ✓ MCU starts after 50ms from power-up.
- On-chip PLL
  - ✓ VCO operating frequency : 70MHz ~ 130MHz
  - ✓ PFD comparison frequency : 2MHz ~ 20MHz
  - ✓ Support 2bits output divider, 2bits input divider
  - ✓ Support 8bits feedback divider
- Supply voltage
  - ✓ Core : 1.62V ~ 1.98V
  - ✓ IO : 1.62V ~ 3.6V
- Operating temperature & Frequency
  - ✓ Max 100MHz @ -20 °C ~ 85 °C
  - ✓ Max 80MHz @ -40 °C ~ 125 °C
- Power consumption
  - ✓ Active current : Typ. 50mA @ 1.8V, 100MHz
  - ✓ Stop current : Typ. 10uA @ 1.8V
- E.S.D. protection up to 2,000V
- Latch-up protection up to ±200mA
- Package
  - ✓ 44-MQFP/PQFP/LQFP
  - ✓ 32-MLF/QFN

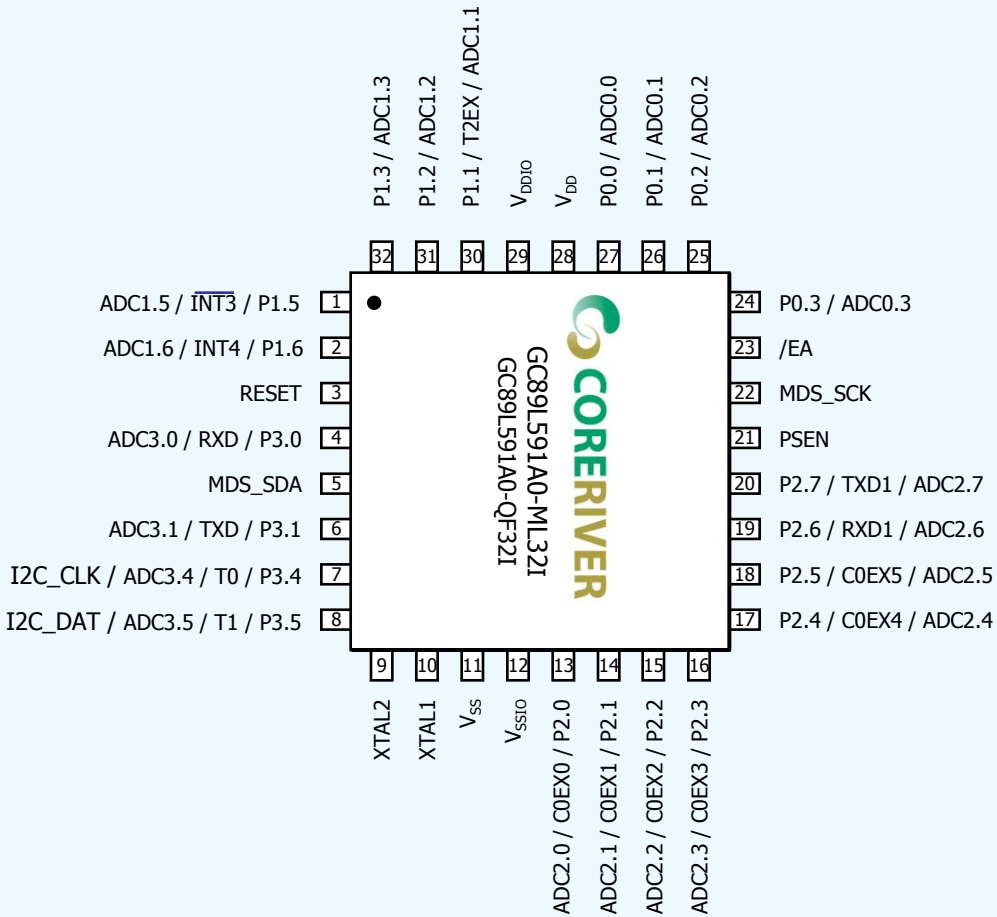
3. Block Diagram



4. Pin Configurations (44-MQFP/PQFP/LQFP)



4. Pin Configurations (32-MLF / QFN)



5. Pin Descriptions

Symbol	Direction	Description	Share Pins
VDD	Input	Power Supply	-
VDDIO	Input	IO Power Supply	-
VSS	Input	Ground	-
VSSIO	Input	IO Ground	-
RESET	Input	External Reset	-
XTAL1	Input	Input to the inverting Oscillator amplifier	-
XTAL2	Output	Output from the inverting Oscillator amplifier	-
/EA	Input	External ROM Access Enable (MiDAS3.0 family dose not use this pin.)	-
ALE	Input/Output	Address Latch Enable (If ALEOFF is set, active only for external RAM access) This pin is also used for the parallel programming of FLASH memory.	-
PSEN	Input/Output	Program Strobe Enable. Pull-up. Used for Special Input only. (MiDAS3.0 does not support the code fetch from external ROM.)	-
MDS_SDA, MDS_SCK	Input/Output	I/O for ISP. The pull-up resistor is always switched on. This port is quasi-bidirectional.	-

5. Pin Descriptions (Cont'd)

Symbol	Direction	Description	Share Pins
P0[7:0]	Input/Output	◆ An 8-bit open-drain or push-pull I/O port or ADC Input(3.3V). 5V Tolerant Input. ◆ Note that the output is fully driven (push-pull) when P0 drives address/data to access external RAM or PCA1 drives output signals (C1EXn). • P0.0 ~ P0.7 → AD0 ~ AD7 : Low address or data input/output • P0.0 ~ P0.5 → C1EX0 ~ C1EX5 for PCA1 • P0.6 → ECI1 for PCA1 • P0.7 → ECI0 for PCA0 • P0.0 ☐ ADC0.0 : A/D converter Input 0 • P0.1 ☐ ADC0.1 : A/D converter Input 1 • P0.2 ☐ ADC0.2 : A/D converter Input 2 • P0.3 ☐ ADC0.3 : A/D converter Input 3 • P0.4 ☐ ADC0.4 : A/D converter Input 4 • P0.5 ☐ ADC0.5 : A/D converter Input 5 • P0.6 ☐ ADC0.6 : A/D converter Input 6 • P0.7 ☐ ADC0.7 : A/D converter Input 7	P0.0 / AD0 / ADC0.1 / C1EX0 P0.1 / AD1 / ADC0.2 / C1EX1 P0.2 / AD2 / ADC0.3 / C1EX2 P0.3 / AD3 / ADC0.4 / C1EX3 P0.4 / AD4 / ADC0.5 / C1EX4 P0.5 / AD5 / ADC0.6 / C1EX5 P0.6 / AD6 / ADC0.7 / ECI1 P0.7 / AD7 / ADC0.8 / ECI0
P1[7:0]	Input/Output	◆ An 8-bit Quasi-bidirectional or push-pull I/O port or ADC Input(3.3V). 5V Tolerant Input. • P1.0 ☐ T2 : External Input for Timer/Counter 2 • P1.1 ☐ T2EX : Timer/Counter 2 Capture/Reload Trigger • P1.4 ☐ INT2 : External Interrupt 2 (Positive Edge) • P1.5 ☐ $\overline{\text{INT3}}$: External Interrupt 3 (Negative Edge) • P1.6 ☐ INT4 : External Interrupt 4 (Positive Edge) • P1.7 ☐ $\overline{\text{INT5}}$: External Interrupt 5 (Negative Edge) • P1.0 ☐ ADC1.0 : A/D converter Input 8 • P1.1 ☐ ADC1.1 : A/D converter Input 9 • P1.2 ☐ ADC1.2 : A/D converter Input 10 • P1.3 ☐ ADC1.3 : A/D converter Input 11 • P1.4 ☐ ADC1.4 : A/D converter Input 12 • P1.5 ☐ ADC1.5 : A/D converter Input 13 • P1.6 ☐ ADC1.6 : A/D converter Input 14 • P1.7 ☐ ADC1.7 : A/D converter Input 15	P1.0 / T2 / ADC1.0 P1.1 / T2EX / ADC1.1 P1.2 / ADC1.2 P1.3 / ADC1.3 P1.4 / INT2 / ADC1.4 P1.5 / $\overline{\text{INT3}}$ / ADC1.5 P1.6 / INT4 / ADC1.6 P1.7 / $\overline{\text{INT5}}$ / ADC1.7

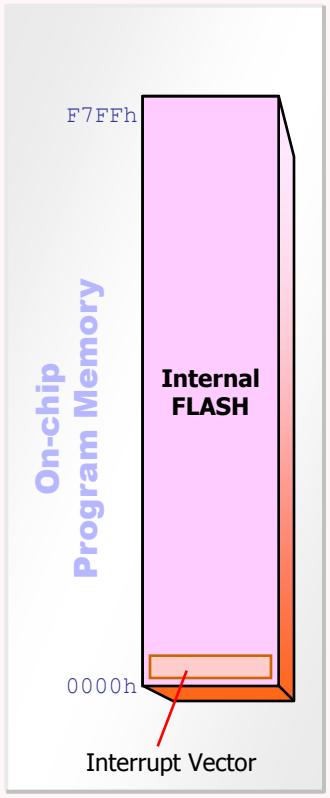
5. Pin Descriptions (Cont'd)

Symbol	Direction	Description	Share Pins
P2[7:0]	Input/Output	◆ An 8-bit Quasi-bidirectional or push-pull I/O port or ADC Input(3.3V). 5V Tolerant Input. ◆ Note that the output is fully driven (push-pull) when P2 drives the high byte of address to access external RAM or PCA0 drives output signals (C0EXn). • P2.0~P2.7 → AD8 ~ AD15 : High address output • P2.0~P2.5 → C0EX0 ~ C0EX5 for PCA0 • P2.6 → RXD1 : Serial Port 1 Output • P2.7 → TXD1 : Serial Port 1 Input • P2.0 ☐ ADC2.0 : A/D converter Input 16 • P2.1 ☐ ADC2.1 : A/D converter Input 17 • P2.2 ☐ ADC2.2 : A/D converter Input 18 • P2.3 ☐ ADC2.3 : A/D converter Input 19 • P2.4 ☐ ADC2.4 : A/D converter Input 20 • P2.5 ☐ ADC2.5 : A/D converter Input 21 • P2.6 ☐ ADC2.6 : A/D converter Input 22 • P2.7 ☐ ADC2.7 : A/D converter Input 23	P2.0 / AD8 / ADC2.0 / C0EX0 P2.1 / AD9 / ADC2.1 / C0EX1 P2.2 / AD10 / ADC2.2 / C0EX2 P2.3 / AD11 / ADC2.3 / C0EX3 P2.4 / AD12 / ADC2.4 / C0EX4 P2.5 / AD13 / ADC2.5 / C0EX5 P2.6 / AD14 / ADC2.6 / RXD1 P2.7 / AD15 / ADC2.7 / TXD1

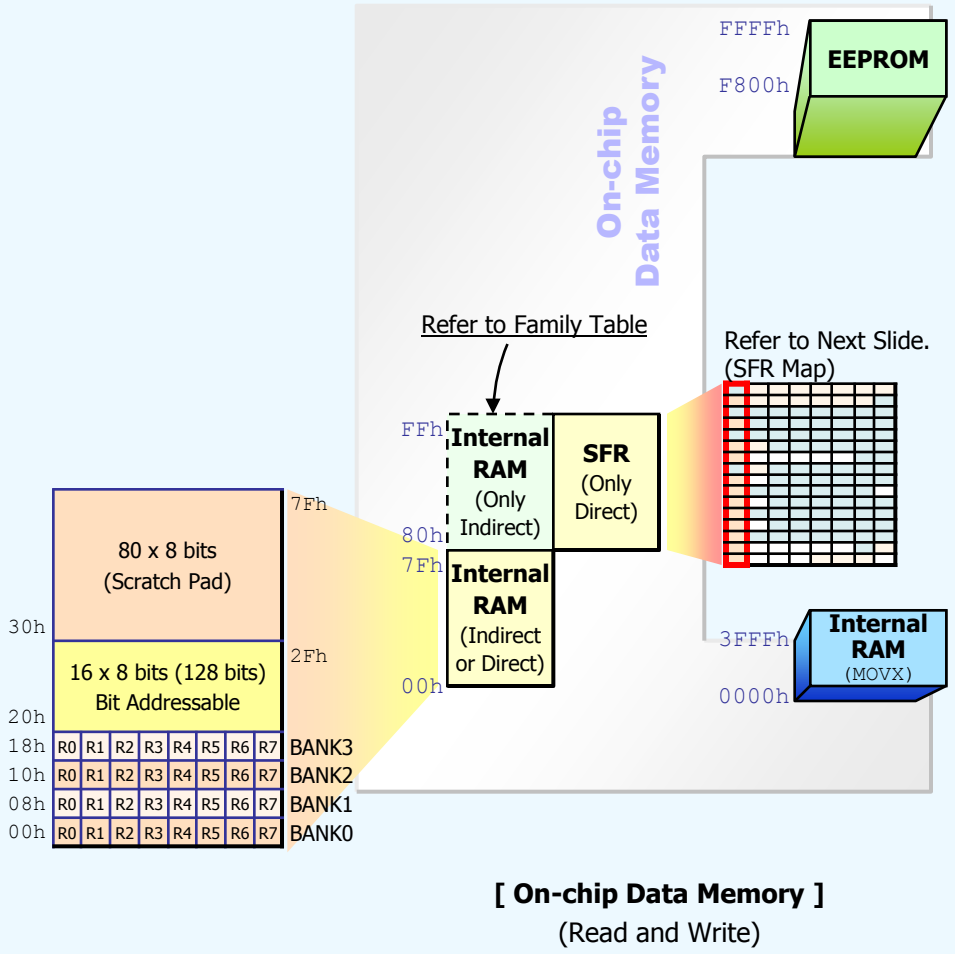
5. Pin Descriptions (Cont'd)

Symbol	Direction	Description	Share Pins
P3[7:0]	Input/Output	◆ An 8-bit Quasi-bidirectional or push-pull I/O port or ADC Input(3.3V). 5V Tolerant Input. • P3.0 → RXD : Serial Port 0 Input • P3.1 → TXD : Serial Port 0 Output • P3.2 → $\overline{\text{INT0}}$: External Interrupt Input 0 • P3.3 → $\overline{\text{INT1}}$: External Interrupt Input 1 • P3.4 → T0 : Timer 0 External Input • P3.5 → T1 : Timer 1 External Input • P3.6 → $\overline{\text{WR}}$: External Data Memory Writer Strobe • P3.7 → $\overline{\text{RD}}$: External Data Memory Read Strobe • P3.0 ☐ ADC3.0 : A/D converter Input 24 • P3.1 ☐ ADC3.1 : A/D converter Input 25 • P3.2 ☐ ADC3.2 : A/D converter Input 26 • P3.3 ☐ ADC3.3 : A/D converter Input 27 • P3.4 ☐ ADC3.4 : A/D converter Input 28 • P3.5 ☐ ADC3.5 : A/D converter Input 29 • P3.6 ☐ ADC3.6 : A/D converter Input 30 • P3.7 ☐ ADC3.7 : A/D converter Input 31	P3.0 / RXD / ADC3.0 P3.1 / $\overline{\text{TXD}}$ / ADC3.1 P3.2 / $\overline{\text{INT0}}$ / ADC3.2 P3.3 / $\overline{\text{INT1}}$ / ADC3.3 P3.4 / T0 / ADC3.4 P3.5 / T1 / ADC3.5 P3.6 / $\overline{\text{WR}}$ / ADC3.6 P3.7 / $\overline{\text{RD}}$ / ADC3.7

6.1. Memory Organization

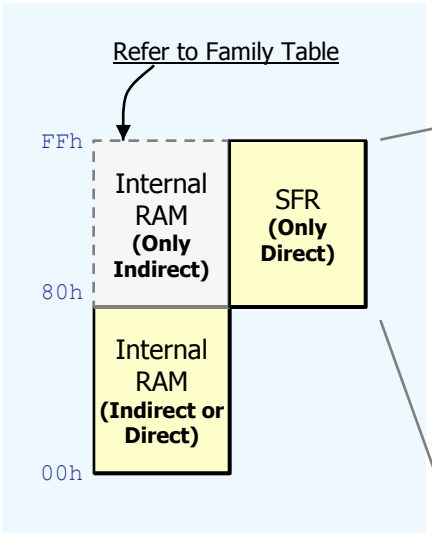


[On-chip Program Memory]
(Read/Write with IAP)



[On-chip Data Memory]
(Read and Write)

6.2. SFR (Special Function Register) Map



: Newly added SFR at MiDAS3.0 Family

: Reserved for future use.

Bit addressable

	0h/8h	1h/9h	2h/Ah	3h/Bh	4h/Ch	5h/Dh	6h/Eh	7h/Fh	
F8h	EIP	UINDX	UDATA	CLKSEL					FFh
F0h	B							FAEN	F7h
E8h	EIE	P3SEL	C1L	C1H	ADCENB0	ADCENB1	ADCENB2	ADCENB3	EFh
E0h	ACC	P2SEL	C1CAPM0	C1CAPM1	C1CAPM2	C1CAPM3	C1CAPM4	C1CAPM5	E7h
D8h	WDCON	P1SEL	C1CAP0H	C1CAP1H	C1CAP2H	C1CAP3H	C1CAP4H	C1CAP5H	DFh
D0h	PSW	P0SEL	C1CAP0L	C1CAP1L	C1CAP2L	C1CAP3L	C1CAP4L	C1CAP5L	D7h
C8h	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2	C1CON	C1MOD	CFh
C0h		PLLCON	PLLNR	PLLFR	PMR	STATUS	OSCICN	IOCFG	C7h
B8h	IP	SADEN	ITSEL	P0DIR	P1DIR	P2DIR	P3DIR	AUXAD	BFh
B0h	P3	SCON1	IT	P0TYP	P1TYP	P2TYP	P3TYP	IPH	B7h
A8h	IE	SADDR	SADDR1	SADEN1	C0CON	C0MOD	C0L	C0H	AFh
A0h	P2	SBUF1	C0CAPM0	C0CAPM1	C0CAPM2	C0CAPM3	C0CAPM4	C0CAPM5	A7h
98h	SCON	SBUF	C0CAP0H	C0CAP1H	C0CAP2H	C0CAP3H	C0CAP4H	C0CAP5H	9Fh
90h	P1	EXIF	C0CAP0L	C0CAP1L	C0CAP2L	C0CAP3L	C0CAP4L	C0CAP5L	97h
88h	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	RINGCON	8Fh
80h	P0	SP	DPL	DPH	ADCON	ADCSEL	ADCR	PCON	87h

(for 32-MLF)

6.2. SFR Brief Description

- 80C52 SFR Registers

Register	Name	Reset Value
ACC	Accumulator	00000000
B	B Register	00000000
PSW	Program Status Word	00000000
SP	Stack Pointer	00000111
DPTR	Data Pointer (2 bytes)	
DPL	Low byte	00000000
DPH	High byte	00000000
P0	Port 0	11111111
P1	Port 1	11111111
P2	Port 2	11111111
P3	Port 3	11111111
IP	Interrupt Priority Low	10000000
IPH	Interrupt Priority High	10000000
IE	Interrupt Enable Control	00000000
TCON	T/C 0/1 Control	00000000
TMOD	T/C 0/1 Mode Control	00000000
T2CON	T/C 2 Control	00000000
T2MOD	T/C 2 Mode Selection	******00
TH0	T/C 0 High byte	00000000
TL0	T/C 0 Low byte	00000000
TH1	T/C 1 High byte	00000000
TL1	T/C 1 Low byte	00000000
TH2	T/C 2 High byte	00000000
TL2	T/C 2 Low byte	00000000
RCAP2H	T/C 2 Capture Reg. High byte	00000000
RCAP2L	T/C 2 Capture Reg. Low byte	00000000
SCON	Serial Port Control of UART0	00000000
SBUF	Serial Data Buffer of UART0	00000000
SADEN	Slave Address Mask Enable of UART0	00000000
SADDR	Slave Address of UART0	00000000
PCON	Power Control	00*10000

- Newly added SFR Registers in MiDAS3.0 Family

Register	Name	Reset Value
P0SEL	Port 0 Pull-up Control	11111111
P1SEL	Port 1 Pull-up Control	00000000
P2SEL	Port 2 Pull-up Control	00000000
P3SEL	Port 3 Pull-up Control	00000000
P0DIR	Port 0 Input/Output Control	11111111
P1DIR	Port 1 Input/Output Control	11111111
P2DIR	Port 2 Input/Output Control	11111111
P3DIR	Port 3 Input/Output Control	11111111
P0TYPE	Port 0 Type Control	11111111
P1TYPE	Port 1 Type Control	11111111
P2TYPE	Port 2 Type Control	11111111
P3TYPE	Port 3 Type Control	11111111
SCON1	Serial Port Control of UART1	00000000
SBUF1	Serial Data Buffer of UART1	00000000
SADDR1	Slave Address of UART1	00000000
SADEN1	Slave Address Mask Enable of UART1	00000000
ADCON	ADC Control & ADC Result Low	0010**00
ADCR	ADC Result High	00000000
ADCSEL	ADC Clock & MUX Selection	00000000
ADCENB0	ADC Channel Enable Bar : ADC0.0~7	11111111
ADCENB1	ADC Channel Enable Bar : ADC1.0~7	11111111
ADCENB2	ADC Channel Enable Bar : ADC2.0~7	11111111
ADCENB3	ADC Channel Enable Bar : ADC3.0~7	11111111
EIP	Extended Interrupt Priority	00000000
EIE	Extended Interrupt Enable	00000000
AUXAD	High Address for MOVX with Ri	00000000
WDCON	Watchdog Timer & Power Status	*1010000
FAEN	IAP Routine Access Enable	*******0

*** : Don't touch bit.**

6.2. SFR Brief Description (Cont'd)

- Newly added SFR Registers in MiDAS3.0 Family (Cont'd)

Register	Name	Reset Value
PMR	Power Management	****0000
EXIF	External Interrupt Flag	00001001
CKCON	Clock Control	11000*00
STATUS	Crystal Status	***1****
OSCICN	Internal RING Oscillator Control	****0100
IOCFG	I/O Configuration	****0***
RINGCON	RING Control Register	01110000
CLKSEL	Internal Clock Selection	0**00110
PLLCON	PLL Control	0*011010
PLLNR	PLL NR Control	****1010
PLLFR	PLL FR Control	00000000
C0L	Low Byte of PCA0 Counter	00000000
C0H	High Byte of PCA0 Counter	00000000
C0CON	PCA0 Counter Control	00000000
C0MOD	PCA0 Counter Mode	00000000
C0CAPM0	Mode Control of PCA0 MODULE0	01000000
C0CAPM1	Mode Control of PCA0 MODULE1	01000000
C0CAPM2	Mode Control of PCA0 MODULE2	01000000
C0CAPM3	Mode Control of PCA0 MODULE3	01000000
C0CAPM4	Mode Control of PCA0 MODULE4	01000000
C0CAPM5	Mode Control of PCA0 MODULE5	01000000
C0CAP0L	Low Capture/Compare of PCA0 MODULE0	00000000
C0CAP1L	Low Capture/Compare of PCA0 MODULE1	00000000
C0CAP2L	Low Capture/Compare of PCA0 MODULE2	00000000
C0CAP3L	Low Capture/Compare of PCA0 MODULE3	00000000
C0CAP4L	Low Capture/Compare of PCA0 MODULE4	00000000
C0CAP5L	Low Capture/Compare of PCA0 MODULE5	00000000
C0CAP0H	High Capture/Compare of PCA0 MODULE0	00000000
C0CAP1H	High Capture/Compare of PCA0 MODULE1	00000000
C0CAP2H	High Capture/Compare of PCA0 MODULE2	00000000
C0CAP3H	High Capture/Compare of PCA0 MODULE3	00000000
C0CAP4H	High Capture/Compare of PCA0 MODULE4	00000000
C0CAP5H	High Capture/Compare of PCA0 MODULE5	00000000

Register	Name	Reset Value
C1L	Low Byte of PCA1 Counter	00000000
C1H	High Byte of PCA1 Counter	00000000
C1CON	PCA1 Counter Control	00000000
C1MOD	PCA1 Counter Mode	00*00000
C1CAPM0	Mode Control of PCA1 MODULE0	01000000
C1CAPM1	Mode Control of PCA1 MODULE1	01000000
C1CAPM2	Mode Control of PCA1 MODULE2	01000000
C1CAPM3	Mode Control of PCA1 MODULE3	01000000
C1CAPM4	Mode Control of PCA1 MODULE4	01000000
C1CAPM5	Mode Control of PCA1 MODULE5	01000000
C1CAP0L	Low Capture/Compare of PCA1 MODULE0	00000000
C1CAP1L	Low Capture/Compare of PCA1 MODULE1	00000000
C1CAP2L	Low Capture/Compare of PCA1 MODULE2	00000000
C1CAP3L	Low Capture/Compare of PCA1 MODULE3	00000000
C1CAP4L	Low Capture/Compare of PCA1 MODULE4	00000000
C1CAP5L	Low Capture/Compare of PCA1 MODULE5	00000000
C1CAP0H	High Capture/Compare of PCA1 MODULE0	00000000
C1CAP1H	High Capture/Compare of PCA1 MODULE1	00000000
C1CAP2H	High Capture/Compare of PCA1 MODULE2	00000000
C1CAP3H	High Capture/Compare of PCA1 MODULE3	00000000
C1CAP4H	High Capture/Compare of PCA1 MODULE4	00000000
C1CAP5H	High Capture/Compare of PCA1 MODULE5	00000000
UINDX	I2C Slave Access Index Register	***00000
UDATA	I2C Slave Access Data Register	01100111
IT	Interrupt Type Selection	00001111
ITSEL	Interrupt Polarity Selection	**010100

*** : Don't touch bit.**

6.3. Instruction Set Summary

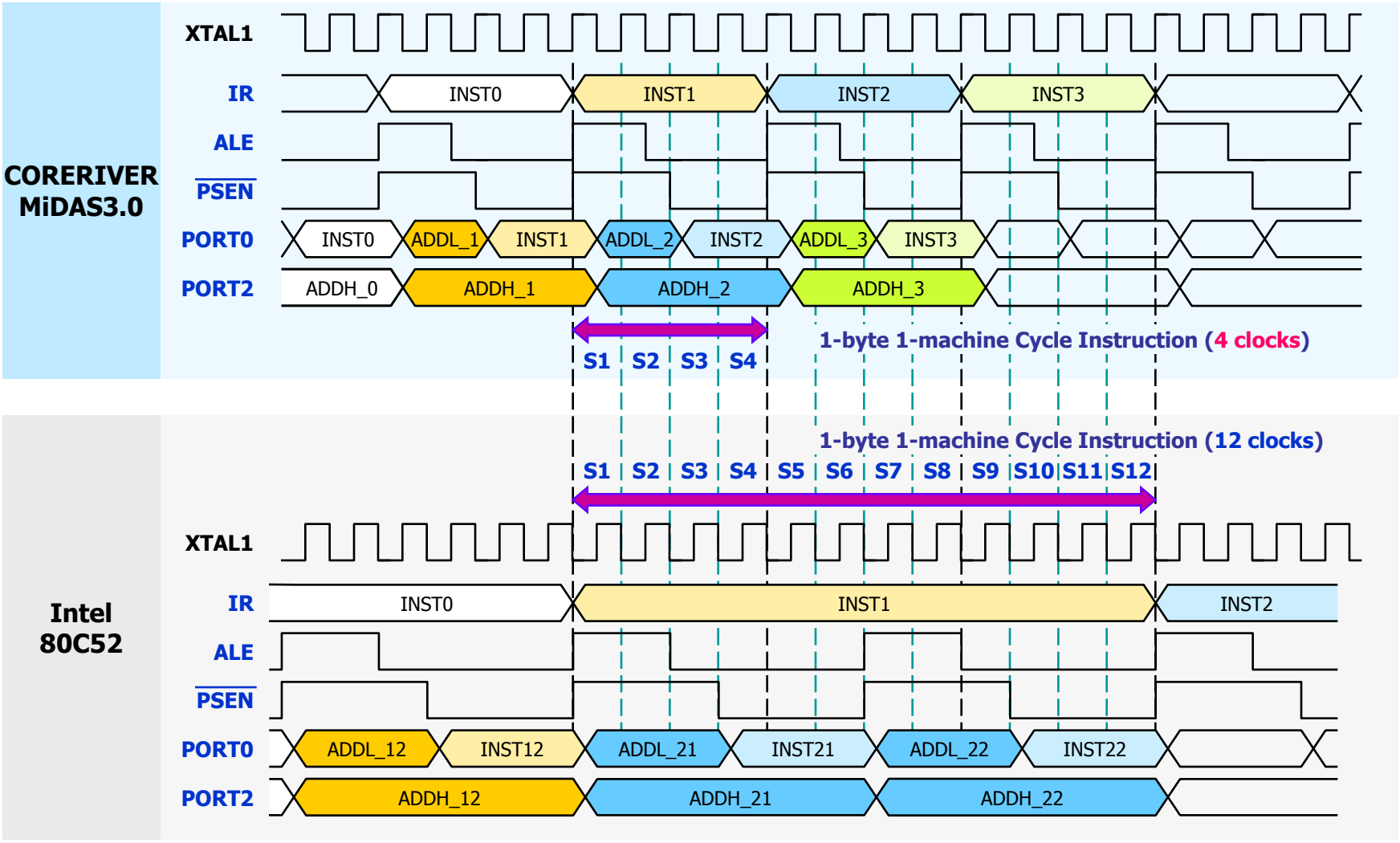
- Refer to Appendix A (Instruction Set) for more details.

Type	Instruction	Description
Arithmetic	ADD	Addition
	ADDC	Addition with Carry
	SUBB	Subtraction with Borrow
	INC	Increment
	DEC	Decrement
	MUL	Multiply
	DIV	Divide
	DA	Decimal Adjust
Logical	ANL	AND
	ORL	OR
	XRL	Exclusive OR
	CLR	Clear
	CPL	Complement
	RL	Rotate Left
	RLC	Rotate Left with Carry
	RR	Rotate Right
	RRC	Rotate Right with Carry
	SWAP	Swap Nibbles
Data Transfer	MOV	Move Data
	MOVC	Move Code
	MOVX	Move Data to Ext. RAM
	PUSH	PUSH
	POP	POP
	XCH	Exchange
	XCHD	Exchange Low-digit

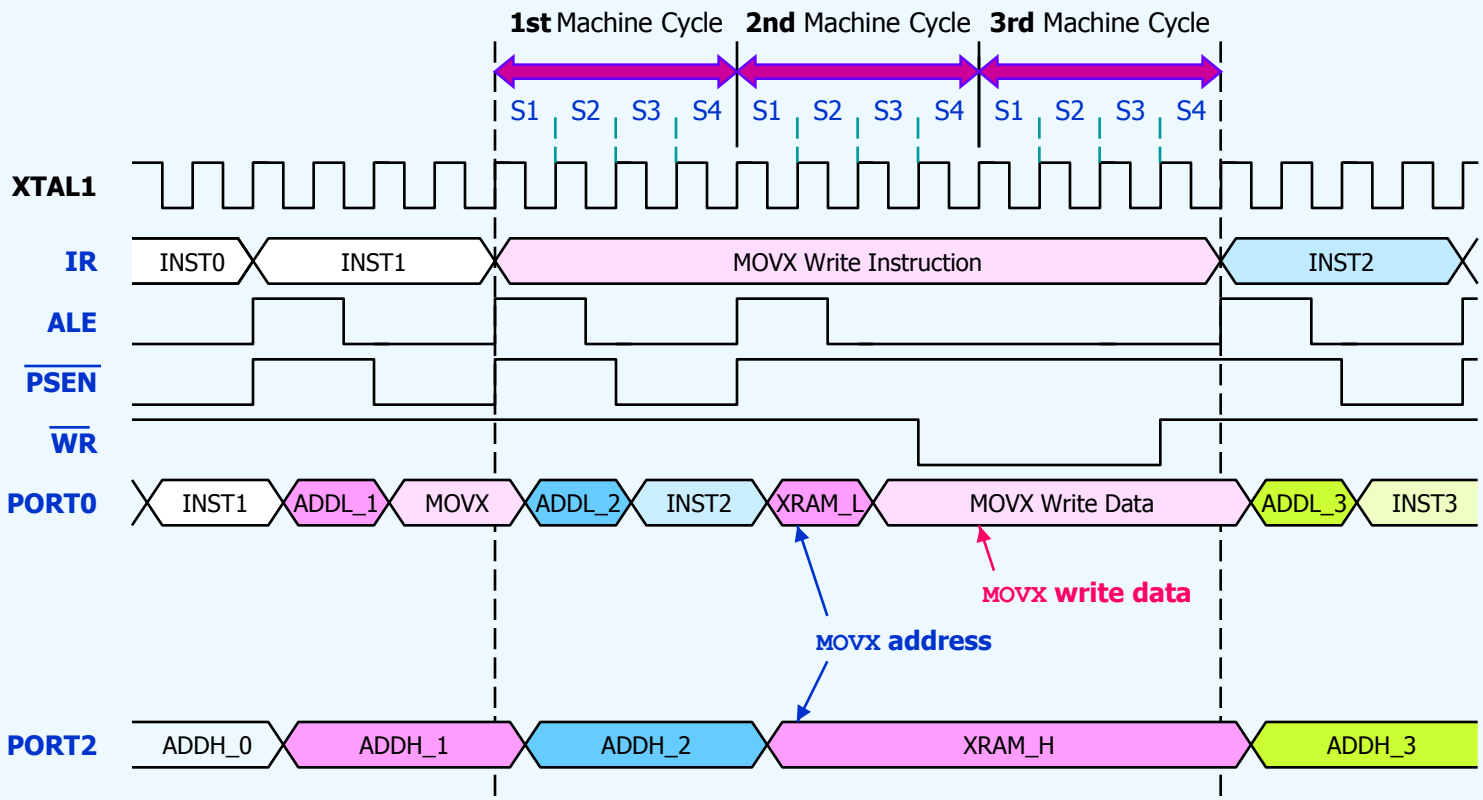
Type	Instruction	Description
Boolean	CLR	Clear bit
	SETB	Set bit
	CPL	Complement bit
	ANL	AND bit
	ORL	OR bit
	MOV	Move bit
	JC	Jump if Carry is set
	JNC	Jump if Carry is not set
	JB	Jump if bit is set
	JNB	Jump if bit is not set
	JBC	Jump if bit is set & clear
Branch	ACALL	Absolute Call
	LCALL	Long Call
	RET	Return from Subroutine
	RETI	Return from Interrupt
	AJMP	Absolute Jump
	LJMP	Long Jump
	SJMP	Short Jump
	JMP	Jump with DPTR
	JZ	Jump if ACC is zero
	JNZ	Jump if ACC is not zero
	CJNE	Compare and Jump if not equal
	DJNZ	Decrement and Jump if not zero
	NOP	No Operation

6.4. CPU Timing

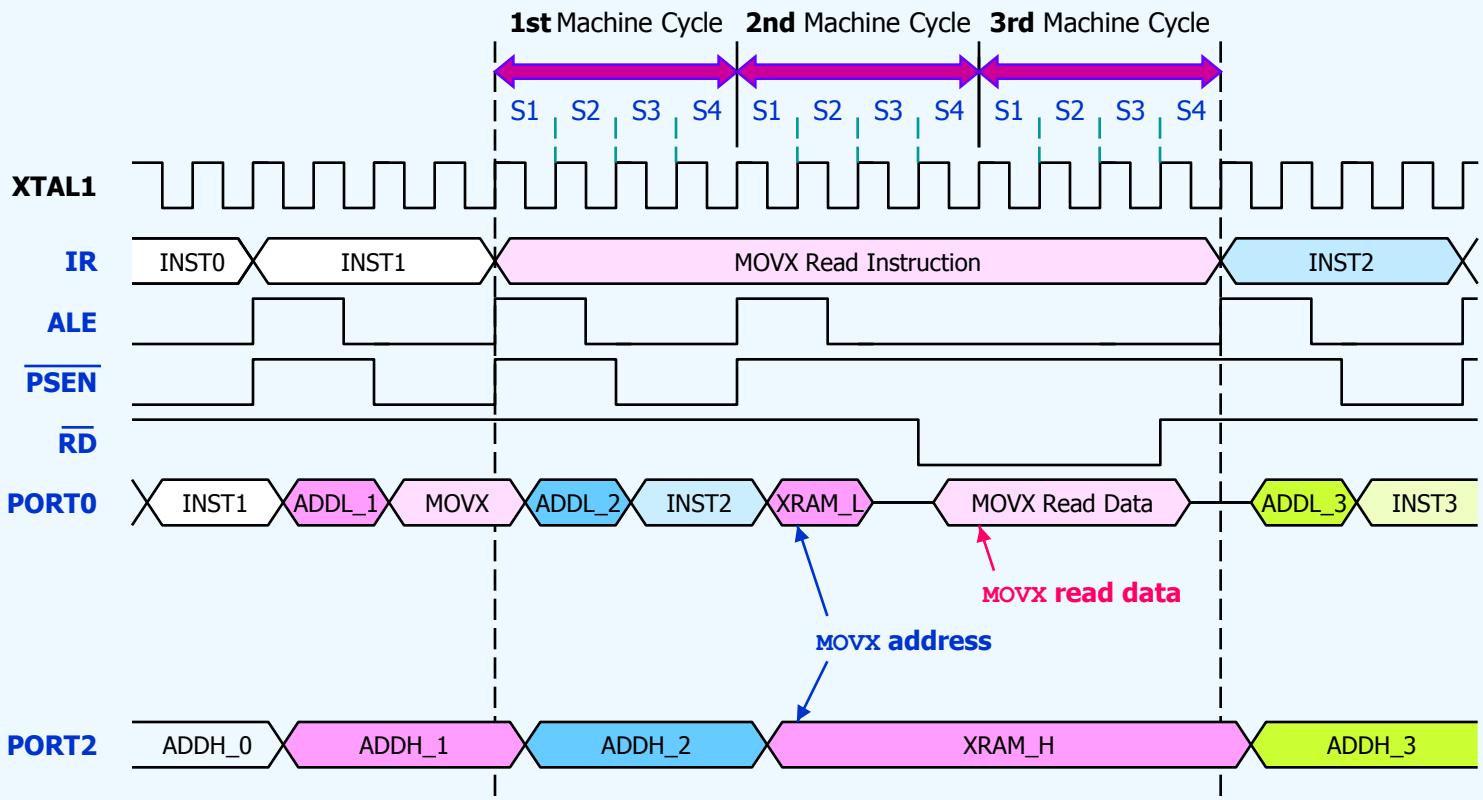
- Comparative timing of the MiDAS3.0 family and Intel 80C52



6.4. CPU Timing : MOVX Write Timing



6.4. CPU Timing : MOVX Read Timing



6.4. CPU Timing : Instruction Execution Time

- The Fastest instruction execution in the world

Instruction	**MiDAS3.0 (CORERIVER)**	W77C32 (Winbond)	DS80C320 (Maxim)	87C52 (Intel)
`MUL AB` `DIV AB`	**12 clocks**	20 clocks	20 clocks	48 clocks
`MOVC A, @A+PC` `MOVC A, @A+DPTR`	**8 clocks**	8 clocks	12 clocks	24 clocks
`JMP @A+DPTR`	**8 clocks**	8 clocks	12 clocks	24 clocks
`RET` `RETI`	**8 clocks**	8 clocks	16 clocks	24 clocks
`INC DPTR` `DEC DPTR`	**4 clocks** **4 clocks**	8 clocks 8 clocks	12 clocks Not exist	24 clocks Not exist
`Others`	**Same**	Same	Same	-

6.5. I/O Ports : PORT0[7:0]

- 5V tolerant input, open-drain (compatible with Intel 8052) or push-pull output, ADC input.
- Read-Modify-Write instructions do not read port pin but read SFR register.
  - ✓`ANL / OPL / XRL / JBC / CPL / INC / DEC / DJNZ / MOV PX.Y, C / CLR PX.Y / SETB PX.Y`
- An available alternative input functions when the corresponding SFR bit is "1" (PCA0 and PCA1 input pins).
  - ✓ C1EX0(P0.0), C1EX1(P0.1), C1EX2(P0.2), C1EX3(P0.3), C1EX4(P0.4), C1EX5(P0.5), ECI1(P0.6), ECI0(P0.7)

✓ **P0TYPE** (B3h) : Port 0 Type Control Register

P0TYPE.7	P0TYPE.6	P0TYPE.5	P0TYPE.4	P0TYPE.3	P0TYPE.2	P0TYPE.1	P0TYPE.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- 0 = Push-pull Output / 1 = Open-drain Output (Default)

✓ **P0DIR** (BBh) : Port 0 Input/Output Control Register

P0DIR.7	P0DIR.6	P0DIR.5	P0DIR.4	P0DIR.3	P0DIR.2	P0DIR.1	P0DIR.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- 0 = Output / 1 = Input (Default)

✓ **P0SEL** (D1h) : Port 0 Pull-up Control Register

P0SEL.7	P0SEL.6	P0SEL.5	P0SEL.4	P0SEL.3	P0SEL.2	P0SEL.1	P0SEL.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- 0 = Pull-up resistor ON
- 1 = Pull-up resistor OFF when ADC_EN (ADCON[7]) = 1 (Default)

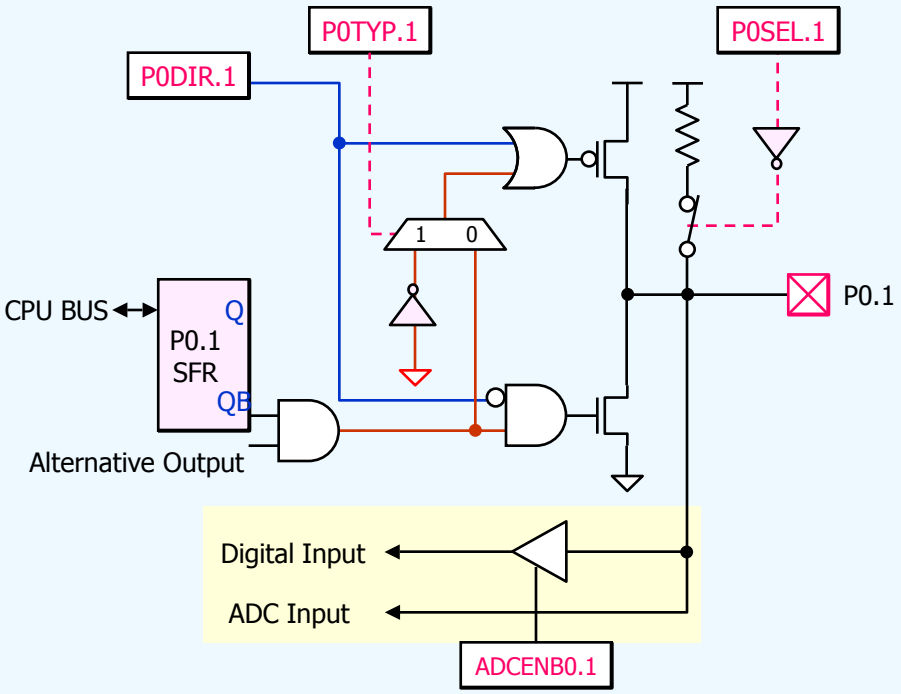
✓ **ADCENB0** (ECh) : ADC Channel Enable Bar Register (P0 port)

ADCENB0.7	ADCENB0.6	ADCENB0.5	ADCENB0.4	ADCENB0.3	ADCENB0.2	ADCENB0.1	ADCENB0.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- 0 = ADC0 channel ON / 1 = ADC0 channel OFF (Default)

✓ **P0** (80h) : Port 0 Register

P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)



6.5. I/O Ports : PORT1[7:0]

- 5V tolerant input, quasi-bidirectional (compatible with Intel 8052) or push-pull port, ADC input.
- Read-Modify-Write instructions do not read port pin but read SFR register.
  - ✓ANL / OPL / XRL / JBC / CPL / INC / DEC / DJNZ / MOV PX.Y, C / CLR PX.Y / SETB PX.Y
- An available alternative input functions when the corresponding SFR bit is "1".
  - ✓ P1.1 = T2EX / P1.4 = INT2 / P1.5 = /INT3 / P1.6 = INT4 / P1.7 = /INT5

✓ **P1TYPE** (B4h) : Port 1 Type Control Register

P1TYPE.7	P1TYPE.6	P1TYPE.5	P1TYPE.4	P1TYPE.3	P1TYPE.2	P1TYPE.1	P1TYPE.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- 0 = Push-pull Output / 1 = quasi-bidirectional Output (Default)

✓ **P1DIR** (BCh) : Port 1 Input/Output Control Register

P1DIR.7	P1DIR.6	P1DIR.5	P1DIR.4	P1DIR.3	P1DIR.2	P1DIR.1	P1DIR.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- 0 = Output / 1 = Input (Default)

✓ **P1SEL** (D9h) : Port 1 Pull-up Control Register

P1SEL.7	P1SEL.6	P1SEL.5	P1SEL.4	P1SEL.3	P1SEL.2	P1SEL.1	P1SEL.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- 0 = Pull-up resistor ON (Default)
- 1 = Pull-up resistor OFF when ADC_EN (ADCON[7]) = 1

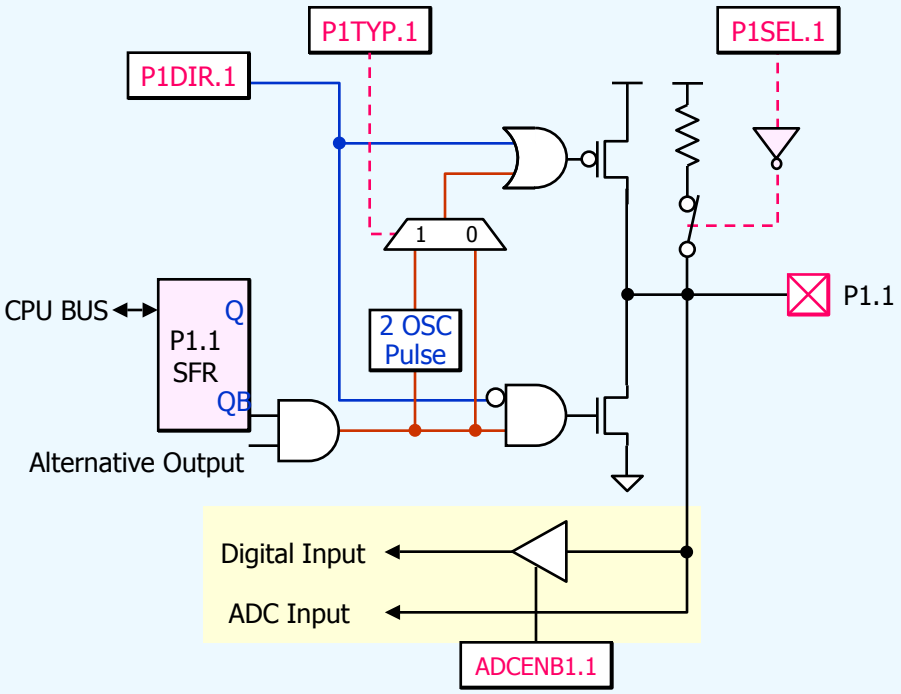
✓ **ADCENB1** (EDh) : ADC Channel Enable Bar Register (P1 port)

ADCENB1.7	ADCENB1.6	ADCENB1.5	ADCENB1.4	ADCENB1.3	ADCENB1.2	ADCENB1.1	ADCENB1.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- 0 = ADC channel ON / 1 = ADC channel OFF (Default)

✓ **P1** (90h) : Port 1 Register

P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)



6.5. I/O Ports : PORT2[7:0]

- 5V tolerant input, quasi-bidirectional (compatible with Intel 8052) or push-pull port, ADC input.
- Read-Modify-Write instructions do not read port pin but read SFR register.
  - ✓`ANL / OPL / XRL / JBC / CPL / INC / DEC / DJNZ / MOV PX.Y, C / CLR PX.Y / SETB PX.Y`
- An available alternative input function when the corresponding SFR bit is "1".
  - ✓ PCA0 inputs : C0EX0(P2.0), C0EX1(P2.1), C0EX2(P2.2), C0EX3(P2.3), C0EX4(P2.4), C0EX5(P2.5)
  - ✓ UART1 : RXD1(P2.6), TXD1(P2.7)

✓ **P2TYPE** (B5h) : Port 2 Type Control Register

P2TYPE.7	P2TYPE.6	P2TYPE.5	P2TYPE.4	P2TYPE.3	P2TYPE.2	P2TYPE.1	P2TYPE.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- 0 = Push-pull Output / 1 = quasi-bidirectional Output (Default)

✓ **P2DIR** (BDh) : Port 2 Input/Output Control Register

P2DIR.7	P2DIR.6	P2DIR.5	P2DIR.4	P2DIR.3	P2DIR.2	P2DIR.1	P2DIR.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- 0 = Output / 1 = Input (Default)

✓ **P2SEL** (E1h) : Port 2 Pull-up Control Register

P2SEL.7	P2SEL.6	P2SEL.5	P2SEL.4	P2SEL.3	P2SEL.2	P2SEL.1	P2SEL.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- 0 = Pull-up resistor ON (Default)
- 1 = Pull-up resistor OFF when ADC_EN (ADCON[7]) = 1

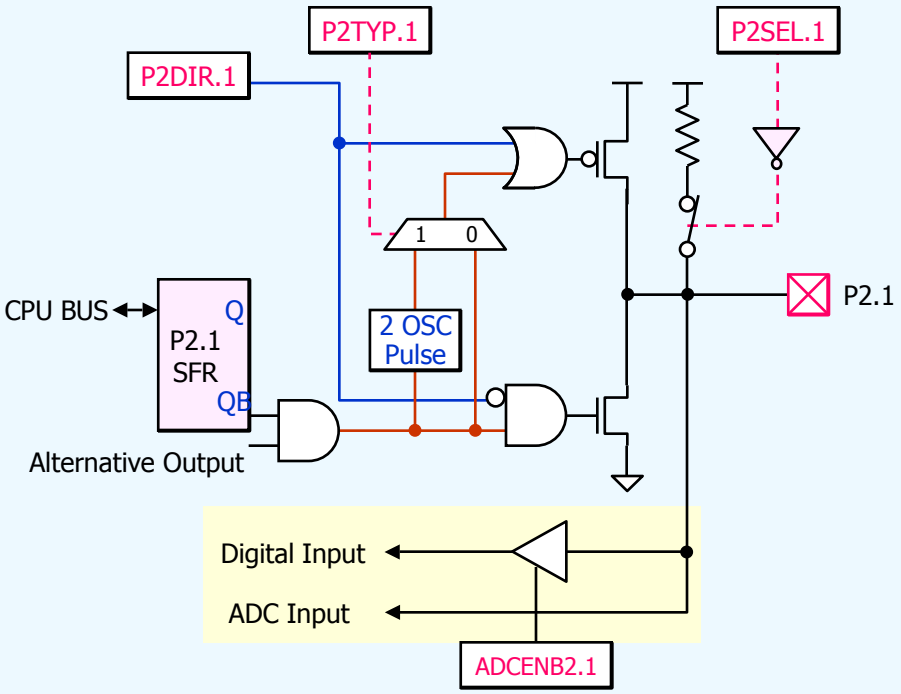
✓ **ADCENB2** (EEh) : ADC Channel Enable Bar Register (P2 port)

ADCENB2.7	ADCENB2.6	ADCENB2.5	ADCENB2.4	ADCENB2.3	ADCENB2.2	ADCENB2.1	ADCENB2.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- 0 = ADC channel ON / 1 = ADC channel OFF (Default)

✓ **P2** (A0h) : Port 2 Register

P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)



6.5. I/O Ports : PORT3[7:0]

- 5V tolerant input, quasi-bidirectional (compatible with Intel 8052) or push-pull port, ADC input.
- Read-Modify-Write instructions do not read port pin but read SFR register.
  - ✓ANL / OPL / XRL / JBC / CPL / INC / DEC / DJNZ / MOV PX.Y, C / CLR PX.Y / SETB PX.Y
- The available alternative input function when the corresponding SFR bit is "1".
  - ✓ P3.0 = RXD / P3.1 = TXD / P3.4 = T0 / P3.5 = T1

✓ **P3TYPE** (B6h) : Port 3 Type Control Register

P3TYPE.7	P3TYPE.6	P3TYPE.5	P3TYPE.4	P3TYPE.3	P3TYPE.2	P3TYPE.1	P3TYPE.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- 0 = Push-pull Output / 1 = quasi-bidirectional Output (Default)

✓ **P3DIR** (BEh) : Port 3 Input/Output Control Register

P3DIR.7	P3DIR.6	P3DIR.5	P3DIR.4	P3DIR.3	P3DIR.2	P3DIR.1	P3DIR.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- 0 = Output / 1 = Input (Default)

✓ **P3SEL** (E9h) : Port 3 Pull-up Control Register

P3SEL.7	P3SEL.6	P3SEL.5	P3SEL.4	P3SEL.3	P3SEL.2	P3SEL.1	P3SEL.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- 0 = Pull-up resistor ON (Default)
- 1 = Pull-up resistor OFF when ADC_EN (ADCON[7]) = 1

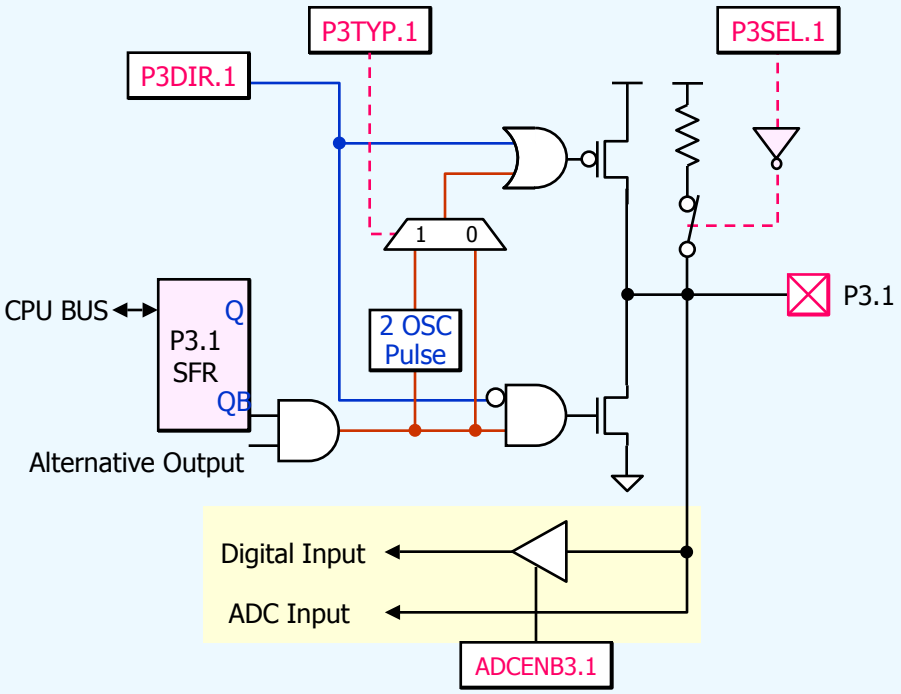
✓ **ADCENB3** (EFh) : ADC Channel Enable Bar Register (P3 port)

ADCENB3.7	ADCENB3.6	ADCENB3.5	ADCENB3.4	ADCENB3.3	ADCENB3.2	ADCENB3.1	ADCENB3.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- 0 = ADC channel ON / 1 = ADC channel OFF (Default)

✓ **P3** (A0h) : Port 3 Register

P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)



6.5. I/O Ports : PORT Configuration

- MiDAS3.0 family provides a dedicated address register for `movx` instructions using Ri.
  - ✓ If configured so, the AUXAD register provides the high byte of address for `movx` instruction instead of P2 SFR.
  - ✓ Then, the PORT2 can be used exclusively as general purpose I/O or PCA I/O on the condition that an user accesses only the internal RAM (0000h ~ 3FFFh).
  - ✓ To enable this feature, set ENAUX bit (IOCFG.3) to 1.

✓ **AUXAD** (BFh) : High Address Register for MOVX with Ri

AUXAD.7	AUXAD.6	AUXAD.5	AUXAD.4	AUXAD.3	AUXAD.2	AUXAD.1	AUXAD.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- If ENAUX bit (IOCFG.3) is set, "MOVX A, @Ri" and "MOVX @Ri, A" instructions refer to AUXAD instead of P2 register for high address.

✓ **IOCFG** (C7h) : I/O Configuration Register

-	-	-	-	ENAUX	-	-	-
				R/W(0)			

- ENAUX : Select AUXAD for MOVX with Ri.
  1 = AUXAD register serves high address for MOVX with Ri.
  0 = P2 register serves high address for MOVX with Ri.

6.6. WDT (Watch Dog Timer)

- Detects software upset due to external noise or other causes
- Allows an automatic recovery using WDT interrupt
- If enabled,
  WDT interrupt or WDT reset makes MCU wake up from stop mode.
- Watchdog time-out counter mode
  - ✓CKCON[7:6], CLKSEL[3] : WD1, WD0, WDEM
- **Notice, Before WDT Reset , PLL Clock must be Power Down status running X-TAL or Ring Clock**

WDEM	WD1	WD0	Interrupt Time-out (@25MHz)		Reset Time-out (@25MHz)	
0	0	0	2^{17} clocks	5.24 ms	2^{17} + 512 clocks	5.26 ms
	0	1	2^{20} clocks	41.94 ms	2^{20} + 512 clocks	41.96 ms
	1	0	2^{23} clocks	335.53 ms	2^{23} + 512 clocks	335.56 ms
	1	1	2^{26} clocks	2,684.35 ms	2^{26} + 512 clocks	2,684.38 ms

✓ **CLKSEL** (FBh) : Clock Selection

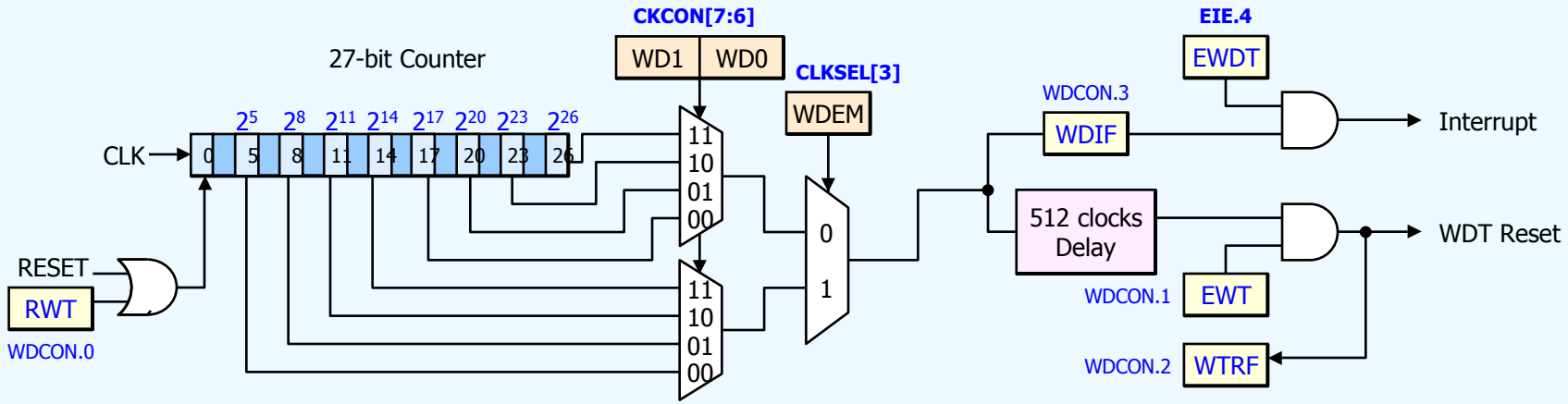
-	-	-	XT/HF	WDEM	XR/PL	RG/PL	OSC32EB
-	-	-	R/W(0)	R/W(1)	R/W(1)	R/W(0)	R/W(0)

- WDEM : Watchdog Timer extension mode

✓ **WDCON** (D8h) : Watchdog Timer & Power Status Register

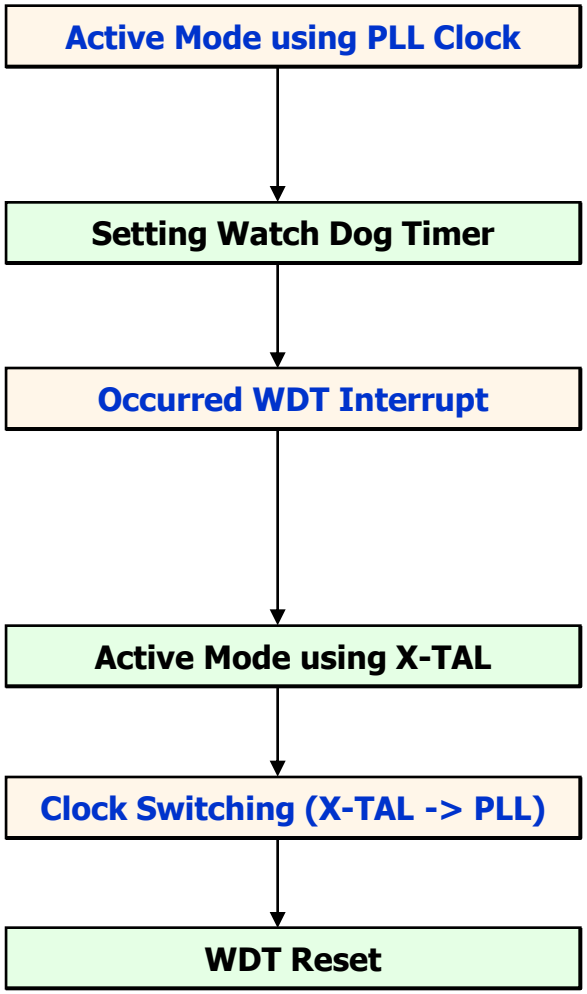
-	POR	EPFI	PFI	WDIF	WTRF	EWT	RWT
	R/W(1)	R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- POR : Power-on Reset Flag
- EPFI : Enable Power-fail Interrupt
- PFI : Power-Fail interrupt Flag
- WDIF : Watchdog Timer Interrupt Flag
- WTRF : Watchdog Timer Reset Flag
- EWT : Watchdog Timer Reset Enable
- RWT : Restart Watchdog Timer



6.6. WDT (Watch Dog Timer) - Example

- Example : How to use Watch Dog Timer When PLL Clock used




```
PLLNR = 0x01;                 // RDIV=1,ODIV=0
PLLFR = 0x08;                 // 08 : 80 Mhz @ 22.1184 Mhz
PLLCON &= 0xFD;               // PLL ON
while(!(PLLCON & 0x80));      // PLL Lock Check
CLKSEL &= 0xFB;               // Clock Switch : XTAL -> PLL Clock
```

```
CKCON = 0xBF                  // 2^23 Clocks
RWT = 1;                      // Restart Watch Dog Timer
EWDT = 1;                     // Enable Watch Dog Timer Interrupt
EWT = 1;                      // Watch Dog Timer Reset Enable
```

```
void wdt_int() interrupt WDT_VECTOR
{
/* Active Mode using X-TAL */
  EXIF |= 0x08;               // X-TAL Clock Select
  CLKSEL |= 0x06;             // XTAL/Ring Clock Select
                              // 4MHz ring clock
  PLLCON = 0x1A;              // PLL Clock Power Down (Kill)
```

```
 while(!(STATUS & 0x10));     // Stable X-TAL Clock Check
  EXIF = 0x08;                // X-TAL Clock Select
```

```
  wdt_flag = 0;
  WDIF = 0;                   // WDT flag clear
```

```
  /* Reset by Watch Dog Timer  */
}
```

6.7. Timer/Counter : Timer 0/1

- Compatible with traditional 80C52 Timer/Counter function
- Time base is selectable by S/W : 4 clocks or 12 clocks

Mode / Timer	Mode 0 (M1,M0=00)	Mode 1 (M1,M0=01)	Mode 2 (M1,M0=10)	Mode 3 (M1,M0=11)
Timer0	13-bit T/C	16-bit T/C	8-bit T/C with automatic reload (TL0 ← TH0)	8-bit T/C (TL0) ➔ Timer0 interrupt 8-bit T/C (TH0) ➔ Timer1 interrupt
Timer1	13-bit T/C	16-bit T/C	8-bit T/C with automatic reload (TL1 ← TH1)	Halt

✓ **TMOD** (89h) : Timer 0/1 Mode Control Register

GATE	C/T	M1	M0	GATE	C/T	M1	M0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- Timer[1]: GATE[7], C/T[6], M1:M0[5:4]
- Timer[0]: GATE[3], C/T[2], M1:M0[1:0]
- GATE : When TRx (in TCON) is set and GATE=1, Timer x will run only while INTx pin is high (hardware control). When GATE=0, Timer x will run only while TRx=1 (software control).
- C/T : Counter or Timer Selector. Cleared for Timer operation (input from internal system clock). Set for Counter operation (input from Tx input pin).
- M1, M0 : Mode Selector bits
  [0 0] Mode 0. 13-bit T/C.
  [0 1] Mode 1. 16-bit T/C.
  [1 0] Mode 2. 8-bit Auto-Reload T/C.
  [1 1] Mode 3.
  (Timer 1) stopped,
  (Timer 0) TL0: 8-bit T/C controlled by the Timer 0 control bits.
  TH0: 8-bit T/C controlled by the Timer 1 control bits.

✓ **CKCON** (8Eh) : Clock Control Register

WD1	WD0	T2M	T1M	T0M	-	U1T2DIS	U0T2DIS
R/W(1)	R/W(1)	R/W(0)	R/W(0)	R/W(0)		R/W(0)	R/W(0)

- T1M : Timer 1 Clock Time-base Selection
  T1M=1, Time-base is 4 clocks not 12 clocks.
- T0M : Timer 0 Clock Time-base Selection
  T0M=1, Time-base is 4 clocks not 12 clocks.

✓ **TCON** (88h) : Timer 0/1 Control Register

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- TF1 : Timer 1 Overflow Flag
- TR1 : Timer 1 Run Enable
- TF0 : Timer 0 Overflow Flag
- TR0 : Timer 0 Run Enable
- IE1 : External Interrupt 1 Flag
- IT1 : External Interrupt 1 Type Select
  Edge Detect (IT1=1). Level Detect (IT1=0)
- IE0 : External Interrupt 0 Flag
- IT0 : External Interrupt 0 Type Select
  Edge Detect (IT0=1). Level Detect (IT0=0)

✓ **TL0** (8Ah) : Timer 0 Low Byte Register

TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

✓ **TH0** (8Ch) : Timer 0 High Byte Register

TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

✓ **TL1** (8Bh) : Timer 1 Low Byte Register

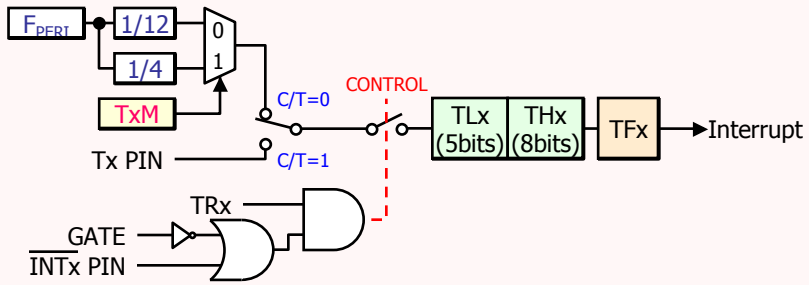
TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

✓ **TH1** (8Dh) : Timer 1 High Byte Register

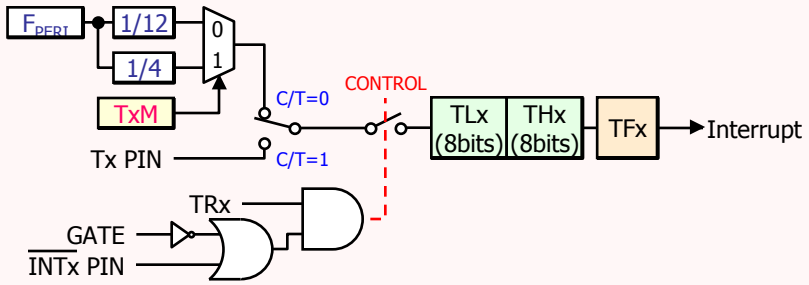
TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

6.7. Timer/Counter : Timer 0/1 Mode Description

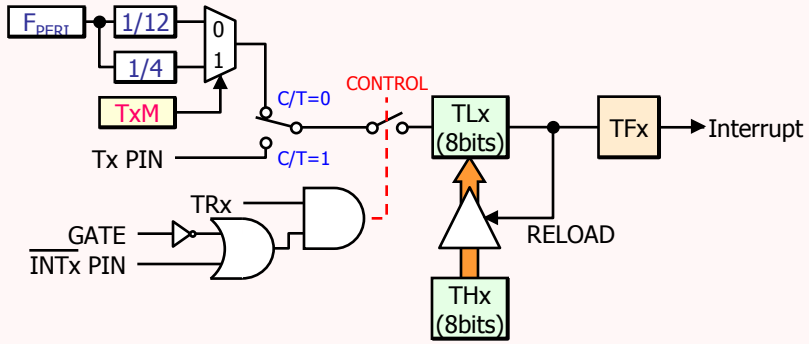
F_{PERI} : Peripheral Clock



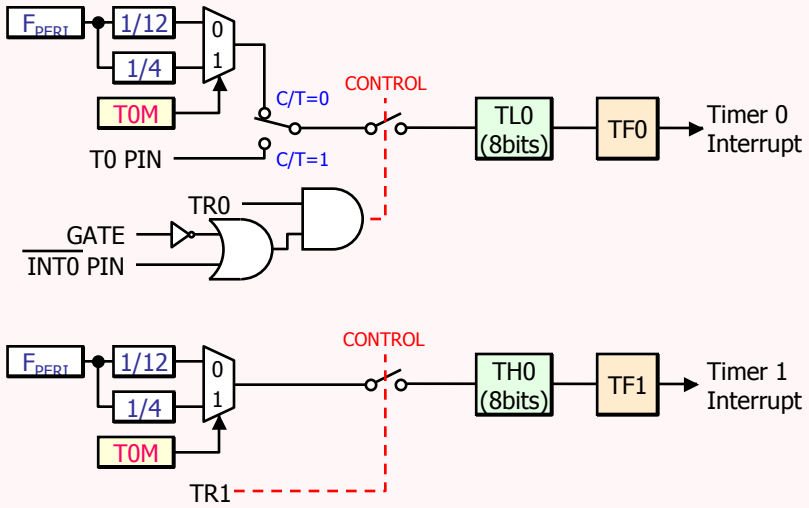
[Mode 0]



[Mode 1]



[Mode 2]



[Mode 3(Timer 0 only)]

6.7. Timer/Counter : Timer 2

- Compatible with traditional 80C52 Timer/Counter 2 function
- Up or down counting selectable by a software
- Time base is selectable by S/W : 4 clocks or 12 clocks

1. 16-bit Auto-reload [RCLK+TCLK=0, CP/RL2=0, T2OE=0]	16-bit Timer/Counter With Automatic Reload (TH2, TL2 ← RCAP2H, RCAP2L)
2. 16-bit Capture [RCLK+TCLK=0, CP/RL2=1, T2OE=0]	16-bit Timer/Counter with Capture (RCAP2H, RCAP2L ← TH2, TL2)
3. Baud Rate Generator [RCLK+TCLK=1, CP/RL2=X, T2OE=X]	Baud Rate Generation * Timer 2 Interrupt Disable
4. Programmable Clock Out [RCLK+TCLK=X, CP/RL2=0, T2OE=1]	Clock-out on P1.0

✓ **T2CON** (C8h) : Timer 2 Control Register

TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- TF2 : Timer 2 Overflow Flag
- EXF2 : Timer 2 External Flag
- RCLK : Receive Clock Flag
- TCLK : Transmit Clock Flag
- EXEN2 : Timer 2 External Enable Flag
- TR2 : Timer 2 Run Enable
- C/T2 : Timer or Counter Selection. If C/T2=0, Timer Operation.
- CP/RL2 : Capture/Reload Flag.
  CP/RL2=0, Reload. (TH2,TL2) ← (RCAP2H, RCAP2L)
  CP/RL2=1, Capture. (RCAP2H, RCAP2L) ← (TH2,TL2)

✓ **CKCON** (8Eh) : Clock Control Register

WD1	WD0	T2M	T1M	T0M	-	U1T2DIS	U0T2DIS
R/W(1)	R/W(1)	R/W(0)	R/W(0)	R/W(0)		R/W(0)	R/W(0)

- T2M : Timer 2 Clock Time-base Selection
  T2M=1, Time-base is 4 clocks not 12 clocks.

✓ **T2MOD** (C9h) : Timer 2 Mode Register

-	-	-	-	-	-	T2OE	DCEN
						R/W(0)	R/W(0)

- T2OE : Timer 2 Clock Output to P1.0
- DCEN : Timer 2 Down Count Enable

✓ **TL2** (CCh) : Timer 2 Low Byte Register

TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

✓ **TH2** (CDh) : Timer 2 High Byte Register

TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

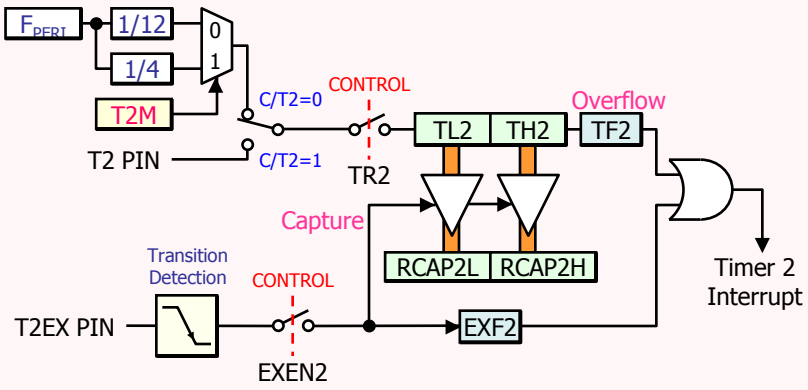
✓ **RCAP2L** (CAh) : Timer 2 Capture/Reload Low Byte Register

RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

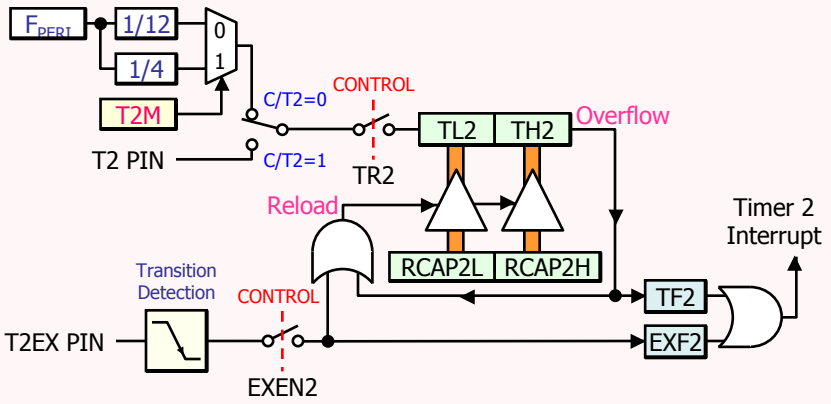
✓ **RCAP2H** (CBh) : Timer 2 Capture/Reload High Byte Register

RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

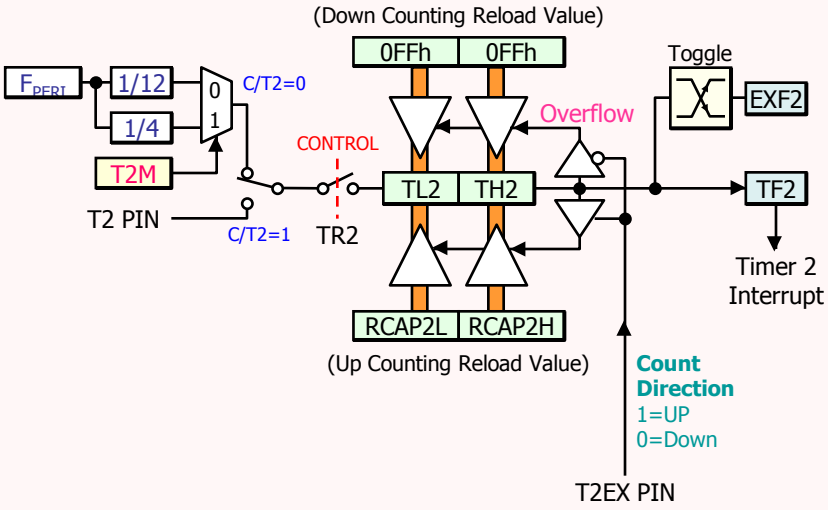
6.7. Timer/Counter : Timer 2 Mode Description



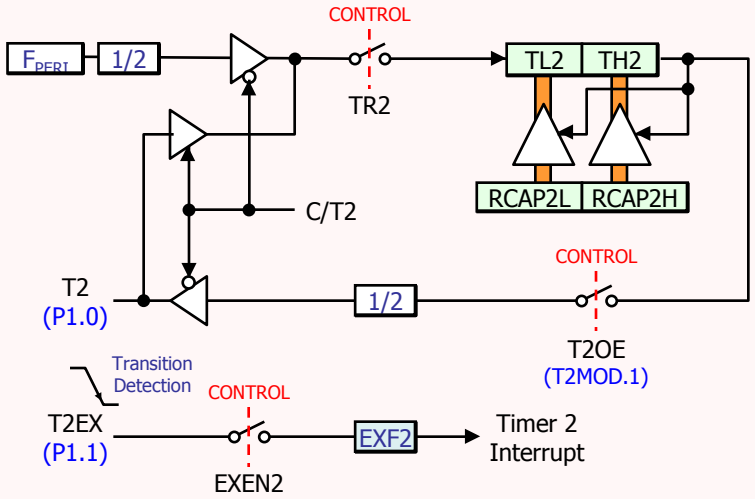
[Capture Mode]



[Auto Reload Mode (DCEN=0)]

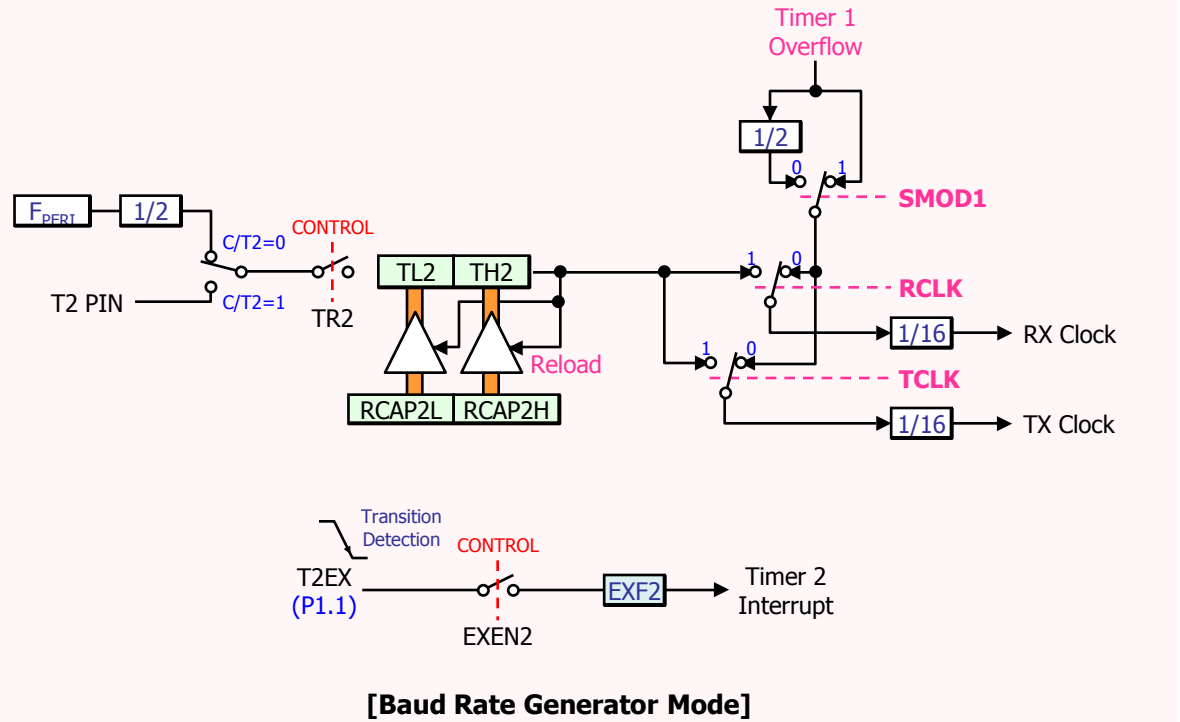


[Auto Reload Mode (DCEN=1)]



[Clock-Out Mode]

6.7. Timer/Counter : Timer 2 Mode Description



[Baud Rate Generator Mode]

6.8. UART (UART0/UART1)

- Function-level compatible with traditional 80C52 UART.
- Automatic address recognition :
  - ✓ Multi processor communication.
- The SFR name for UART0 is the same as the legacy UART.

	Data Size		Baud Rate
Mode 0	8 bits	8 data bits	1/4 x Oscillator Clock
Mode 1	10 bits	Start bit(0) 8 data bit Stop bit(1)	1/32 x Timer 1 Overflow (SMOD1=0) 1/16 x Timer 1 Overflow (SMOD1=1) 1/16 x Timer 2 Overflow Rate
Mode 2	11 bits	Start bit(0) 8 data bit Programmable bit Stop bit(1)	1/32 x Oscillator Clock (SMOD1=0) 1/16 x Oscillator Clock (SMOD1=1)
Mode 3	11 bits	Start bit(0) 8 data bit Programmable bit Stop bit(1)	1/32 x Timer 1 Overflow (SMOD1=0) 1/16 x Timer 1 Overflow (SMOD1=1) 1/16 x Timer 2 Overflow Rate

✓ **Timer 1 Overflow varies with the CKCON register value**

➔ 12 clocks time-base or 4 clocks time-base.

✓ **PCON** (87h) : Power Control Register

SMOD1	SDMO0	-	POF	GF1	GF0	PD	IDL
R/W(0)	R(0)		R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- SMOD1 : Timer 1 baud rate double in UART mode 1, 2, and 3
- SMOD0 : Enable SM0 access. Don't modify this bit.

✓ **SCON** (98h) : Serial Port Control Register for UART0

SM0	SM1	SM2	REN	TB8	RB8	TI	RI
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- SM0, SM1 : Serial Port Mode Select
  [0,0] : Mode 0. 8-bit Shift Register (F_{PERI}/4)
  [0,1] : Mode 1. 8-bit UART (Variable)
  [1,0] : Mode 2. 9-bit UART (F_{PERI}/32 or F_{PERI}/16)
  [1,1] : Mode 3. 9-bit UART (Variable)
- SM2 : Enable the Automatic Address Recognition in Mode 2 and 3.
  Clear after receiving the address.
  In Mode 1, Valid Stop Bit Check if SM2=1.
  In Mode 0, SM2 should be 0.
- REN : Serial Reception Enable.
- TB8 : 9th data bit that will be transmitted in Mode 2 and 3.
- RB8 : 9th data bit that was received in Mode 2 and 3.
  In Mode 1, RB8 is equal to Stop Bit if SM2=0.
  In Mode 0, RB8 is not used.
- TI : Transmission Interrupt Flag. Must be cleared by S/W.
- RI : Reception Interrupt Flag. Must be cleared by S/W.

✓ **SBUF** (99h) : Serial Data Buffer Register for UART0

SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- The transmission buffer and the reception buffer are separated.
- The transmission/reception buffers have the same address.

6.8. UART : Automatic Address Recognition

◆ Example

Slave 1:

```
SADDR = 11110001
SADEN = 11111010
GIVEN = 11110X0X
```

Slave 2:

```
SADDR = 11110011
SADEN = 11111001
GIVEN = 11110XX1
```

- A master can selectively communicate with groups of slaves by using the Given Address.
- It sends 11110000 to communicate with just Slave 1.
- It sends 11110111 to communicate with just Slave 2.
- It sends 11110001 or 11110101 to communicate with Slave 1 and Slave 2.

✓ **SADDR**(A9h) : Slave Address Register of UART0

SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- Programmed with the given or broadcast address assigned to serial port0.

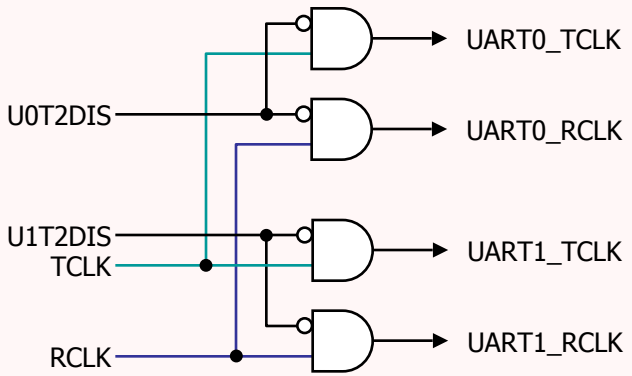
✓ **SADEN**(B9h) : Slave Address Mask Enable Register of UART0

SADEN.7	SADEN.6	SADEN.5	SADEN.4	SADEN.3	SADEN.2	SADEN.1	SADEN.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

◆ Baud Rate Discrimination between UART0 and UART1

✓ An user can selectively disable TCLK or RCLK to set UART0 and UART1 to different baud rates.

✓ For instance, if U0T2DIS is set, UART0 may use Timer1 for baud rate generation even though TCLK or RCLK bit is set.



✓ **CKCON**(8Eh) : Clock Control Register

WD1	WD0	T2M	T1M	T0M	-	U1T2DIS	U0T2DIS
R/W(1)	R/W(1)	R/W(0)	R/W(0)	R/W(0)		R/W(0)	R/W(0)

- U1T2DIS : Used to disable RCLK/TCLK control for UART1 to generate its baud rate with T1 overflow.
- U0T2DIS : Used to disable RCLK/TCLK control for UART0 to generate its baud rate with T1 overflow.

6.8. UART : UART1 SFRs

✓ **SCON1** (B1h) : Serial Port Control Register for UART1

SM0	SM1	SM2	REN	TB8	RB8	TI	RI
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- SM0, SM1 : Serial Port Operating Mode Selection
  [0,0] : Mode 0. 8-bit Shift Register (F_{PERI}/4)
  [0,1] : Mode 1. 8-bit UART (Variable)
  [1,0] : Mode 2. 9-bit UART (F_{PERI}i/32 or F_{PERI}/16)
  [1,1] : Mode 3. 9-bit UART (Variable)
- SM2 : Enable the Automatic Address Recognition in Mode 2 and 3.
  Clear after receiving the address.
  In Mode 1, the Validity of the Stop Bit is checked if SM2=1.
  In Mode 0, SM2 should be 0.
- REN : Enable/Disable Reception.
- TB8 : 9th data bit that will be transmitted in Mode 2 and 3.
- RB8 : 9th data bit that was received in Mode 2 and 3.
  In Mode 1, RB8 is equal to Stop Bit if SM2=0.
  In Mode 0, RB8 is not used.
- TI : Transmission Interrupt Flag. Must be cleared by S/W.
- RI : Reception Interrupt Flag. Must be cleared by S/W.

✓ **SBUF1** (A1h) : Serial Data Buffer for UART1

SBUF1.7	SBUF1.6	SBUF1.5	SBUF1.4	SBUF1.3	SBUF1.2	SBUF1.1	SBUF1.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- Transmission buffer and reception buffer are separated.
- Read and Write address are same.

✓ **SADDR1**(AAh) : Slave Address Register of UART1

SADDR1.7	SADDR1.6	SADDR1.5	SADDR1.4	SADDR1.3	SADDR1.2	SADDR1.1	SADDR1.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- Programmed with the given
  or broadcast address assigned to serial port1.

✓ **SADEN1**(ABh) : Slave Address Mask Enable Register of UART1

SADEN1.7	SADEN1.6	SADEN1.5	SADEN1.4	SADEN1.3	SADEN1.2	SADEN1.1	SADEN1.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

6.8. UART : Baud Rate Example

- Serial Port Mode 0

$$\text{Baudrate} = \frac{\text{Oscillator Frequency}}{4}$$

- Serial Port Mode 2

$$\text{Baudrate} = \frac{2^{SMOD1}}{32} \times \text{Oscillator Frequency}$$

(PCON.7 ←)

- Serial Port Mode 1, 3
  - ✓ Using Timer 1 Overflow

$$\text{Baudrate} = \frac{2^{SMOD1}}{32} \times \text{Timer 1 overflow}$$

  - ✓ Using Timer 2 Overflow

$$\text{Baudrate} = \frac{\text{Timer 2 overflow}}{16}$$

EX) Using Timer 1 to Generate Baudrates

$$\text{Mode 1 \& 3 Baudrate} = \frac{2^{SMOD1}}{32} \times F_{PERI} \times \frac{3^{T1M}}{12} \times \frac{1}{[\,256 - (TH1)\,]}$$

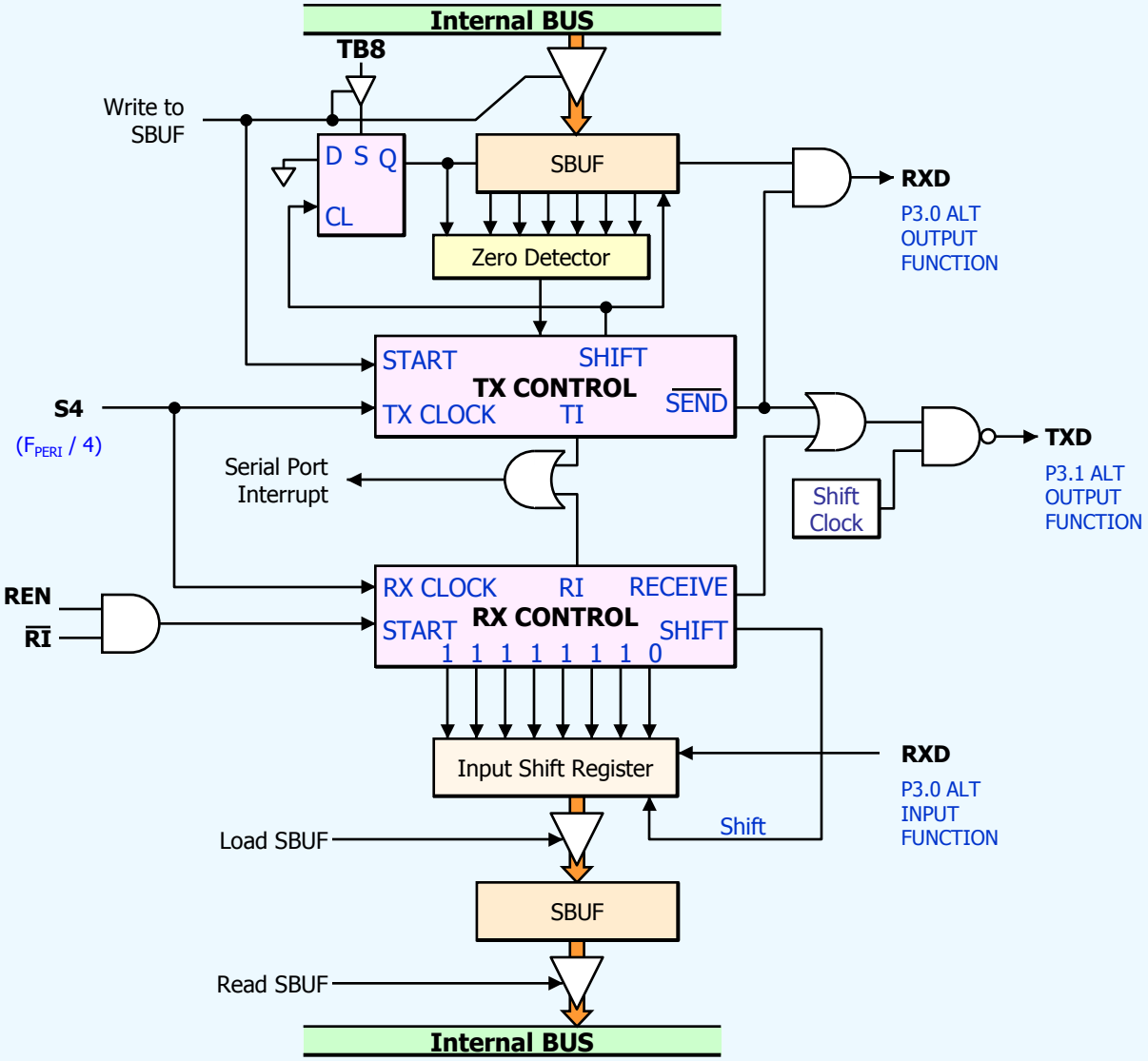
- If SMOD1(PCON.7) = 1 ➔ Double Buadrate
- If T1M(CKCON.4) = 0 ➔ 1/12 x F_{PERI}
- If T1M(CKCON.4) = 1 ➔ 1/4 X F_{PERI}

EX) Using Timer 2 to Generate Baudrates

$$\text{Mode 1 \& 3 Baudrate} = \frac{1}{32} \times F_{PERI} \times \frac{1}{[65536 - (RCAPH,RCAPL)\,]}$$

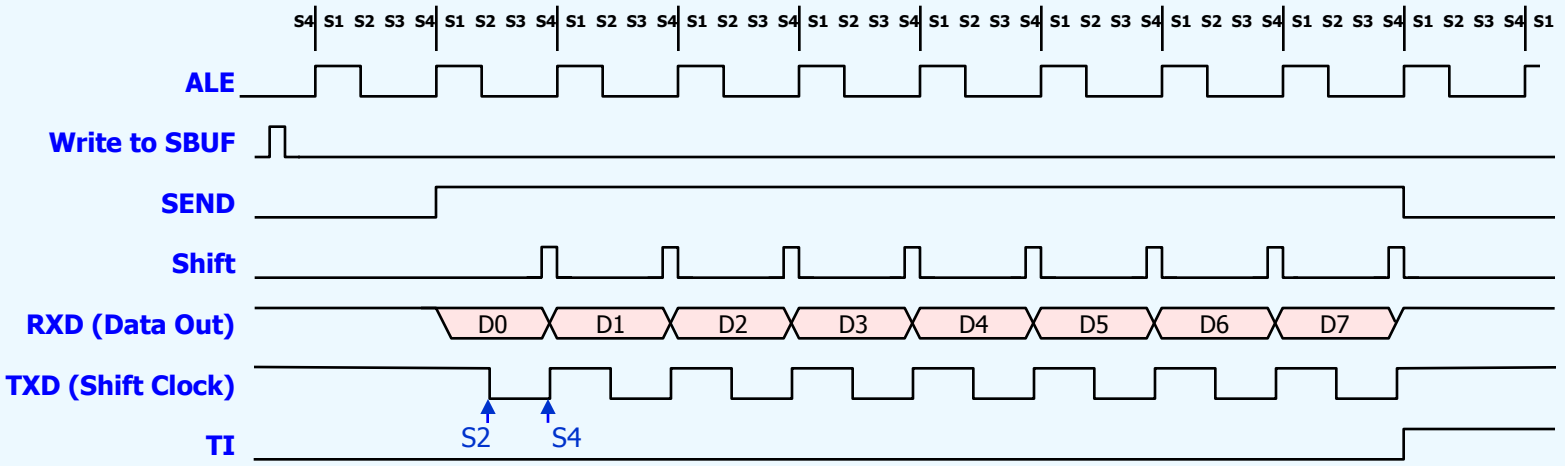
Baudrate		UART Mode	F_{PERI}	SMOD1	Timer 1		
T1M=0	T1M=1				C/T	Mode	Reload Value (TH1)
Max : 3 MHz	Max : 3 MHz	Mode 0	12 MHz	X	X	X	X
Max : 750 KHz	Max : 750 KHz	Mode 2	12 MHz	1	X	X	X
62.5 KHz	187.5 KHz	Mode 1 & 3	12 MHz	1	0	2	FFh
19.2 KHz	57.6 KHz		11.0592 MHz	1	0	2	FDh
9.6 KHz	28.8 KHz		11.0592 MHz	0	0	2	FDh
4.8 KHz	14.4 KHz		11.0592 MHz	0	0	2	FAh
2.4 KHz	7.2 KHz		11.0592 MHz	0	0	2	F4h
1.2 KHz	3.6 KHz		11.0592 MHz	0	0	2	E8h
137.5 Hz	412.5 Hz		11.0592 MHz	0	0	2	1Dh
110 Hz	330 Hz		6 MHz	0	0	2	72h
110 Hz	330 Hz		12 MHz	0	0	1	FEEBh

6.8. UART : Mode 0 Function

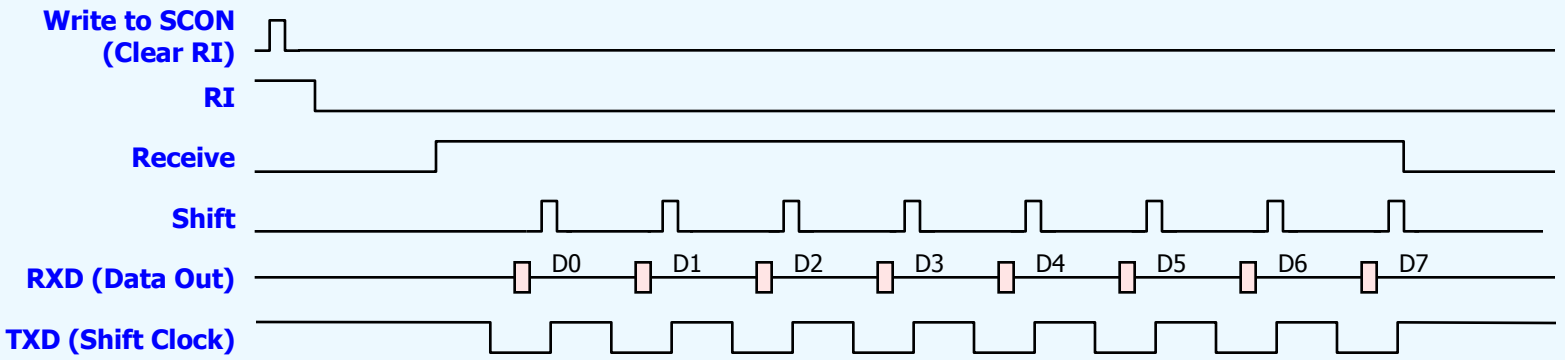


6.8. UART : Mode 0 Timing

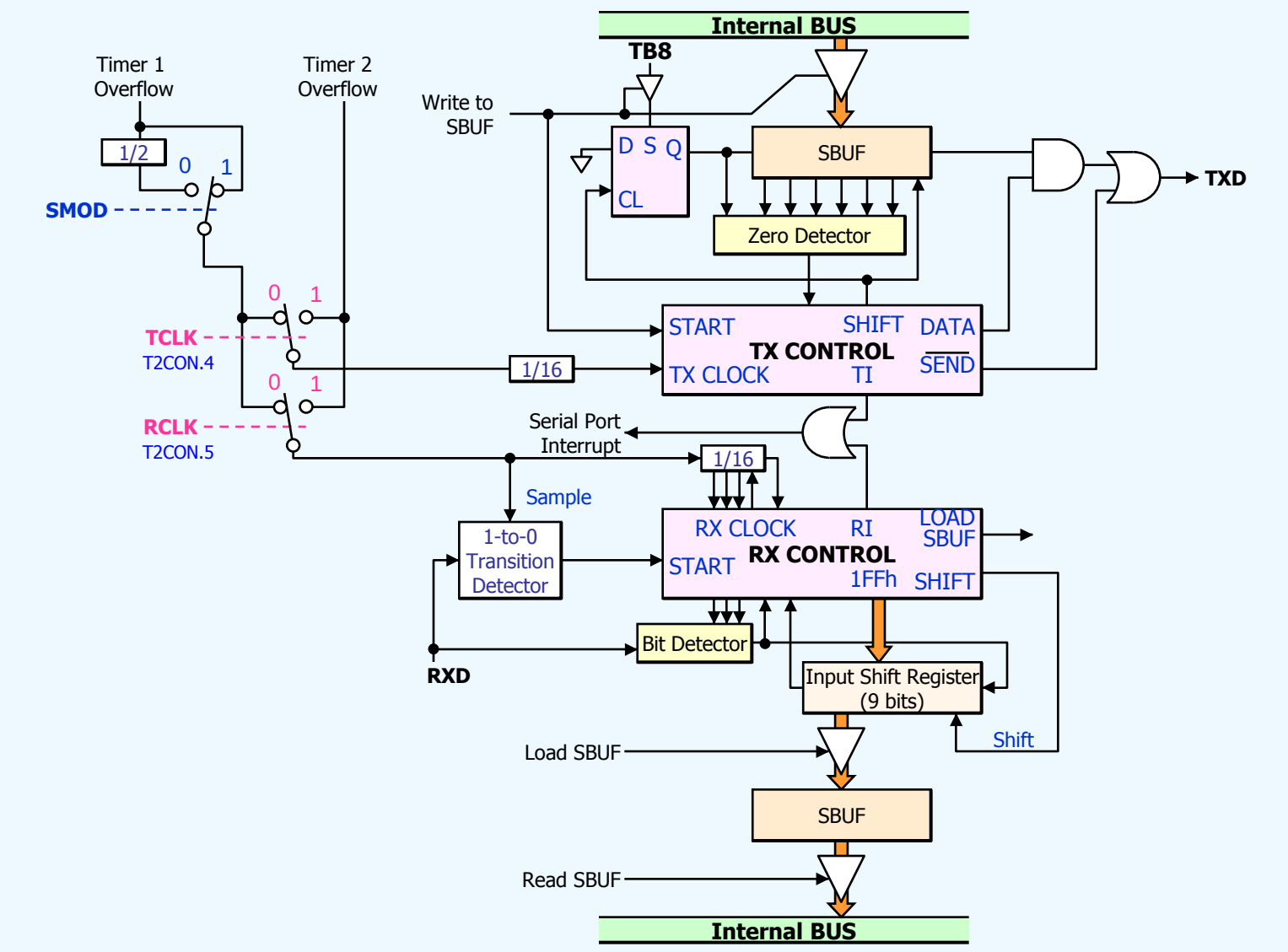
[Transmit]



[Receive]

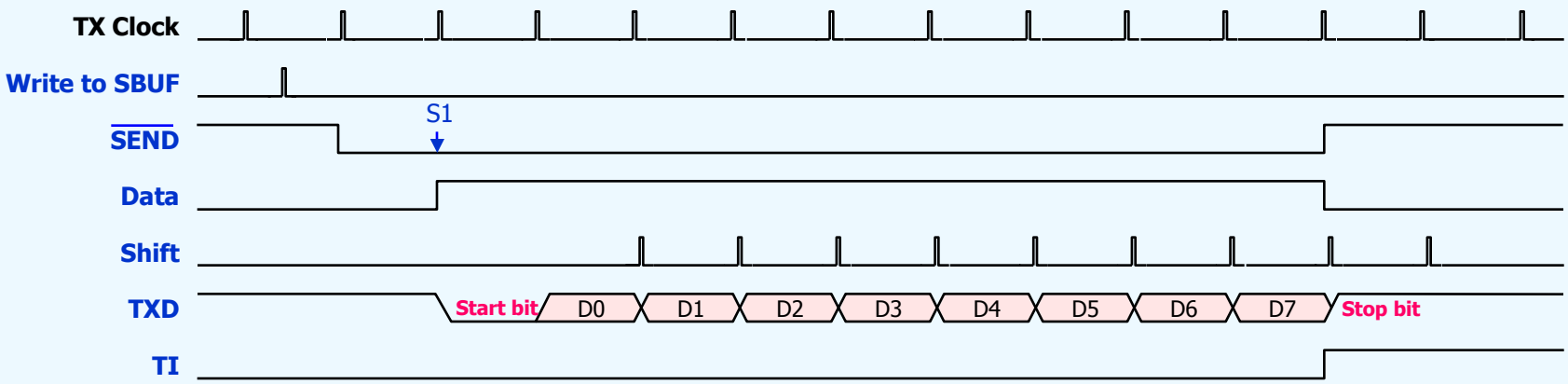


6.8. UART : Mode 1 Function



6.8. UART : Mode 1 Timing

[Transmit]



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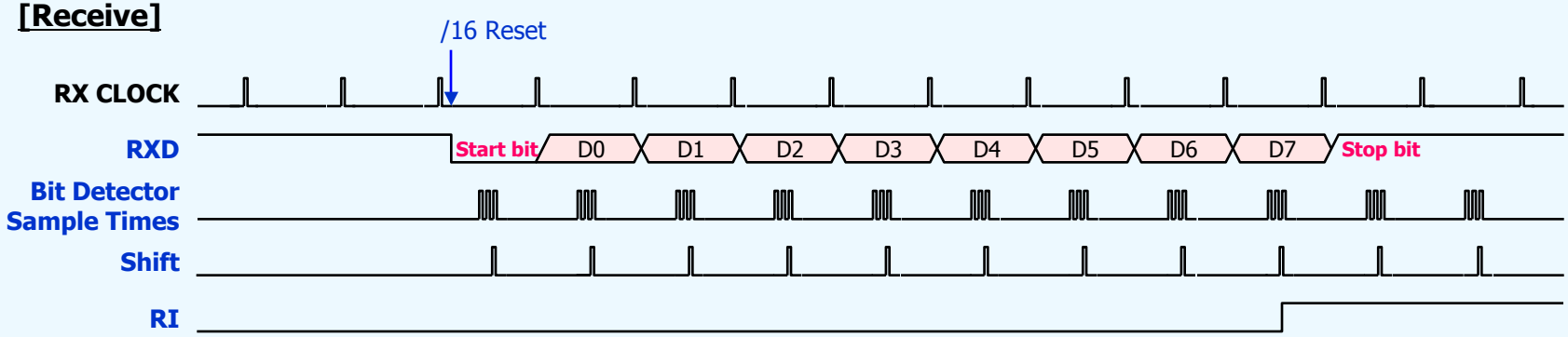
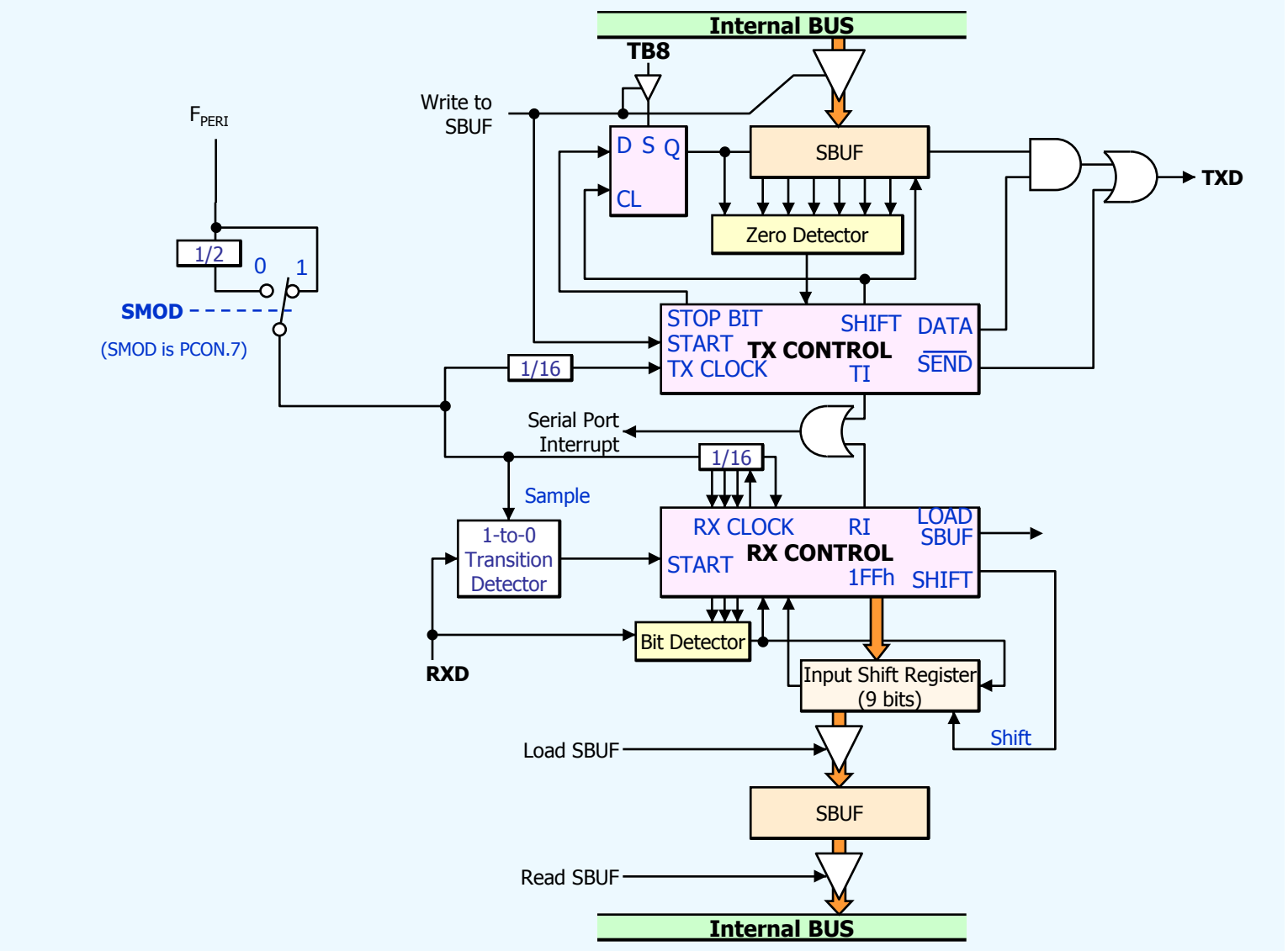
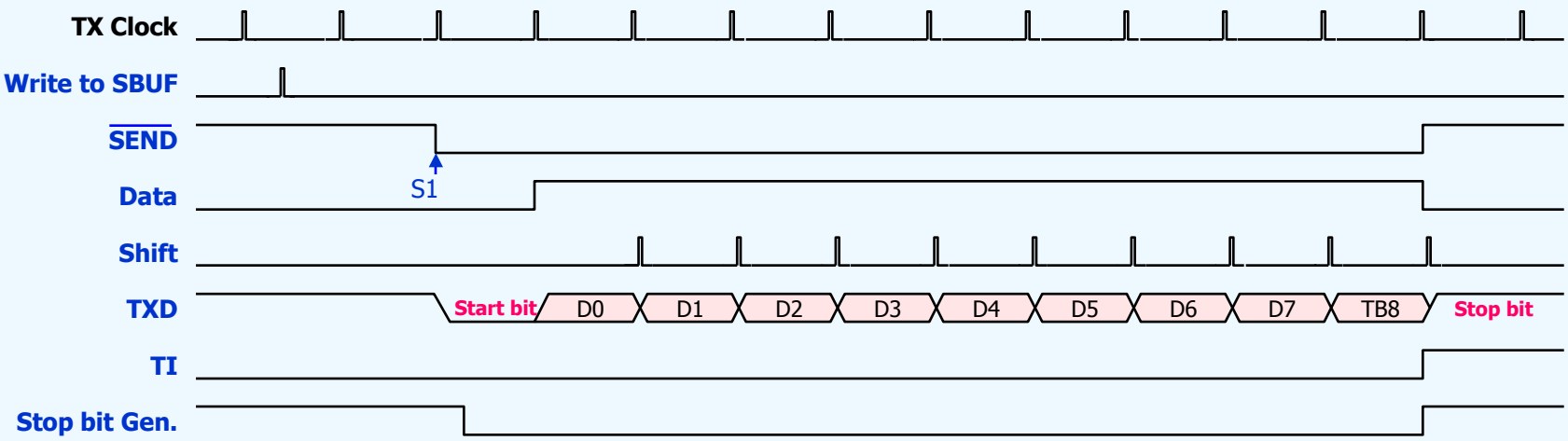


6.8. UART : Mode 2 Function

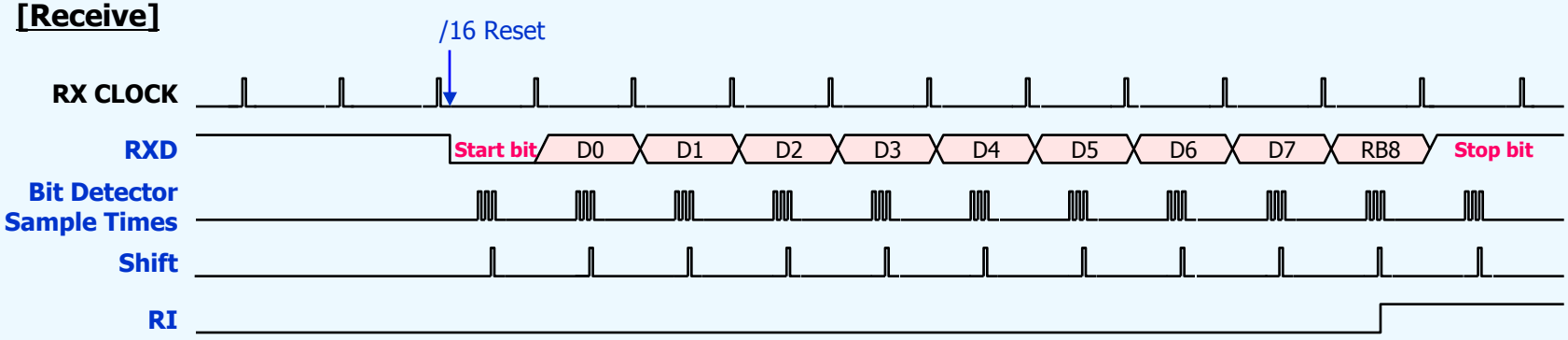


6.8. UART : Mode 2 Timing

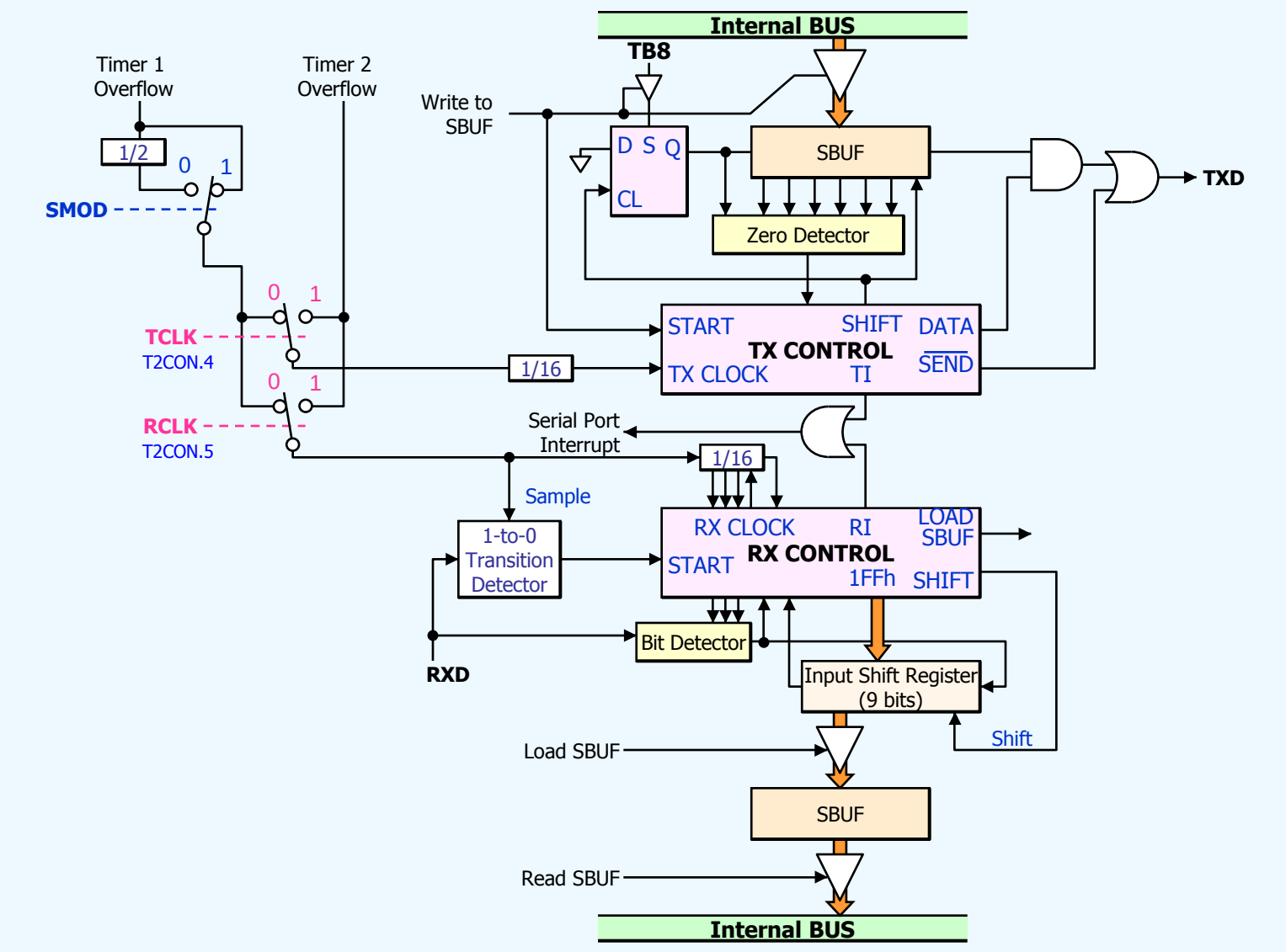
[Transmit]



[Receive]

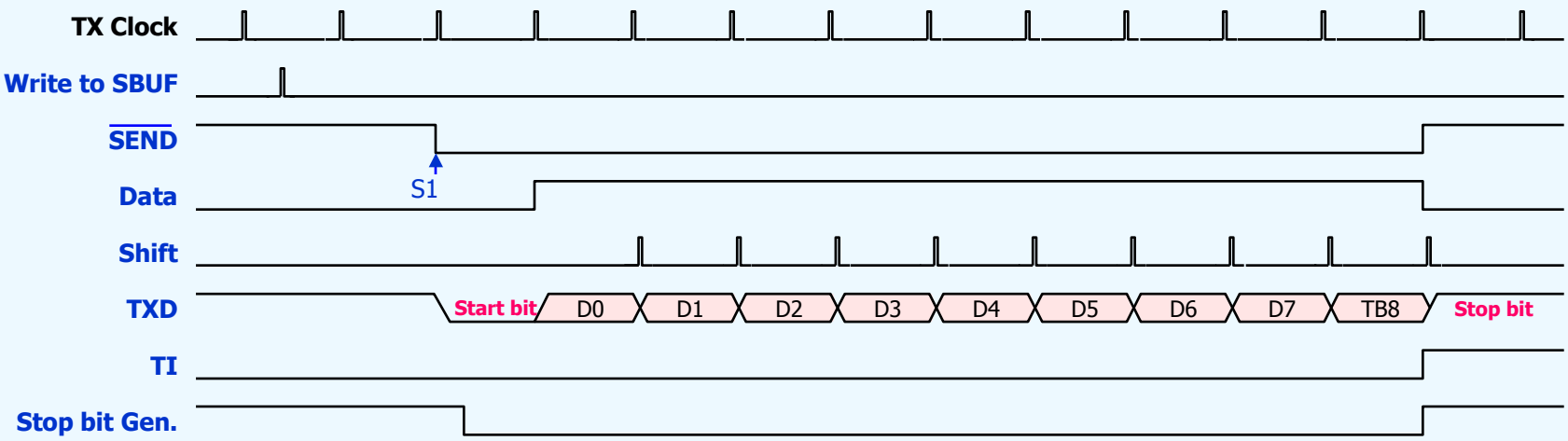


6.8. UART : Mode 3 Function

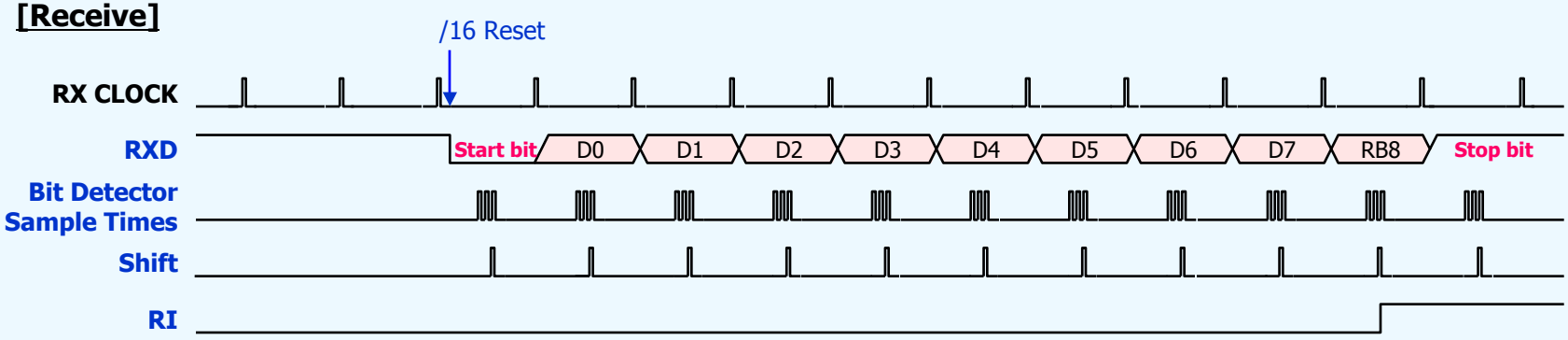


6.8. UART : Mode 3 Timing

[Transmit]



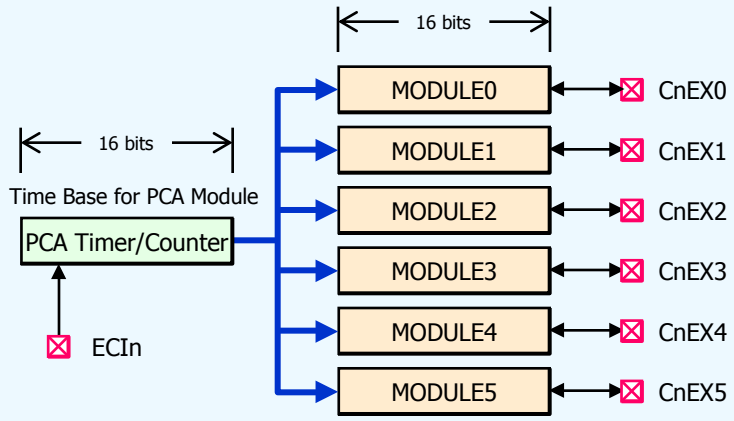
[Receive]



6.9. PCA (Programmable Counter Arrays)

- Basic Feature
  - ✓ Compatible to Intel/Philips PCA.
  - ✓ Support two PCAs.
  - ✓ Each PCA provides 6 modules.
  - ✓ An 8-bit prescaler generates the PCA clock.

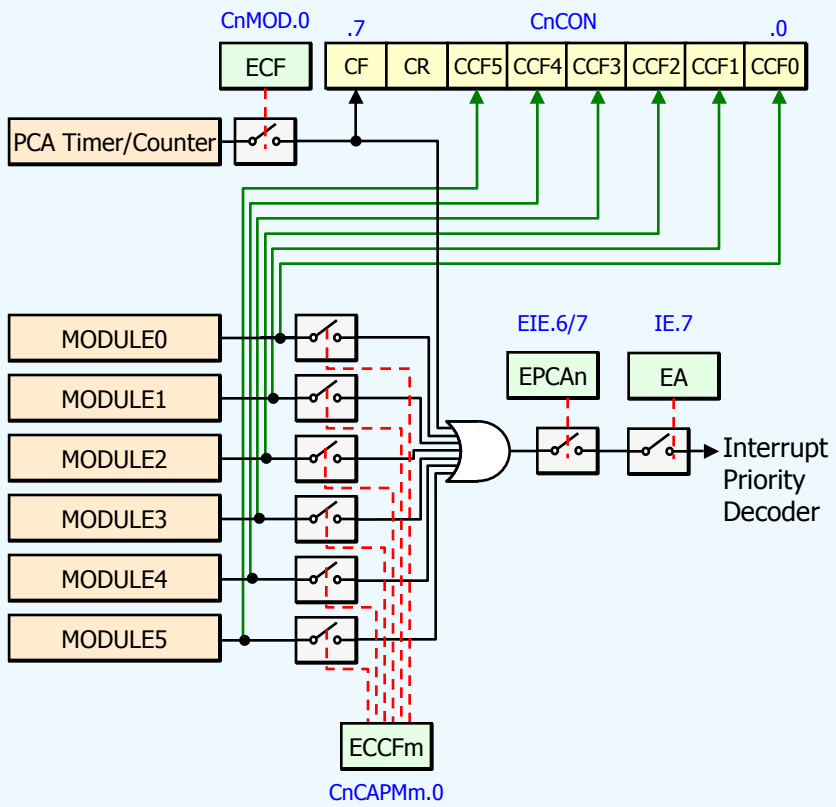
[PCAn]



- **Module Functions:**
  - 16-bit Capture
  - 16-bit Timer
  - 16-bit High Speed Output
  - 16-bit/8-bit Fixed PWM Output
  - 16-bit/8-bit Dynamic PWM Output

- Unique Features
  - ✓ Each PCA provides 6 modules.
  - ✓ In the auto-reset mode, CnL is reset when a match occurs between CnL and CnH.
  - ✓ Support Dynamic PWM (Pulse Width Modulation) by using the auto-reset mode.
  - ✓ An 8-bit prescaler generates the PCA clock.
  - ✓ Provides 16-bit/8-bit Dynamic PWM (Pulse Width Modulation) by exploiting the auto-reset modes.
  - ✓ Each PCA provides max. six 8-bit PWM outputs .
  - ✓ Each PCA provides max. three 16-bit PWM outputs (module 0, 2, 4).

6.9. PCA : Interrupt Sources of a PCA



✓ **C0CON** (ACh) : PCA0 Counter Control Register

CF	CR	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- CF : PCA counter overflow flag.
  Set by hardware when the counter rolls over.
  CF flags an interrupt if bit ECF in COMOD is set.
  CF may be set by either hardware or software but
  can only be cleared by software
- CR : PCA counter run control bit.
  Set by software to turn the PCA counter on.
  Must be cleared by software to turn the PCA counter off.
- CCF5 : PCA module 5 interrupt flag.
  Set by hardware when a match or capture occurs.
  Must be cleared by software.
- CCF4 : PCA module 4 interrupt flag.
- CCF3 : PCA module 3 interrupt flag.
- CCF2 : PCA module 2 interrupt flag.
- CCF1 : PCA module 1 interrupt flag.
- CCF0 : PCA module 0 interrupt flag.

✓ **C1CON** (CEh) : PCA1 Counter Control Register

CF	CR	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

6.9. PCA : PCAn Counter Control Registers

- To use a PCA Counter as an 8-bit Auto-reset Counter
  - ✓ Turn off the PCAn by clearing CR bit (CnCON.6)
  - ✓ Load target values into CnL and CnH.
  - ✓ Set PWMDYN bit (CnMOD.6) and set CF bit (CnCON.7)
  - ✓ Run PCAn by setting CR bit (CnCON.6)
  - ✓ An interrupt will occur when CnL reaches to CnH.
  - ✓ Insert the procedure for the PCAn counter overflow into the PCA interrupt service routine.

✓ **C0MOD** (ADh) : PCA0 Counter Mode Register

CIDL	PWMDYN	PWM16	CPS3	CPS2	CPS1	CPS0	ECF
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- CIDL : Counter idle control.
  CIDL = 0 programs the PCA counter to continue functioning during idle mode.
  CIDL = 1 programs it to be stop during idle mode.
- PWMDYN : Dynamic PWM bit.
  If this bit is set, the dynamic PWM is generated.
  C0L is cleared when a match occurs between C0L and C0H.
  The match signal replaces the overflow signal for PWM.
- PWM16 : Enable 16-bit PWM generation.
  If this bit is set, two timer counter modules are paired to generate one 16-bit PWM output.
  Refer to following table.
- CPS[3:0] : PCA prescaler rate (F_{PCA}) selection. (Refer to below Table)
- ECF : Enable PCA counter overflow interrupt.
  ECF = 1 enables CF bit in C0CON to generate an interrupt.
  ECF = 0 disables that function.

✓ **C1MOD** (CFh) : PCA1 Counter Mode Register

[PCA counter operation mode]

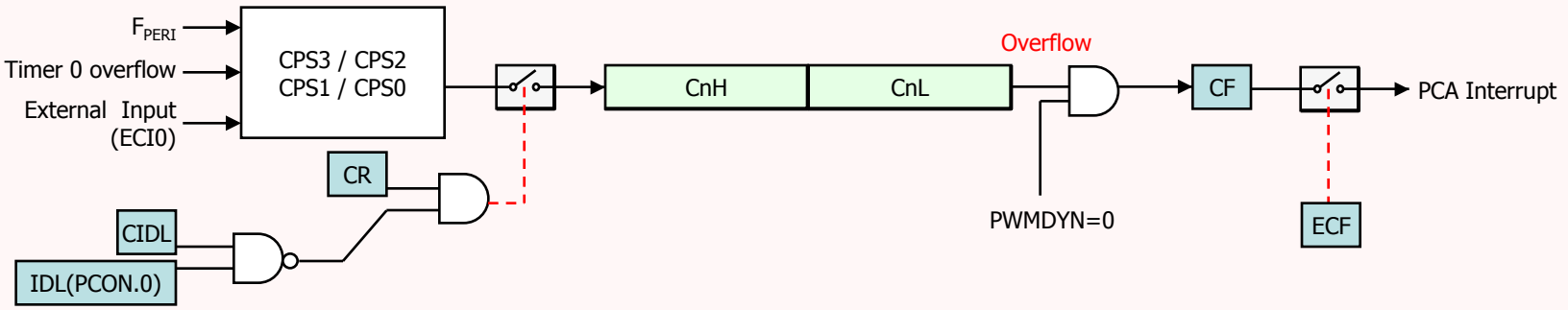
PWMDYN	PWM16	PCA Counter Mode
0	0	16-bit free running mode. Interrupt occurs when PCA counter rolls over to 0 from 0xFFFF. This is the default operation.
0	1	16-bit free running mode. Interrupt occurs when PCA counter rolls over to 0 from 0xFFFF. In this mode, module 0, 2, and 4 may be used to generate 16-bit fixed PWM.
1	0	8-bit auto-reset mode. CnL is reset when CnL reaches to CnH. This also triggers an interrupt and renewal of 8-bit PWM registers.
1	1	16-bit auto-reset mode. The PCA counter is reset when it reaches to capture compare register of module 0 (CnCAP0H, CnCAP0L). Since module 0 and 1 are used to modulate the period of PCA counter, the 16-bit dynamic PWM output is available only in module 2 or 4.

[Count Rate (F_{PCA}) Selection]

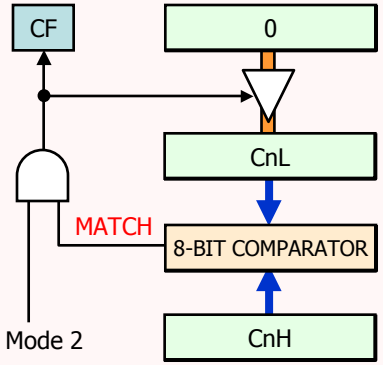
CPS3	CPS2	CPS1	CPS0	Description
0	0	0	0	0 Internal clock, F_{PERI}
0	0	0	1	1 Internal clock, F_{PERI} / 2
0	0	1	0	2 Internal clock, F_{PERI} / 4
0	0	1	1	3 Internal clock, F_{PERI} / 8
0	1	0	0	4 Internal clock, F_{PERI} / 12
0	1	0	1	5 Internal clock, F_{PERI} / 16
0	1	1	0	6 Internal clock, F_{PERI} / 32
0	1	1	1	7 Internal clock, F_{PERI} / 64
1	0	0	0	8 Internal clock, F_{PERI} / 128
1	0	0	1	9 Internal clock, F_{PERI} / 256
1	0	1	0	10 External clock at ECIn pin (max rate = F_{PERI} / 2)
1	0	1	1	11 Timer 0 overflow

6.9. PCA : PCAn Counter

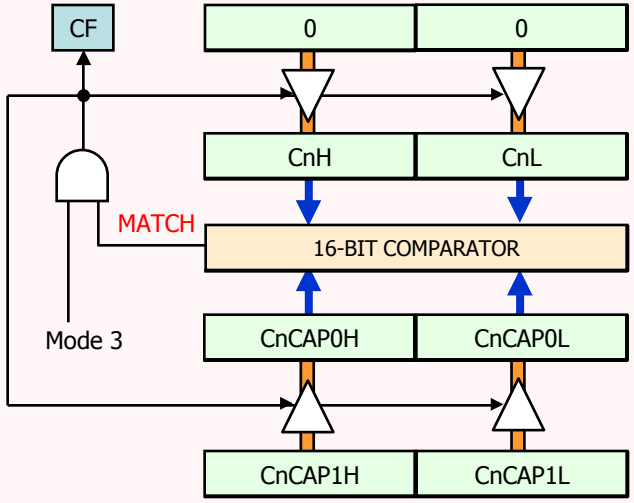
[Mode 0/1 (PWMDYN=0, PWM16=0/1)]



[Mode 2 (PWMDYN=1, PWM16=0)]



[Mode 3 (PWMDYN=1, PWM16=1)]



6.9. PCA : PCAn Module Control Registers

✓ **C0CAPM0** (A2h) : Mode Control Register of PCA0 MODULE0

IPWM0	ECOM0	CAPP0	CAPN0	MAT0	TOG0	PWM0	ECCF0
R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- IPWM0 : Inverted PWM output.
  If this bit is set, the PWM output is high when C0L ≥ C0CAPmL.
  The change of this bit will take effect from the next overflow / match time of PWM.
- ECOM0 : Enable comparator.
  ECOM0 = 1 enables the comparator function.
- CAPP0 : Capture positive.
  CAPP0 = 1 enables positive edge capture.
- CAPN0 : Capture negative.
  CAPN0 = 1 enables negative edge capture.
- MAT0 : Match.
  When MAT0 = 1, a match of the PCA counter with this module's comparator/capture register causes the CCF0 bit int C0CON to be set, flagging an interrupt.
- TOG0 : Toggle.
  When TOG0 = 1, a match of the PCA counter with this module's comparator/capture register causes the C0EX0 pin to toggle.
- PWM0 : Pulse width modulation mode.
  PWM0 = 1 enables the C0EX0 pin to be used as a pulse width modulated output.
- ECCF0 : Enable CCF interrupt.
  Enables compare/capture flag CCF0 in the C0CON register to generate an interrupt.

✓ **C0CAPM1** (A3h) : Mode Control Register of PCA0 MODULE1
✓ **C0CAPM2** (A4h) : Mode Control Register of PCA0 MODULE2
✓ **C0CAPM3** (A5h) : Mode Control Register of PCA0 MODULE3
✓ **C0CAPM4** (A6h) : Mode Control Register of PCA0 MODULE4
✓ **C0CAPM5** (A7h) : Mode Control Register of PCA0 MODULE5

✓ **C1CAPM0** (E2h) : Mode Control Register of PCA1 MODULE0
✓ **C1CAPM1** (E3h) : Mode Control Register of PCA1 MODULE1
✓ **C1CAPM2** (E4h) : Mode Control Register of PCA1 MODULE2
✓ **C1CAPM3** (E5h) : Mode Control Register of PCA1 MODULE3
✓ **C1CAPM4** (E6h) : Mode Control Register of PCA1 MODULE4
✓ **C1CAPM5** (E7h) : Mode Control Register of PCA1 MODULE5

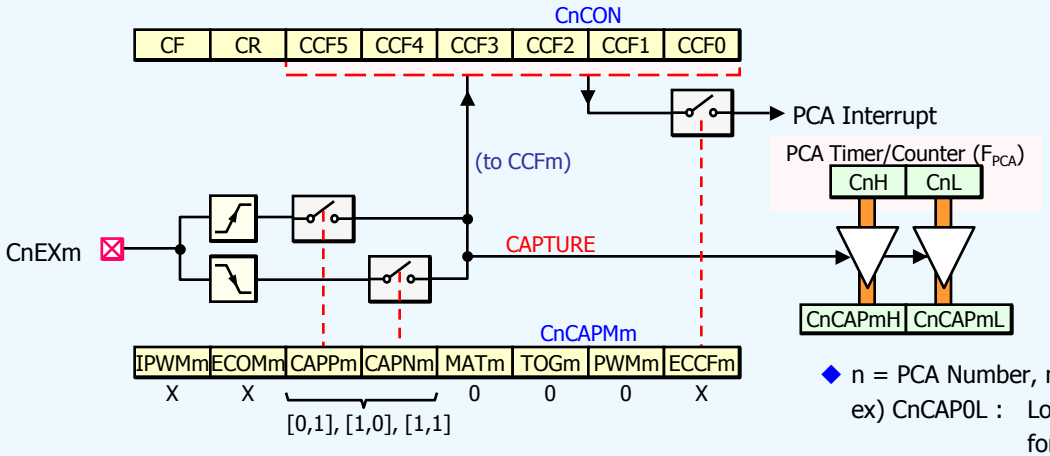
[PCA Module Modes (CnCAPMm Register)]

IPWMm	ECOMm	CAPPm	CAPNm	MATm	TOGm	PWMm	ECCFm	Module Function
X	0	0	0	0	0	0	0	No operation
X	X	1	0	0	0	0	X	1) 16-bit capture by a positive-edge trigger on CnEXm
X	X	0	1	0	0	0	X	1) 16-bit capture by a negative-edge trigger on CnEXm
X	X	1	1	0	0	0	X	1) 16-bit capture by any transition on CnEXm
X	1	0	0	1	0	0	X	2) 16-bit software timer
X	1	0	0	1	1	0	X	3) 16-bit high speed output
0	1	0	0	0	0	1	0	4) 5) 8-bit PWM normal output
1	1	0	0	0	0	1	0	4) 5) 8-bit PWM inverted output

* 1) ~ 5) : Refer to next slides.

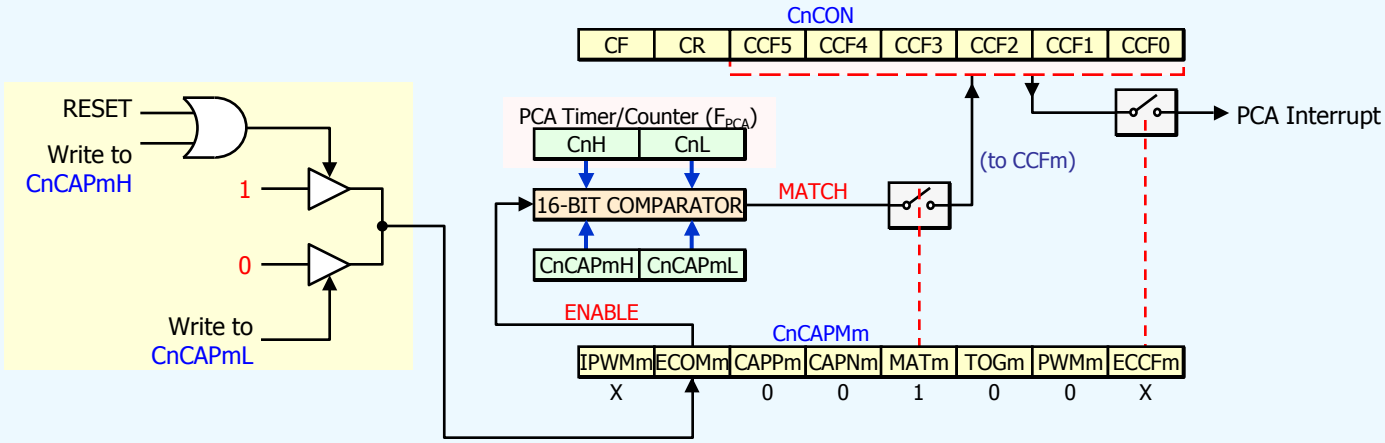
6.9. PCA : PCA Modes

1) Capture Mode



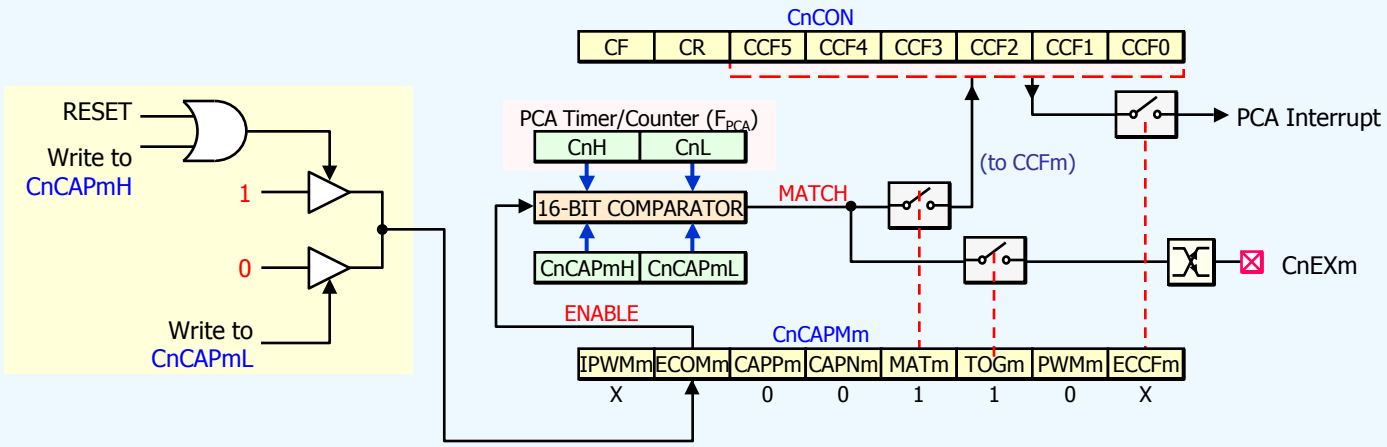
◆ n = PCA Number, m = Module Number
ex) CnCAP0L : Low Capture/Compare Register for Module0 of PCAn

2) Compare/Timer Mode



6.9. PCA : PCA Modes

3) PCA High Speed Output Mode

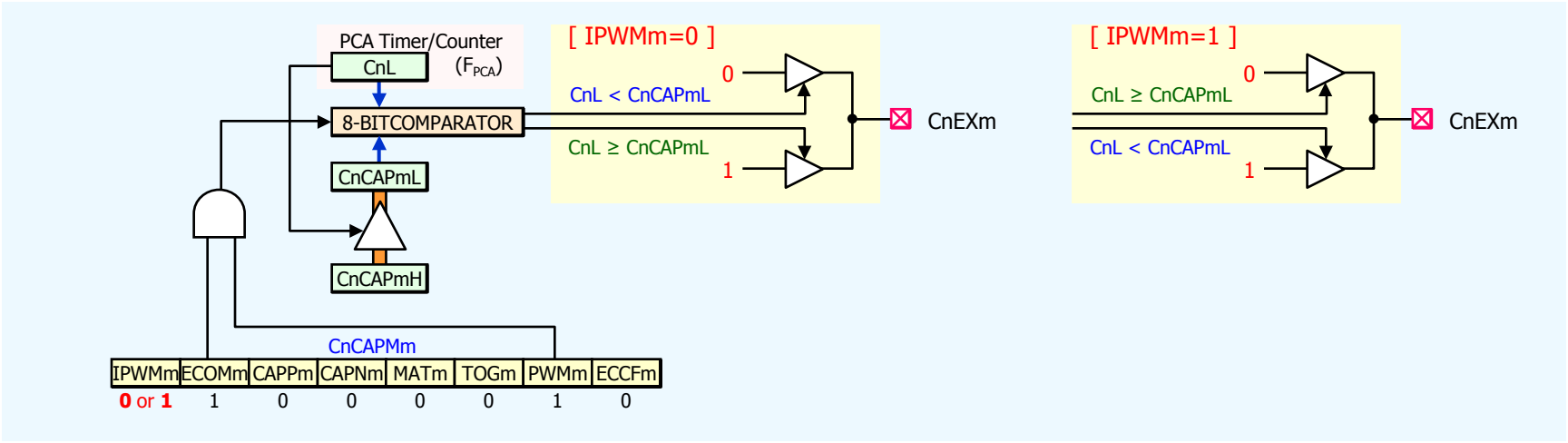


[Update of CnCAPmH & CnCAPmL]

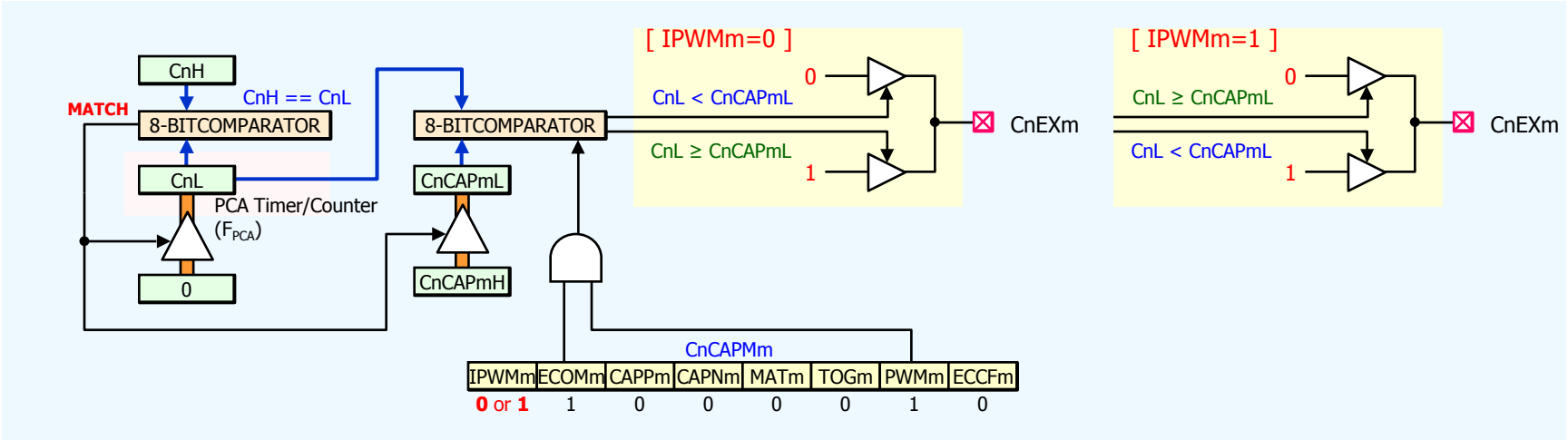
- During the interrupt routine, a new 16-bit compare value can be written to the compare register (CnCAPmH & CnCAPmL)
- Notice, however, that a write to CnCAPmL clears the ECOMm bit, which temporarily disables the comparator function while these registers are being updated so an invalid match does not occur.
- A write to CnCAPmH sets the ECOMm bit and re-enables the comparator.
- For this reason, user software should write to CnCAPmL first, then the CnCAPmH.

6.9. PCA : PCA Modes

4) 8-bit fixed PWM Mode (PWMDYN = 0, PWM16 = 0)

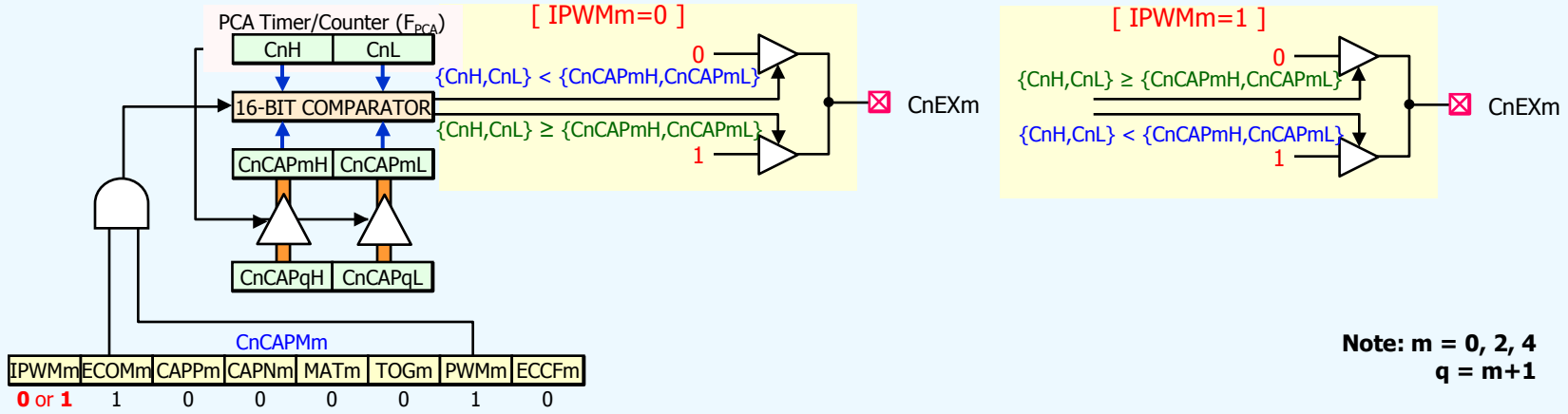


5) 8-bit dynamic PWM Mode (PWMDYN = 1, PWM16 = 0)

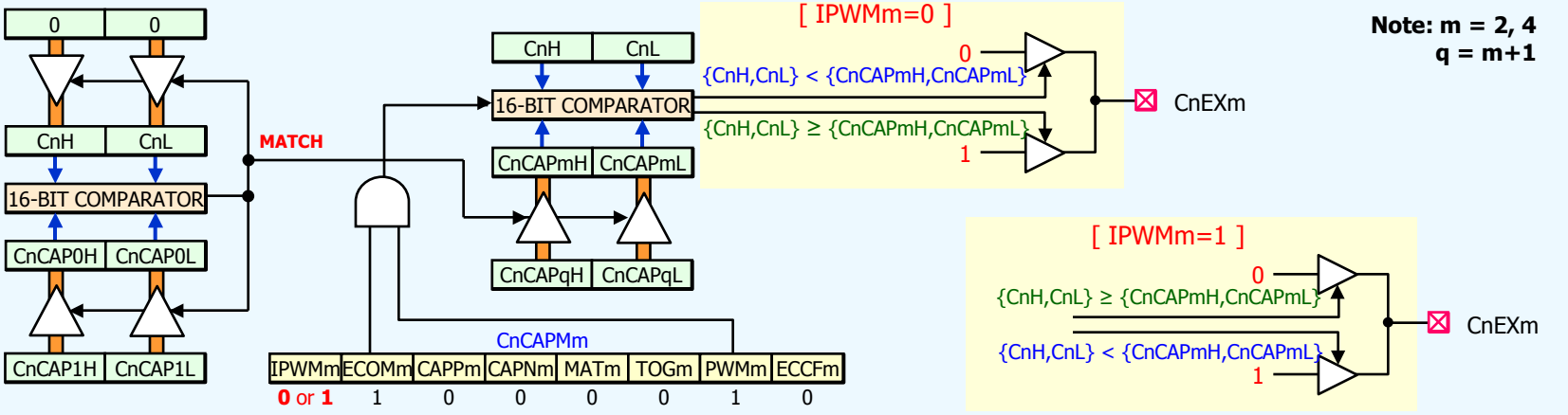


6.9. PCA : PCA Modes

6) 16-bit fixed PWM Mode (PWMDYN = 0, PWM16 = 1)

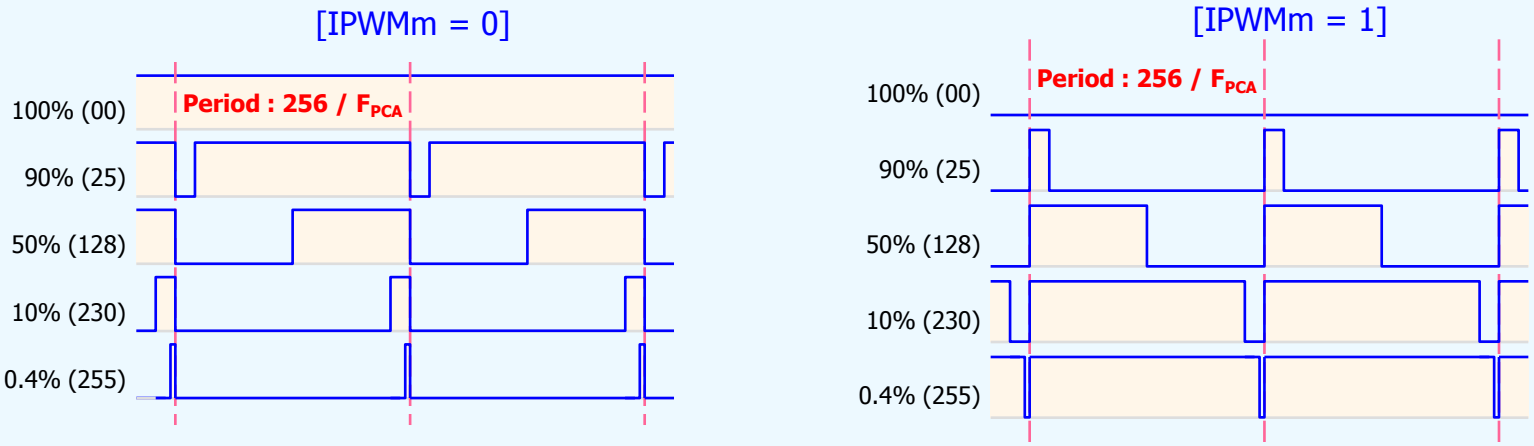


7) 16-bit dynamic PWM Mode (PWMDYN = 1, PWM16 = 1)

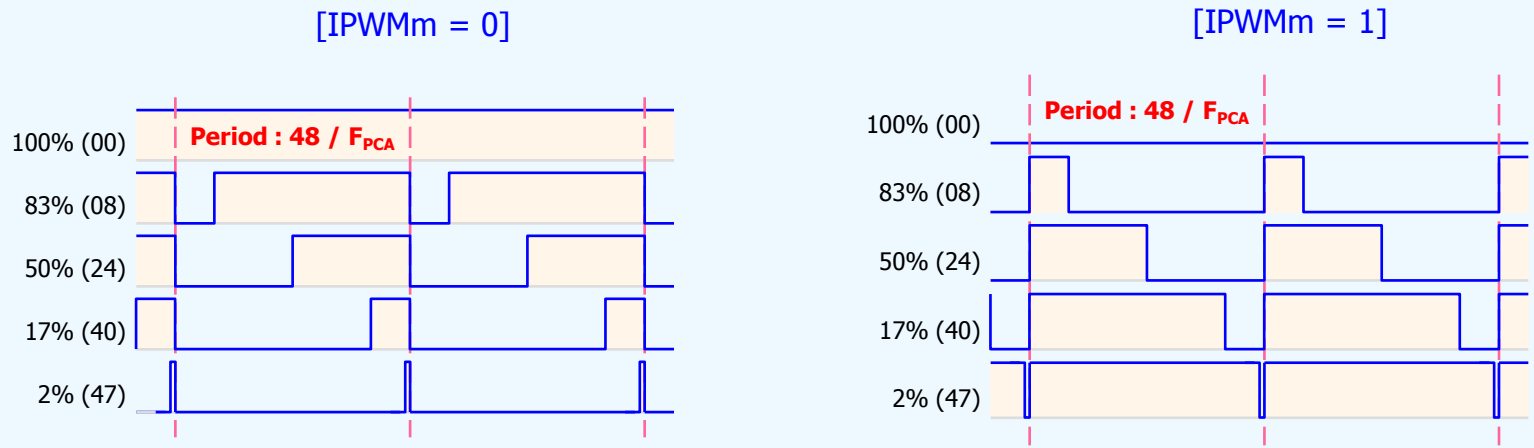


6.9. PCA : Examples of 8-bit PWM Output

- Duty Cycle with PWMDYN = 0, PWM16 = 0.

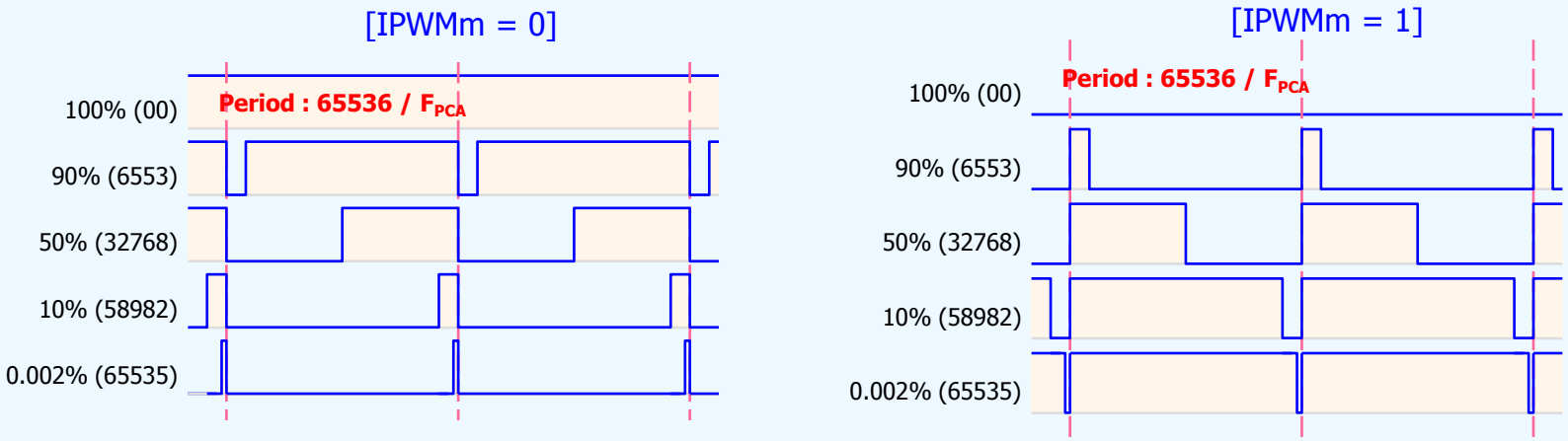


- Duty Cycle with , PWMDYN = 1, PWM16 = 0, CnH = 47(0x2F).

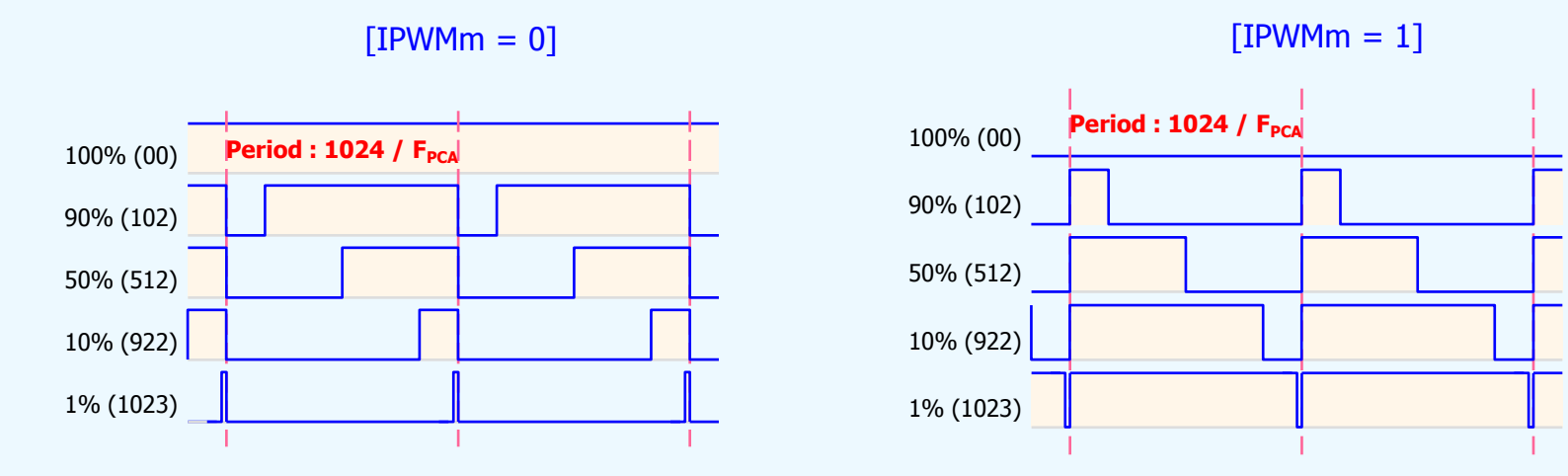


6.9. PCA : Examples of 16-bit PWM Output

- Duty Cycle with PWMDYN = 0, PWM16 = 1.



- Duty Cycle with , PWMDYN = 1, PWM16 = 1, CnCAP0H = CnCAP1H = 4, CnCAP0L = CnCAP1L = 0.



6.10. ADC (Analog-to-Digital Converter)

- 8-channel 10-bit ADC (SAR Type)
- Max. 104ksps(samples per sec.) @ FADC = 10MHz & 3V. (Max. 52ksps @ FADC = 5MHz & 3V)

✓ **ADCON** (84h) : ADC Control & ADC Result Low Register

AD_EN	AD_REQ	AD_END	ADCF	-	-	SAR1	SAR0
R/W(0)	R/W(0)	R(1)	R/W(0)			R/W(0)	R/W(0)

- AD_EN : ADC Ready Enable
- AD_REQ : ADC Start.
  Cleared by H/W when AD_END goes to 1 from 0.
- AD_END : Current ADC Status.
  0 = ADC is running now.
  User must check the ADCF instead of AD_END.
- ADCF : ADC Interrupt Flag.
  Must be cleared by S/W.
- SAR[1:0] : Low Bits of ADC Result Value. (Total 10 bits)

✓ **ADCR** (86h) : ADC Result High Register

SAR9	SAR8	SAR7	SAR6	SAR5	SAR4	SAR3	SAR2
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

✓**ADCSEL** (85h) : ADC Clock and MUX Selection Register

ADIV2	ADIV1	ADIV0	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ADIV[2:0] : ADC clock selection.
  [000] : FSYS / 2.
  [001] : FSYS/ 4.
  [010] : FSYS / 8.
  [011] : FSYS / 16.
  [100] : FSYS / 32.
  [101] : FSYS / 64.
  [110] : FSYS / 128.
  [111] : FSYS / 256.
- ADCS[4:0] : ADC channel selection
  [00000] : ADC0.0 channel selection.
  [00001] : ADC0.1 channel selection.
  [00010] : ADC0.2 channel selection.
  [00011] : ADC0.3 channel selection.
  [00100] : ADC0.4 channel selection.
  [00101] : ADC0.5 channel selection.
  [00110] : ADC0.6 channel selection.
  [00111] : ADC0.7 channel selection.
  [01000] : ADC1.0 channel selection.
  .....
  [10111] : ADC2.7 channel selection.
  [11000] : ADC3.0 channel selection.
  [11001] : ADC3.1 channel selection.
  [11010] : ADC3.2 channel selection.
  [11011] : ADC3.3 channel selection.
  [11100] : ADC3.4 channel selection.
  [11101] : ADC3.5 channel selection.
  [11110] : ADC3.6 channel selection.
  [11111] : ADC3.7 channel selection.

6.10. ADC (Block Diagram)

✓ **ADCENB0** (ECh) : ADC Channel Enable Bar Register (P0 port)

ADCENB0.7	ADCENB0.6	ADCENB0.5	ADCENB0.4	ADCENB0.3	ADCENB0.2	ADCENB0.1	ADCENB0.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- 0 = ADC0 channel ON / 1 = ADC0 channel OFF (Default)

✓ **ADCENB1** (EDh) : ADC Channel Enable Bar Register (P1 port)

ADCENB1.7	ADCENB1.6	ADCENB1.5	ADCENB1.4	ADCENB1.3	ADCENB1.2	ADCENB1.1	ADCENB1.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- 0 = ADC1 channel ON / 1 = ADC1 channel OFF (Default)

✓ **ADCENB2** (EEh) : ADC Channel Enable Bar Register (P1 port)

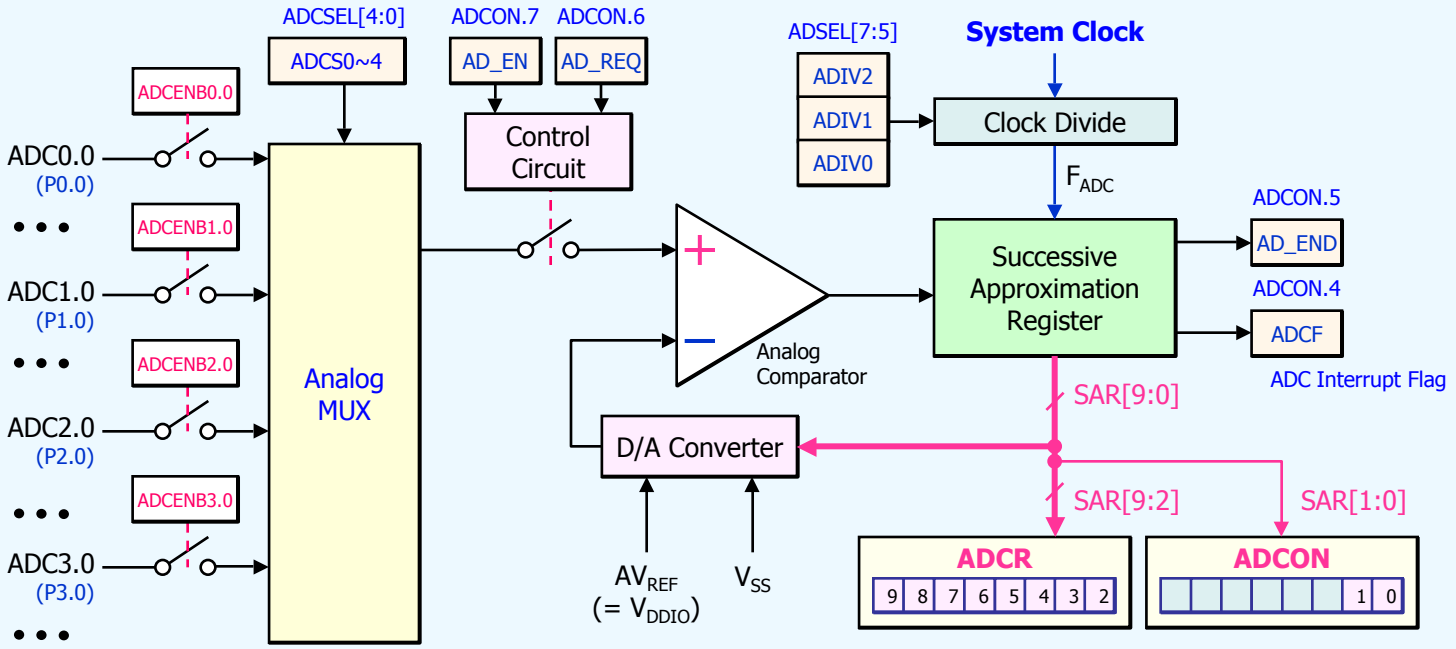
ADCENB2.7	ADCENB2.6	ADCENB2.5	ADCENB2.4	ADCENB2.3	ADCENB2.2	ADCENB2.1	ADCENB2.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- 0 = ADC2 channel ON / 1 = ADC2 channel OFF (Default)

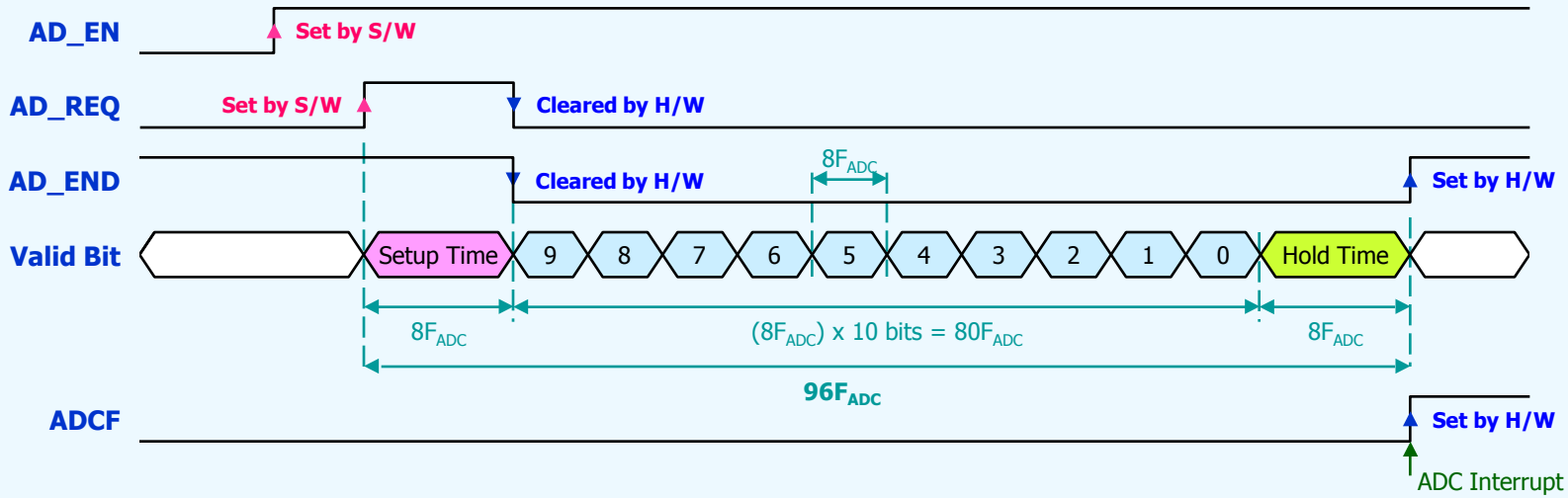
✓ **ADCENB3** (EEh) : ADC Channel Enable Bar Register (P1 port)

ADCENB3.7	ADCENB3.6	ADCENB3.5	ADCENB3.4	ADCENB3.3	ADCENB3.2	ADCENB3.1	ADCENB3.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- 0 = ADC3 channel ON / 1 = ADC3 channel OFF (Default)



6.10. ADC : Conversion Timing



- ✓ **AD_EN** : ADC Block Enable Signal.
  Set or Cleared by S/W.
- ✓ **AD_REQ** : ADC Conversion Request Start Bit.
  Set by S/W and Cleared by H/W.
  This bit must be set at each sample conversion.
- ✓ **AD_END** : Set or Cleared by H/W.
  Clear when Conversion started.
  Set when Conversion ended.
- ✓ **ADCF** : ADC Interrupt Flag.
  Set by H/W and Cleared by S/W.
  User should clear ADCF bit in ADC interrupt routine.
  User must check the ADCF flag instead of AD_END.

[An Example of ADC Conversion Table]

System Clock (F_{PERI})	Divide (ADIV=0)	F_{ADC}	T_{ADC} ($1/F_{ADC}$)	1 Sample Conversion Time
20MHz @ 3V	$F_{PERI}/2$	10MHz	100ns	9.6us
10MHz @ 3V	$F_{PERI}/2$	5MHz	200ns	19.2us
10MHz @ 3V	$F_{PERI}/2$	5MHz	200ns	19.2us
5MHz @ 3V	$F_{PERI}/2$	2.5MHz	400ns	38.4us

6.11. I2C Slave Module : SFRs

- Support 1.2MHz @ 100MHz internal clock
- Support 7bit Slave Address
  - ✓ Address register is shared with Wakeup module
- 32byte RX/TX independent data buffer
  - ✓ RX : 32byte FIFO
  - ✓ TX : 32byte FIFO
- Support single/multi byte access
- I2C protocol : Only device address (No sub-address)
- Support No ACK state
  - ✓ When Device address is mismatched
  - ✓ When RX buffer is full
  - ✓ When TX buffer is empty, except for multi-byte read
- Port sharing between Wake-up module and I2C Slave
  - ✓ Power Down mode : Wake-up module enable
  - ✓ Active mode : I2C slave enable

✓ **IT** (B2h) : Interrupt Type Selection Register

EI2C	FI2C	PI2C	I2C_EN	IT5	IT4	IT3	IT2
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- EI2C : I2C Interrupt Enable Flag
- FI2C : I2C Interrupt Flag
- PI2C : I2C Interrupt Priority
- I2C_EN : Normal I2C Enable Flag
  [0] : Normal I2C Disable
  [1] : Normal I2C Enable

✓ **UINDX** (F9h) : Wakeup/I2C INDEX Register

I2C_BS	I2C_RXP	-	UINDX4	UINDX3	UINDX2	UINDX1	UINDX0
R (0)	R/W(1)	-	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

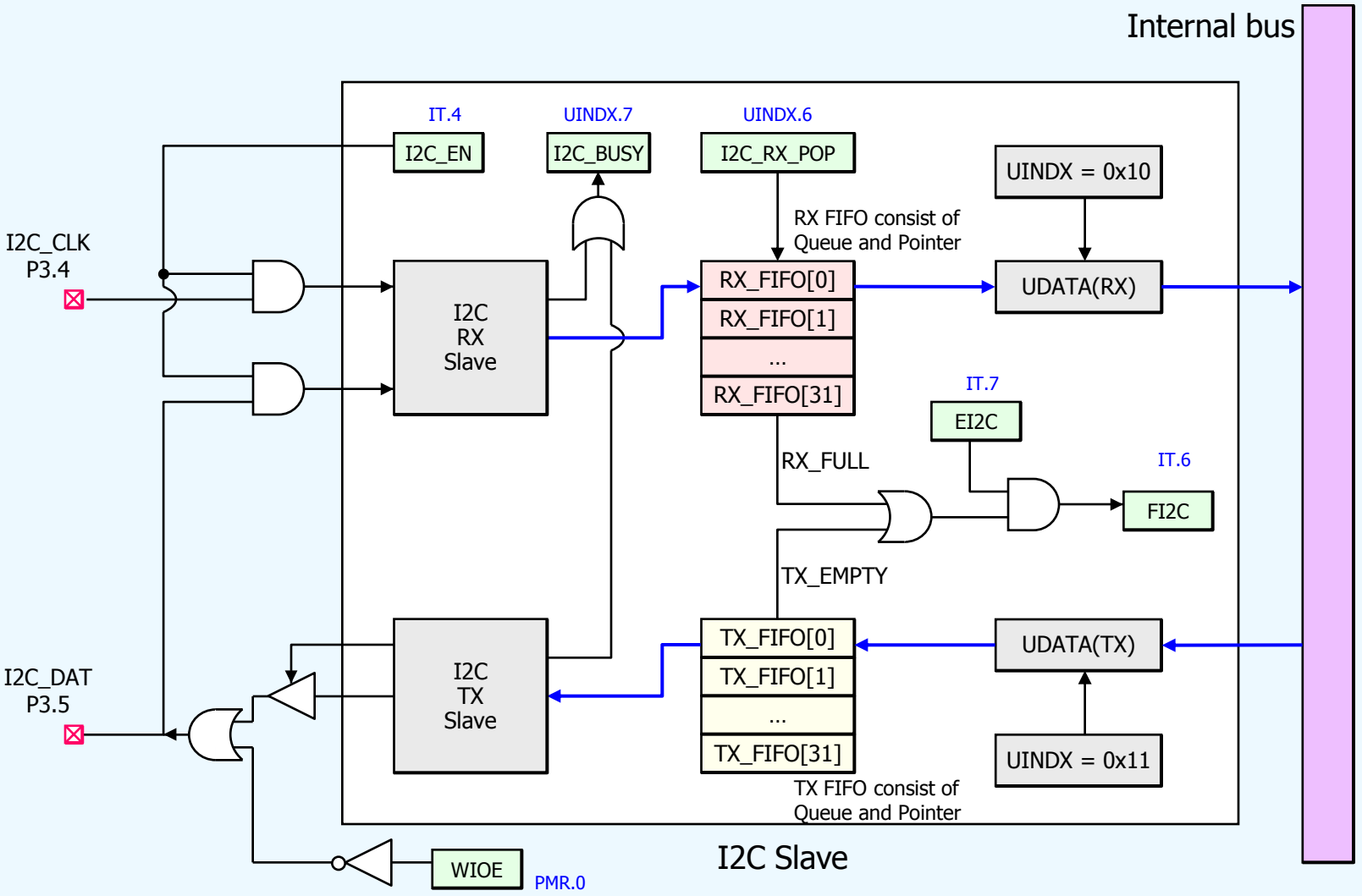
- I2C_BS : I2C Busy Flag
  [0] : Idle
  [1] : Busy
- I2C_RXP : I2C RX FIFO pop
  [0] : Idle
  [1] : Pop FIFO, and move data to UDATA SFR (cleared automatically by H/W)
- UINDX[4:0] : Wakeup Index Register
  [10000] : I2C RX FIFO indirect address
  [10001] : I2C TX FIFO indirect address
  [10010] : I2C RX FIFO pointer indirect address
  [10011] : I2C TX FIFO pointer indirect address
  [01111] : I2C Slave address
  [0XXXX] : reserved

✓ **UDATA** (FAh) : Wakeup/I2C Data Register

UDAT7	UDAT6	UDAT5	UDAT4	UDAT3	UDAT2	UDAT1	UDAT0
R/W(0)	R/W(1)	R/W(1)	R/W(0)	R/W(0)	R/W(1)	R/W(1)	R/W(1)

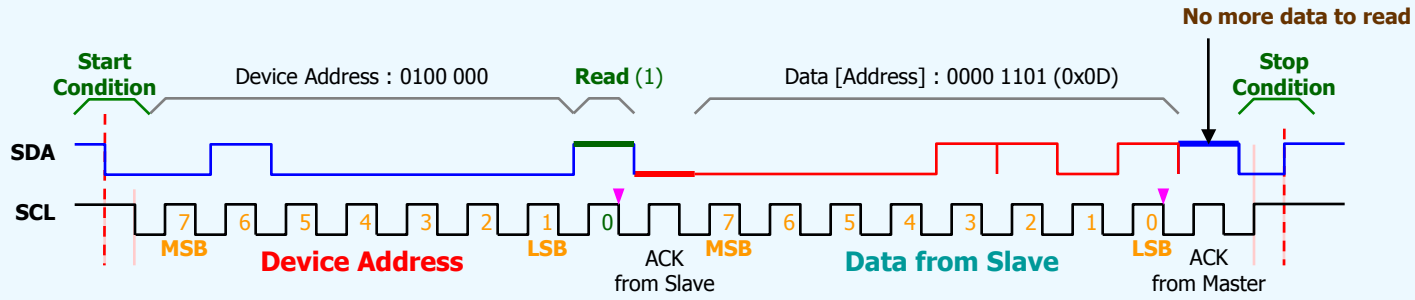
- UDATA[7:0] : I2C Data Register

6.11. I2C Slave Module : I2C Slave Block

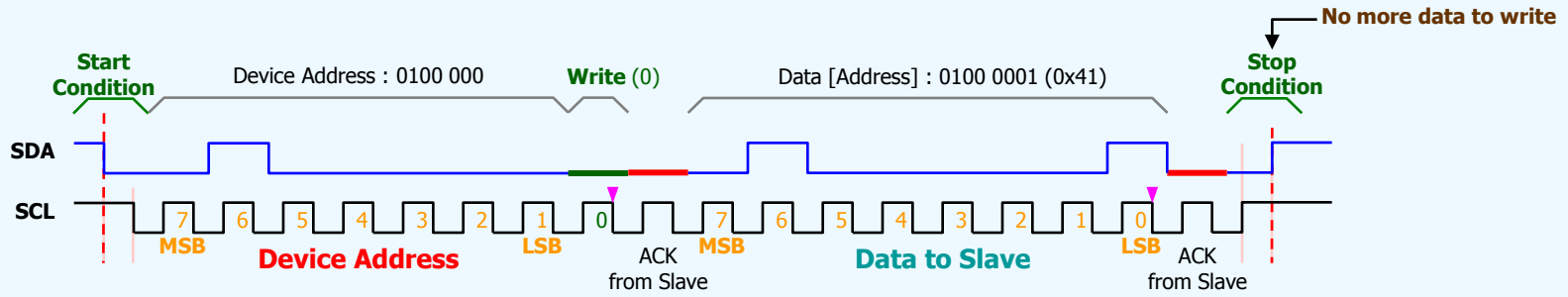


6.11. I2C Slave Module : Single Byte Read/Write

- 1 Byte Read Timing without Memory Address

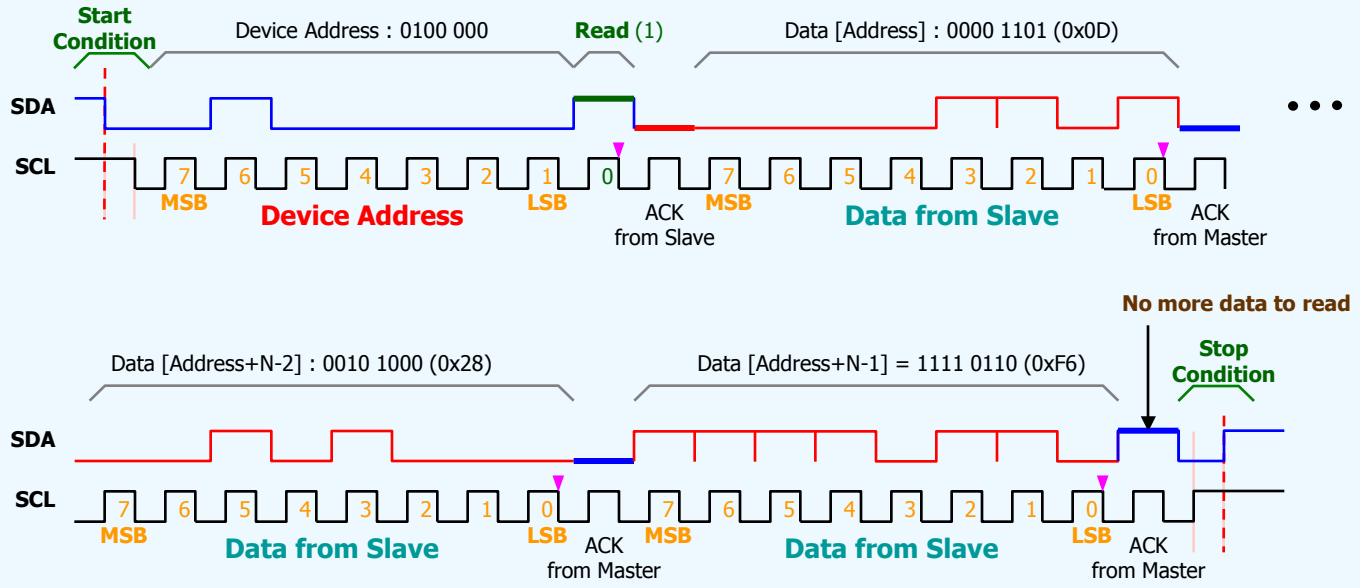


- 1 Byte Write Timing without Memory Address



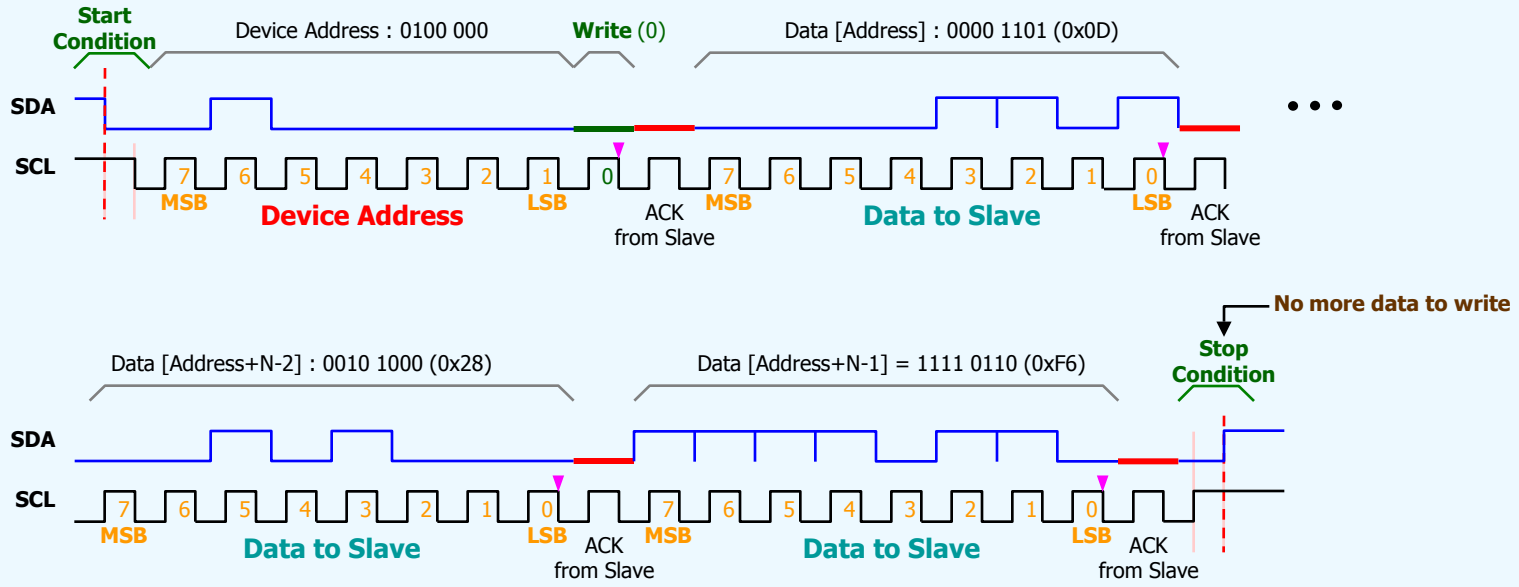
6.11. I2C Slave Module : Multi Bytes Read

- Multi (N) Bytes Read Timing



6.11. I2C Slave Module : Multi Bytes Write

- Multi (N) Bytes Write Timing



6.12. Interrupt : 16 Sources / 4-level Priority

- Interrupt Sources : Timer 0/1/2, UART0/1, PCA0/1, WDT, ADC, I2C, 6 External.
- 4-level Interrupt Priority

[Interrupt Vector Address]

HIGH

PRIORITY

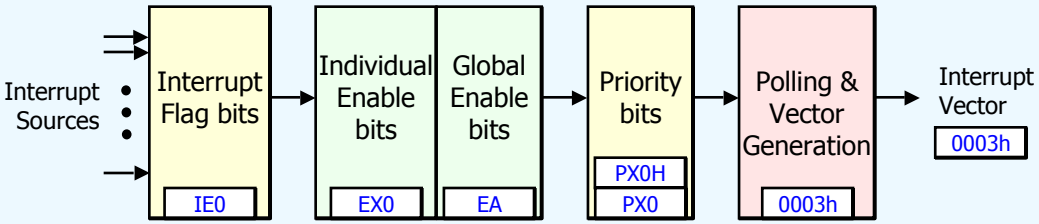
LOW

Interrupt Sources	Address	Priority Level	
/INT0	0003h	4 Levels	8052
TF0	000Bh	4 Levels	
/INT1	0013h	4 Levels	
TF1	001Bh	4 Levels	
RI+TI	0023h	4 Levels	
TF2	002Bh	4 Levels	
ADC	003Bh	4 Levels	
INT2	0043h	2 Levels	
/INT3	004Bh	2 Levels	
INT4	0053h	2 Levels	
/INT5	005Bh	2 Levels	
WDT	0063h	2 Levels	
RI1+TI1	006Bh	2 Levels	
PCA0	0073h	2 Levels	
PCA1	007Bh	2 Levels	
I2C	0083h	2 Levels	

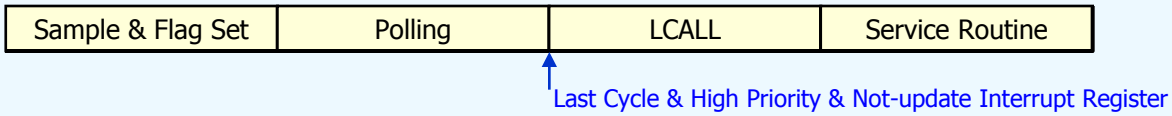
*** Interrupt SFR's (refer to Appendix B : SFR Description)**

✓ **TCON** (88h)	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
✓ **IT** (B2h)	EI2C	FI2C	PI2C	I2C_EN	IT5	IT4	IT3	IT2
✓ **ITSEL** (BAh)	-	-	ITSEL5	ITSEL4	ITSEL3	ITSEL2	ITSEL1	ITSEL0
✓ **EXIF** (91h)	IE5	IE4	IE3	IE2	XT/RL	RGM0	RGSL	BGS
✓ **IE** (A8h)	EA	EADC	ET2	ES	ET1	EX1	ET0	EX0
✓ **EIE** (E8h)	EPCA1	EPCA0	ES1	EWDT	EX5	EX4	EX3	EX2
✓ **IP** (B8h)	-	PADC	PT2	PS	PT1	PX1	PT0	PX0
✓ **IPH** (B7h)	-	PADCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
✓ **EIP** (F8h)	PPCA1	PPCA0	PS1	PWDT	PX5	PX4	PX3	PX2
✓ **WDCON** (D8h)	-	POR	EPFI	PFI	WDIF	WTRF	EWT	RWT

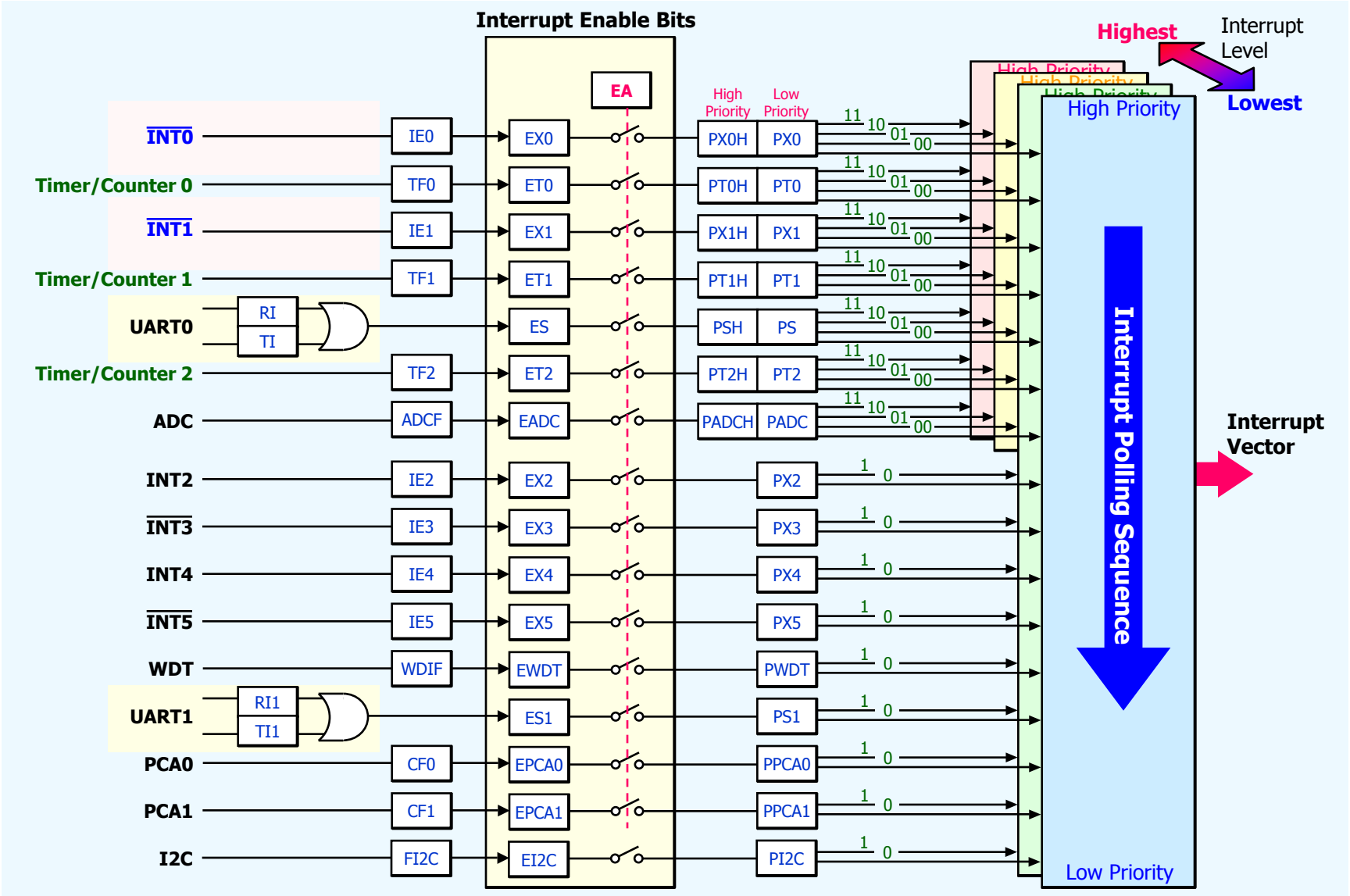
[Interrupt Vector Generation Flow]



[Response Sequence]



6.12. Interrupt : Functional Description



6.12. Interrupt : External Interrupt

- External Interrupt Sources : INT2, /INT3, INT4, /INT5.
- Support positive edge and negative edge detection
- Support high level and low level detection

✓ **ITSEL** (BAh) : Interrupt Polarity Selection Register

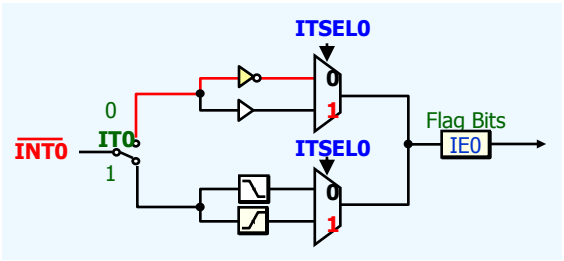
-	-	ITSEL5	ITSEL4	ITSEL3	ITSEL2	ITSEL1	ITSEL0
-	-	R/W(0)	R/W(1)	R/W(0)	R/W(1)	R/W(0)	R/W(0)

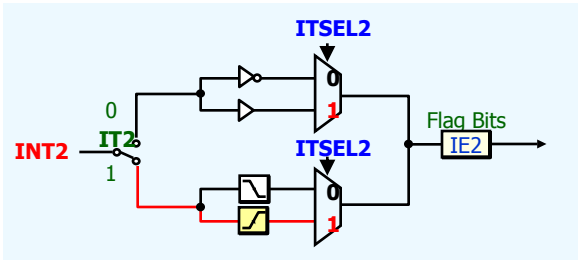
- ITSEL5 : Interrupt5 Polarity Selection Flag
  [0] : low level or negative edge, [1] : high / positive
- ITSEL4 : Interrupt4 Polarity Selection Flag
  [0] : low level or negative edge, [1] : high / positive
- ITSEL3 : Interrupt3 Polarity Selection Flag
  [0] : low level or negative edge, [1] : high / positive
- ITSEL2 : Interrupt2 Polarity Selection Flag
  [0] : low level or negative edge, [1] : high / positive
- ITSEL1 : Interrupt1 Polarity Selection Flag
  [0] : low level or negative edge, [1] : high / positive
- ITSEL0 : Interrupt0 Polarity Selection Flag
  [0] : low level or negative edge, [1] : high / positive

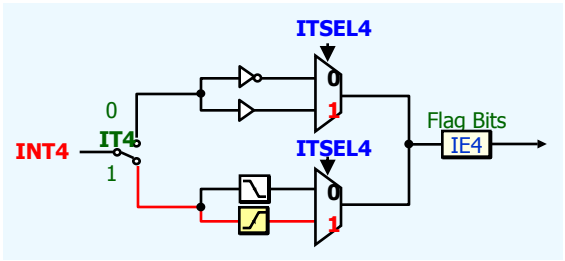
✓ **IT** (B2h) : Interrupt Type Selection Register

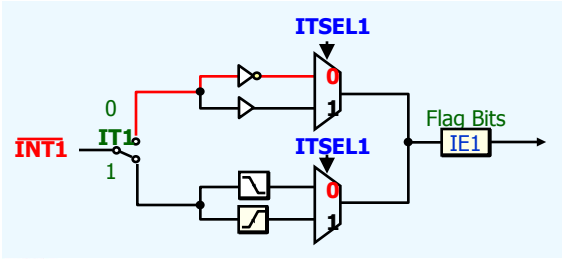
EI2C	FI2C	PI2C	I2C_EN	IT5	IT4	IT3	IT2
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

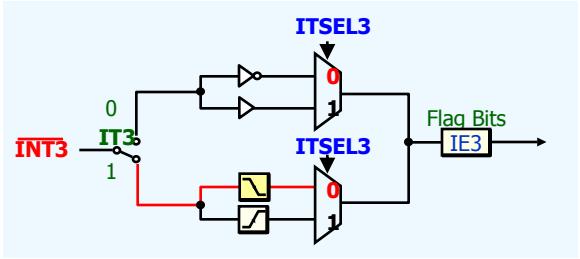
- EI2C : I2C Interrupt Enable Flag
- FI2C : I2C Interrupt Flag
- PI2C : I2C Interrupt Priority
- I2C_EN : Normal I2C Enable Flag
  [0] : Normal I2C Disable, [1] : Normal I2C Enable
- IT5 : Interrupt5 Type Selection Flag
  [0] : Level detect, [1] : Edge detect
- IT4 : Interrupt4 Type Selection Flag
  [0] : Level detect, [1] : Edge detect
- IT3 : Interrupt3 Type Selection Flag
  [0] : Level detect, [1] : Edge detect
- IT2 : Interrupt2 Type Selection Flag
  [0] : Level detect, [1] : Edge detect

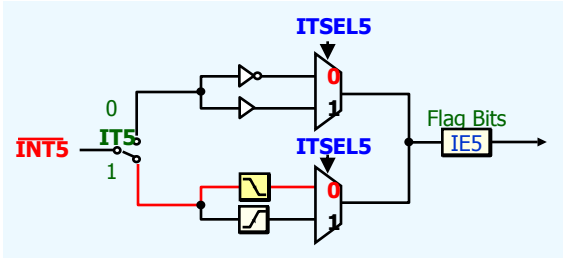












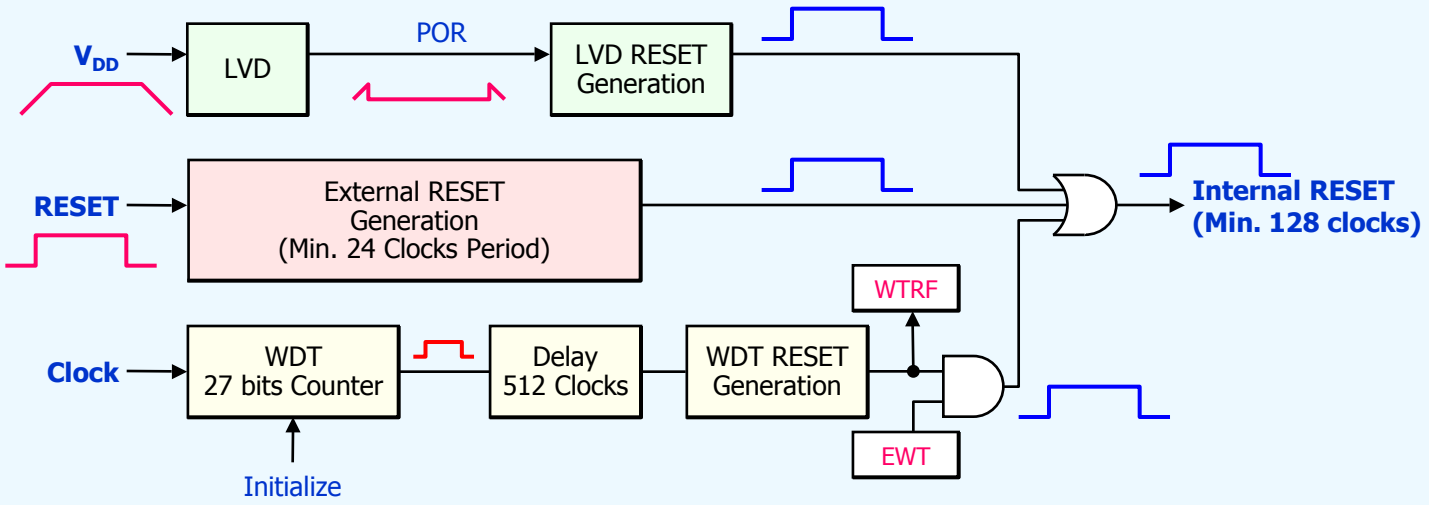
6.13. Reset Circuit : 3 Reset Sources

- LVD(POR) Reset
  - ✓ Power-on Reset when power is turned on.
  - ✓ Power-fail Reset when the supply voltage is below the threshold voltage (V_{RST}).
- External RESET Pin
  - ✓ RESET Pin must be held "H" for min. 24 clocks period.
- WDT Reset : Enable or disable by S/W
- Once triggered by any one of reset sources, the internal reset of MiDAS3.0 remains high for at least 128 clocks.
- Using Reset by External Interrupt(n), Referenced Application Note #023

✓ **WDCON** (D8h) : Watchdog Timer & Power Status Register

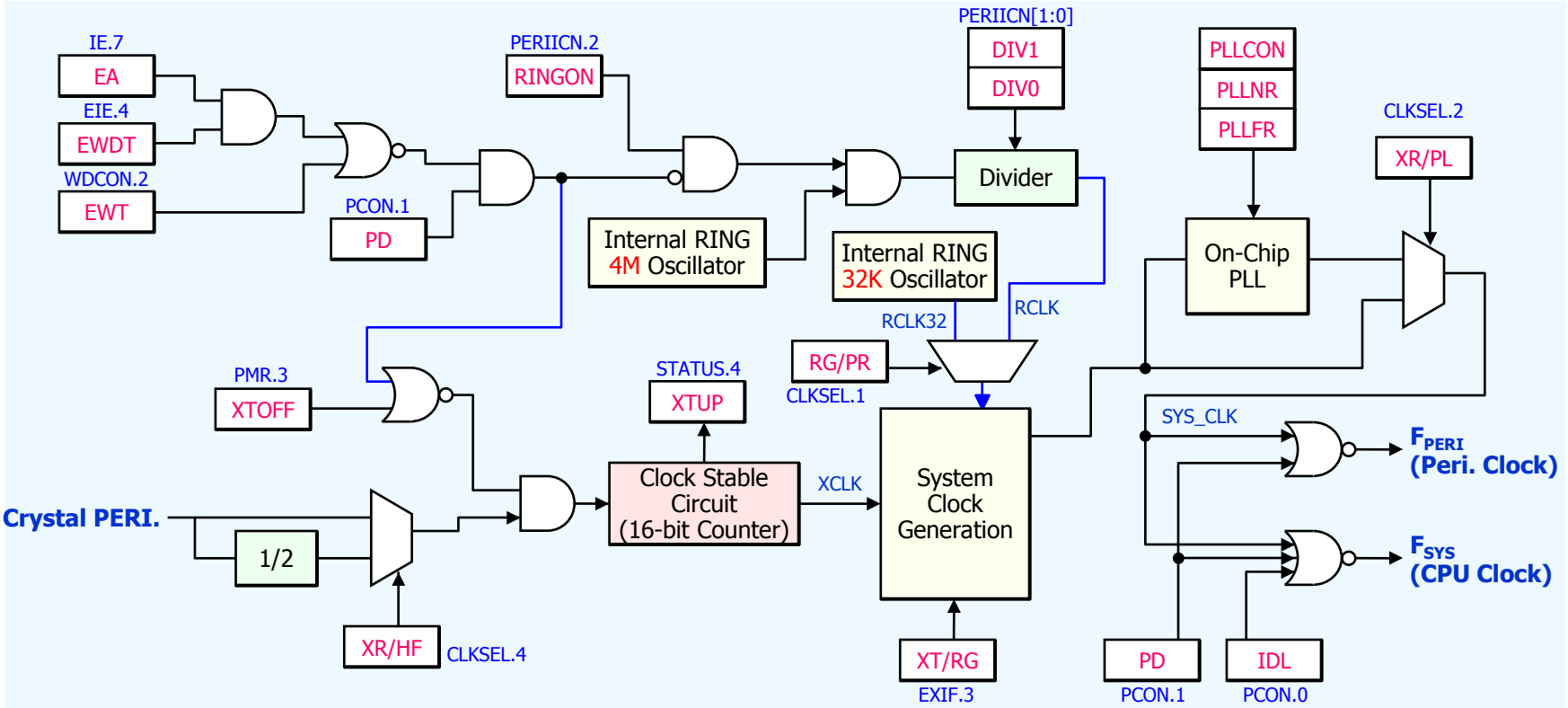
-	POR	EPFI	PFI	WDIF	WTRF	EWT	RWT
	R/W(1)	R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- WTRF : Watchdog Timer Reset Flag.
- EWT : Watchdog Timer Reset Enable.



6.14. Clock Circuit

- System Clock Sources
  - ✓ External Oscillator or Crystal
  - ✓ Internal Ring Oscillator
- Disable of External Clock (Crystal or External Oscillator)
  - ✓ If XTOFF is set.
  - ✓ When MCU is in stop mode and WDT is not active.
- Disable of the Internal RING Oscillator
  - ✓ If RINGON is cleared.
  - ✓ When MCU is in stop mode and WDT is not active.
- Wake-up from stop by WDT
  - ✓ WDT is active in stop mode if EWT is set or WDT interrupt is enabled.
  - ✓ In this case, the clock of WDT is alive during stop mode.



6.14. Clock Circuit : SFRs

✓ **IE** (A8h) : Interrupt Enable Register

EA	EADC	ET2	ES	ET1	EX1	ET0	EX0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- EA : Global interrupt enable

✓ **EIE** (E8h) : Extended Interrupt Enable Register

EPCA1	EPCA0	ES1	EWDT	EX5	EX4	EX3	EX2
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- EWDT : Watchdog timer interrupt enable

✓ **PCON** (87h) : Extended Interrupt Enable Register

SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL
R/W(0)	R/W(0)		R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- PD : Power-down (Stop) mode enable.
- IDL : IDL mode enable

✓ **EXIF** (91h) : External Interrupt Flag Bit Register

IE5	IE4	IE3	IE2	XT/RG	RGMD	RGSL	BGS
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(1)	R(0)	R/W(0)	R/W(1)

- XT/RG : System clock selection.
  0 = Internal RING Oscillator is selected as system clock.
  1 = External clock is selected as system clock.

✓ **PMR** (C4h) : Power Management Control Register

-	-	-	-	XTOFF	ALEOFF	WCLKE	WIOE
				R/W(0)	R/W(0)	R/W(0)	R/W(0)

- XTOFF : 1 = External crystal Oscillator disable.
  0 = External crystal will restart (Default).

✓ **STATUS** (C5h) : Crystal Status Register

-	-	-	XTUP	-	-		-
			R(1)				

- XTUP : Crystal Oscillator warm-up status.
  It represents if the crystal clock is stable(1) or not(0).
  Cleared by H/W if XTOFF is set or if PD is set and WDT is not enabled.
  Set by H/W after crystal stabilization time.

✓ **OSCICN** (C6h) : Internal RING Oscillator Control Register

-	-	-	-	DIV2	RINGON	DIV1	DIV0
			-	R/W(0)	R/W(1)	R/W(0)	R/W(0)

- RINGON : 1 = Internal ring Oscillator is running.
  0 = Internal ring Oscillator is killed.
  Don't clear RINGON bit when XTRG = 0.
- DIV[2:0] : Ring Oscillator divider. (F_{OSC} : 12MHz)
  [0,0,0] = $F_{OSC}/3$
  [0,0,1] = $F_{OSC}/6$
  [0,1,0] = $F_{OSC}/12$
  [0,1,1] = $F_{OSC}/24$
  [1,0,0] = $F_{OSC}/1$
  [1,0,1] = $F_{OSC}/2$
  [1,1,0] = $F_{OSC}/4$
  [1,1,1] = $F_{OSC}/8$

6.14. Clock Circuit : PLL SFRs

✓ **CLKSEL** (FBh) : Clock Selection

-	-	-	XR/HF	WDEM	XR/PL	RG/PR	OSC32EB
-	-	-	R/W(0)	R/W(0)	R/W(1)	R/W(1)	R/W(0)

- XT/HF : XTAL division flag
  [0] : XTAL bypass
  [1] : XTAL/2 division
- XR/PL : PLL clock / XTRG clock selection
  [0] : PLL clock
  [1] : XTAL / RING mux clock
- RG/PR : Ring clock selection.
  [0] : 32KHz ring clock for WDT power down.
  [1] : 4MHz ring clock for normal operation.

✓ **WDCON** (D8h) : Watchdog Timer & Power Status Register

-	POR	EPFI	PFI	WDIF	WTRF	EWT	RWT
	R/W(1)	R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- EWT : Watchdog timer reset enable

- On-Chip PLL
- Support Max. 100MHz Operating Frequency
- Support Lock Detection
- 1.8V Process

✓ **PLLCON** (C1h) : PLL Control Register

LOCK	-	icp1	icp0	Dly_ctr	Ph_sel	PLLPD	PLLBP
R (0)		R/W(0)	R/W(1)	R/W(1)	R/W(0)	R/W(1)	R/W(0)

- PLLBP : [1] : PLL Bypass Mode (Input ☐ Output)
  [0] : PLL Normal Mode
- PLLPD : [1] : PLL Power Down
  [0] : PLL Active
- Ph_sel : PFD phase control
- Dly_ctr : PFD delay control
- icp[1:0] : CP current control
- LCOK : [1] : PLL Lock
  [0] : PLL unlock

✓ **PLLNR** (C2h) : PLL Input Divider Register

-	-	-	-	Odiv1	Odiv0	Rdiv1	Rdiv0
-	-	-	-	R/W(1)	R/W(0)	R/W(1)	R/W(0)

- Rdiv[1:0] : Input 2-bit divider
- Odiv[1:0] : Output 2-bit divider

✓ **PLLFR** (C3h) : PLL Feedback Divider Register

F7	F6	F5	F4	F3	F2	F1	F0
R/W (0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- F[7:0] : Feedback 8-bit divider

6.14. Clock Circuit : PLL Mode

- PLL Operating Mode

Mode	Condition		Description
	PD	BP	
Power Down	1	-	Power down mode disables the PLL and pulls the output clock low
Bypass	0	1	Bypass mode enables some of the block in PLL and let the R-divider output directly go out
Normal	0	0	the PLL is fully enabled

- PLL Frequency Calculation

$$Fsys = F_{VCO} / O_{DIV} = (N_{DIV} \times F_{COMP}) / O_{DIV} = (N_{DIV} \times F_{REF}) / (O_{DIV} \times R_{DIV})$$

- PLL Parameter

Rdiv[1:0]	R_{DIV}
00	1
01	2
10	4
11	8

Odiv[1:0]	O_{DIV}
00	1
01	2
10	4
11	8

Ndiv[7:0]	N_{DIV}
00000000	0
00000001	1
00000010	2
00000011	3
…	…
11111101	253
11111110	254
11111111	255

Minimum N_{DIV} = 4

6.14. Clock Circuit : Fvco , Fsys Range

- Fvco range is between 70 MHz and 130 MHz
- Fsys range is between 8.75 MHz and 100 MHz
  - ✓ **Fvco** = Ndiv * Fcomp = **70 ~ 130 MHz**
  - ✓ **Fsys** = Fvco / Odiv = **8.75 ~ 100 MHz**

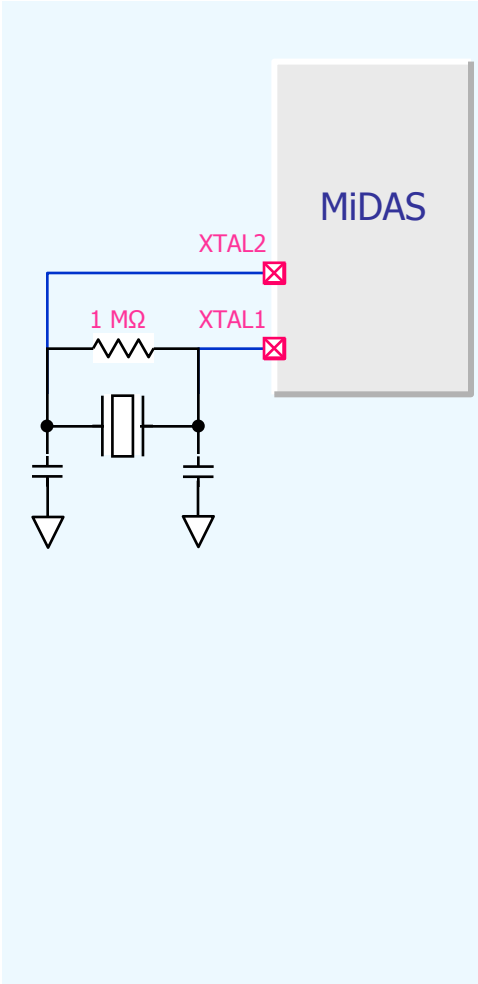
ex) Fref = 10 MHz , Rdiv = 4 , Odiv = 1 , Ndiv = 0x20
Fsys = (Ndiv * Fref) / (Rdiv * Odiv)
= (0x20 * 10 MHz) / (4 * 1) = 80 MHz

Fref : 10 MHz				
Rdiv [1:0]	**Ndiv[7:0] range**	**Fvco range [MHz]**	**Odiv [1:0]**	**Fsys range [MHz]**
1 (00)	0x07 ~ 0x0D	70 ~ 130	1 (00)	70 ~ 100
			2 (01)	35 ~ 65
			4 (10)	17.5 ~ 32.5
			8 (11)	8.75 ~ 16.25
2 (01)	0x0D ~ 0x1A	70 ~ 130	1 (00)	70 ~ 100
			2 (01)	35 ~ 65
			4 (10)	17.5 ~ 32.5
			8 (11)	8.75 ~ 16.25
4 (10)	0x1C ~ 0x34	70 ~ 130	1 (00)	70 ~ 100
			2 (01)	35 ~ 65
			4 (10)	17.5 ~ 32.5
			8 (11)	8.75 ~ 16.25
8 (11)	0x38 ~ 0x68	70 ~ 130	1 (00)	70 ~ 100
			2 (01)	35 ~ 65
			4 (10)	17.5 ~ 32.5
			8 (11)	8.75 ~ 16.25

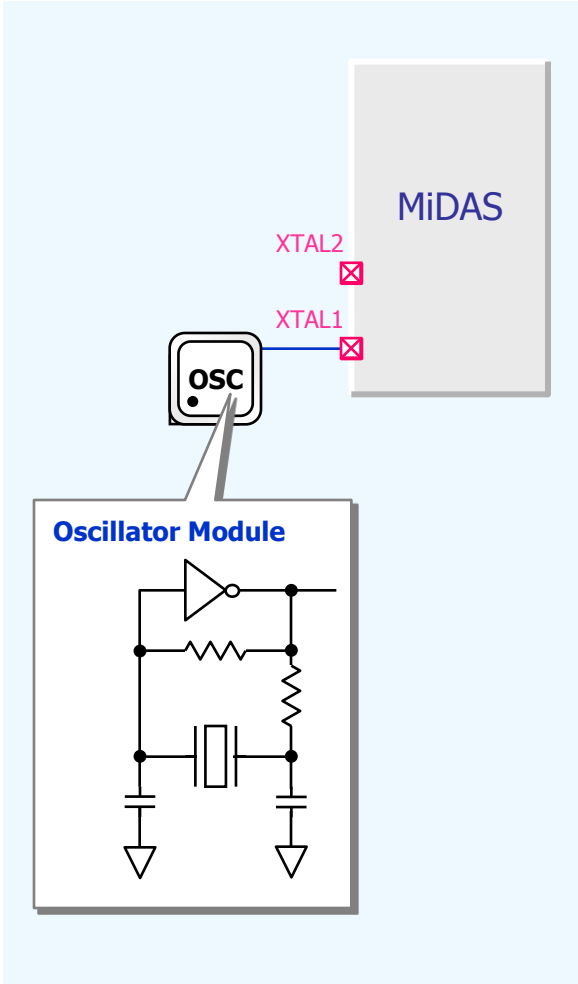
Fref : 20 MHz				
Rdiv [1:0]	**Ndiv[7:0] range**	**Fvco range [MHz]**	**Odiv [1:0]**	**Fsys range [MHz]**
1 (00)	0x04 ~ 0x06	70 ~ 130	1 (00)	70 ~ 100
			2 (01)	35 ~ 65
			4 (10)	17.5 ~ 32.5
			8 (11)	8.75 ~ 16.25
2 (01)	0x07 ~ 0x0D	70 ~ 130	1 (00)	70 ~ 100
			2 (01)	35 ~ 65
			4 (10)	17.5 ~ 32.5
			8 (11)	8.75 ~ 16.25
4 (10)	0x0D ~ 0x1A	70 ~ 130	1 (00)	70 ~ 100
			2 (01)	35 ~ 65
			4 (10)	17.5 ~ 32.5
			8 (11)	8.75 ~ 16.25
8 (11)	0x1C ~ 0x34	70 ~ 130	1 (00)	70 ~ 100
			2 (01)	35 ~ 65
			4 (10)	17.5 ~ 32.5
			8 (11)	8.75 ~ 16.25

6.14. Clock Circuit : Guideline for Configuration

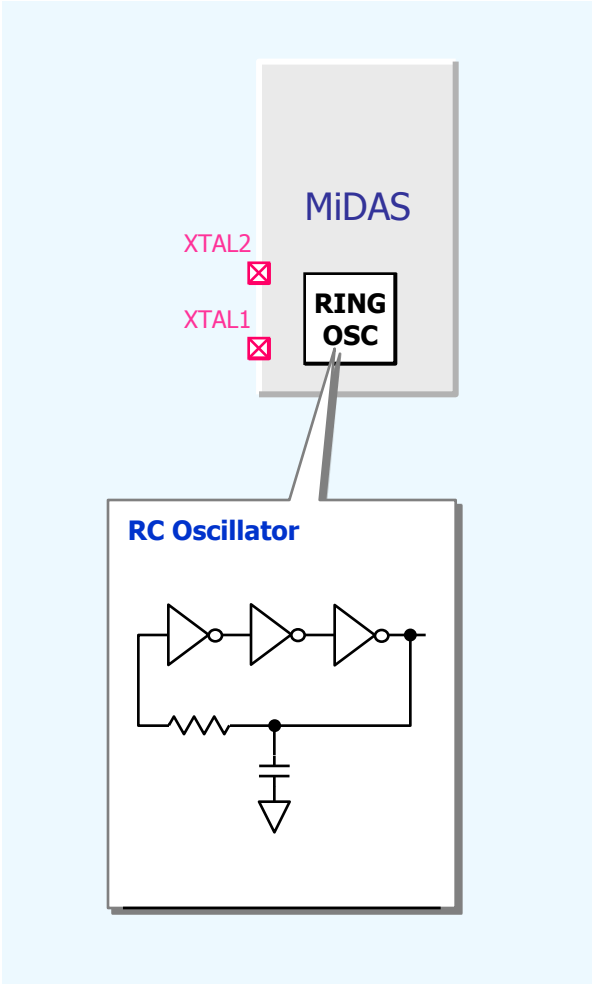
◆ **Crystal Oscillator**



◆ **Oscillator Module**



◆ **Internal Ring Oscillator**



6.15. Power Management : 3 Modes

- Active Mode : The CPU and The Peripherals operate.
- Idle Mode : The CPU is gated off from the clock signal. Only the Peripherals operate.
  - ✓ Wake-up by activating any interrupt. The CPU resumes.
  - ✓ Wake-up by activating any reset. The CPU restarts..
- Stop Mode : The CPU and Peripherals are stopped.
  - ✓ Wake-up by activating external interrupt 0 or 1 (level detect) The CPU resumes.
  - ✓ Wake-up by activating all kinds of resets. CPU restarts.
  - ✓ Wake-up by activating WDT interrupt or reset. If WDT remains enabled, either the crystal Oscillator or the ring Oscillator will operate during the stop mode.
  - ✓ To prevent malfunction of I/O ports during wake-up, it is recommended to execute the NOP instruction twice after the PD bit of PCON is set to 1.

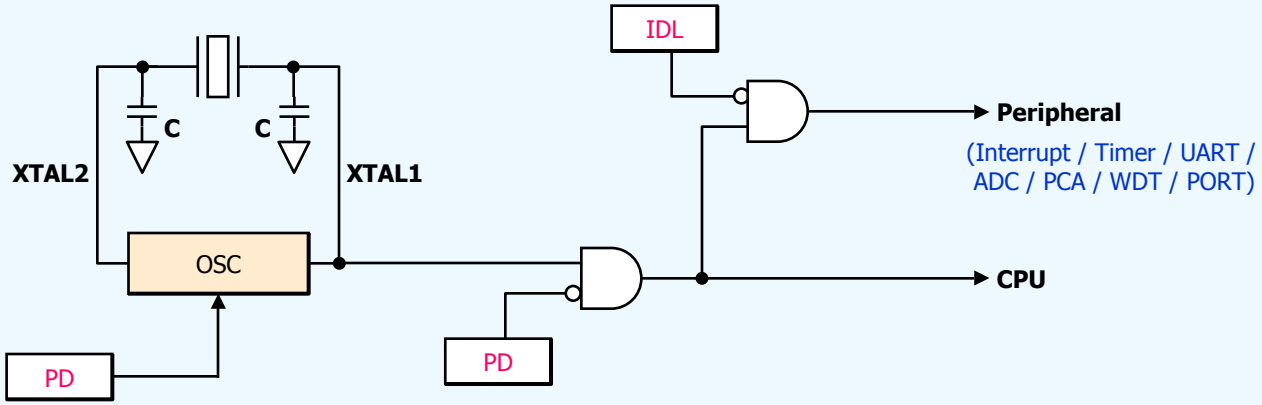
✓ **PCON** (87h) : Power Control Register

SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL
R/W(0)	R/W(0)		R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- PD : Stop Mode (Power-down) Enable.
- IDL : IDLE Mode Enable.

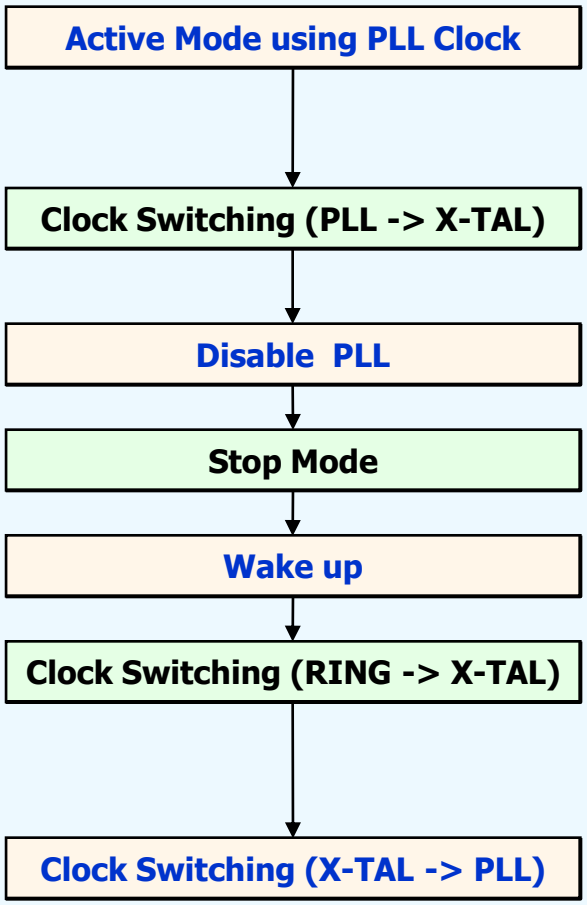
Wake-up from stop mode

- ✓ The crystal Oscillator was used before invoking stop mode and WDT is disabled : External interrupt signals must be held '0' for at least (2^{16} + 8) clock cycles. The internal MCU clocks will be activated after the 16-bit crystal stabilization counter overflows.
- ✓ An User set RGSL(EXIF.1) bit. It enables the MCU immediately to wake up using the internal ring Oscillator. After the stabilization counter overflows, XTAL clock will be available again.
- ✓ The ring Oscillator is available without stabilization. In this case, external interrupt signals should be held '0' is for at least 8 clock cycles, implemented by executing the NOP instruction twice, to enter the interrupt service routine.



6.15. Power Management : Example

- Example : How to use Power Down Mode When PLL Clock used




```
PLLNR = 0x01;                   // RDIV=1,ODIV=0
PLLFR = 0x08;                   // 08 : 80 Mhz @ 22.1184 Mhz
PLLCON &= 0xFD;                 // PLL ON
while(!(PLLCON & 0x80));        // PLL Lock Check
CLKSEL &= 0xFB;                 // Clock Switch : XTAL -> PLL Clock
```

```
CLKSEL |= 0x02;                 // 4Mhz ring clock Selection
EXIF |= 0x08;                   // X-TAL clock Select
EXIF &=0xFE;                    // LVD OFF
```

```
CLKSEL = 0x04;                  // X-TAL/RING Clock
PLLCON = 0x1A;                  // PLL clock Power Down(Kill)
```

```
PCON = 0x02;                    // Stop mode
```

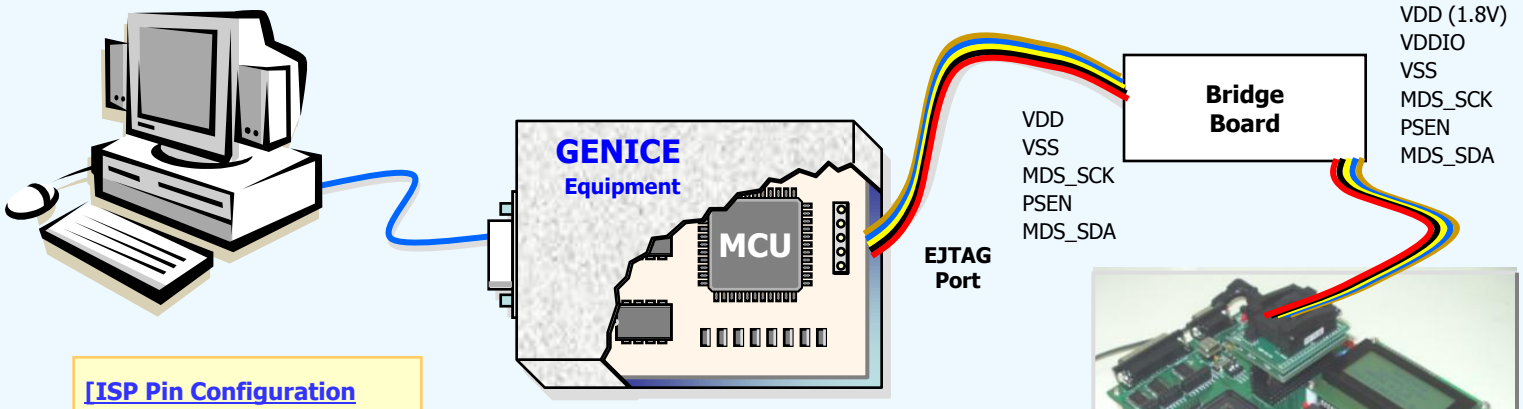
```
/* Wake up By INT0 or INT1 */
```

```
EXIF = 0x00;                    // Internal Oscillator Select
CLKSEL = 0x06;                  // XTAL/RING Clock Select
                                // 4MHz ring clock
while(!(STATUS&0x10));          // Stable XTAL Clock Check
EXIF = 0x08;                    // Clock X-TAL Clock Select
```

```
PLLNR = 0x01;                   // RDIV=1,ODIV=0
PLLFR = 0x08;                   // 08 : 80 Mhz @ 22.1184 Mhz
PLLCON &= 0xFD;                 // PLL ON
while(!(PLLCON & 0x80));        // PLL Lock Check
CLKSEL &= 0xFB;                 // Clock Switch : XTAL -> PLL Clock
```

6.16. ISP (In-System Programming)

- Code memory (62KBytes) can be programmed using EJTAG in target system.
- EEPROM (2KBytes) can be programmed using EJTAG in target system.
- EJTAG Port
  - ✓ VDD(+1.8V), VDDIO(+3.3V), VSS, MDS_SCK, PSEN, MDS_SDA



[ISP Pin Configuration In GenICE52/MiDAS3.0]

- V_{DD} (+1.8V)
- V_{DDIO} (+3.3V)
- V_{SS} (GND)
- SCK
- PSEN
- SDA

※ You should connect VDDIO and VDD using MiDAS 3.0

6.16. ISP : Command Set

Command	Function
Blank	◆ Check the blank status of the device currently connected.
Erase Chip	◆ Erases the device's memory.
	◆ Performs an erase chip, the device's memory, both code and data. • Code : Flash • User data : EEPROM • Information data : Lock bits, RING option, PGM/ERS time (ISP & Parallel)
	◆ The device will be blank and in a programmable state.
Read Code/EEPROM	◆ Reads in the device's memory.
	◆ The results from the read are loaded into the CORERIVER ISP software's buffer and displayed on the screen.
Write Chip/EEPROM	◆ Writes all memory locations in the CORERIVER ISP software's buffer out to the device's memory.
Verify Chip	◆ Compares the CORERIVER ISP software buffer with the device's internal memory.
	◆ If the buffers are found to be exact replicas of the device's memory, a success result is returned.
	◆ If there are any differences, a failure result is returned along with the total number of mismatched bytes.

6.17. IAP (In-Application Programming)

- IAP function is provided for the applications which need to save operation data/status in nonvolatile memory (on-chip EEPROM) or to update application code (on-chip FLASH) by itself.
  - ✓ Code memory(62KB) can be programmed or erased during the operation of MCU.
  - ✓ EEPROM(2KB) can be programmed or erased during the operation of MCU.
- Program/Erase time
  - ✓ Program : 50us except for IAP code execution time.
  - ✓ Erase : 10ms except for IAP code execution time.
- Program/Erase unit
  - ✓ Program : 1 byte
  - ✓ Erase : 1 sector (512 bytes)
- IAP SFR
  - ✓ FAEN : IAP routine Access Enable (default value = 0x00)

✓ **FAEN** (F7h) : IAP Routine Access Enable Register

-	-	-	-	-	-	-	FALSH_AEN
							R/W(0)

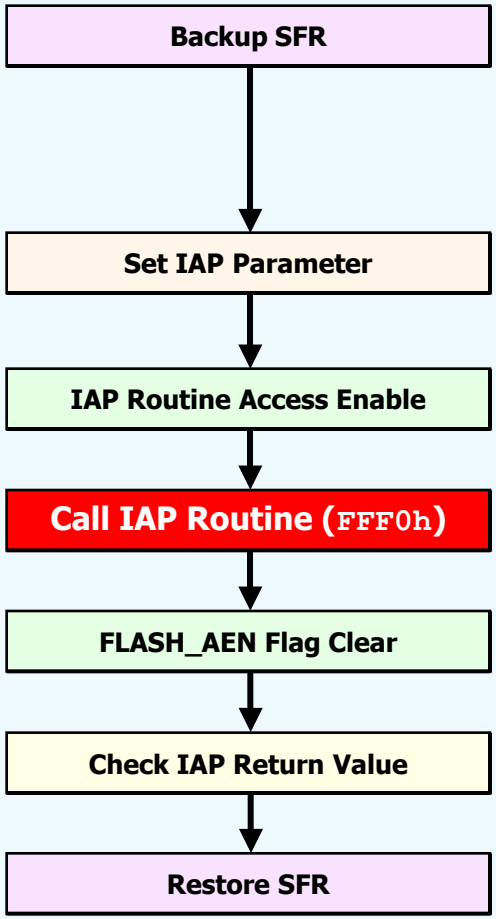
- FLASH_AEN : IAP Routine Access Enable

6.17. IAP : Function Set

- IAP call address
  - ✓ FFF0h
- IAP return value
  - ✓ Success : [ACC] 8Xh
  - ✓ Program Fail : [ACC] FCh
  - ✓ Address fail : [ACC] FDh
  - ✓ Lock fail : [ACC] FEh
  - ✓ Command fail : [ACC] FFh
- Before calling IAP function, FLASH_AEN flag in FAEN SFR must be set.
- After executing IAP function, the value of PSW SFR can be changed.
- Any interrupt service routine will not be executed in time since the CPU is suspended for tens of milliseconds during executing an IAP function (Program/Erase).

Call Address	Command	Function	B	ACC	DPTR	Used XRAM Area	Return Value (ACC)
FFF0h	Program	Program Code Byte	3h	Programmed code	Flash address	No	83h/FCh/FDh/FEh/FFh
		Program EEPROM Byte	6h	Programmed data	EEP Address	No	86h/FCh/FDh/FEh/FFh
	Erase	Erase Code Sector	1h	Don't care	Sector Address	No	81h/FDh/FEh/F로
		Erase EEPROM Sector	4h	Don't care	Sector Address	No	84h/FDh/FEh/FFh

6.17. IAP : Coding Flow

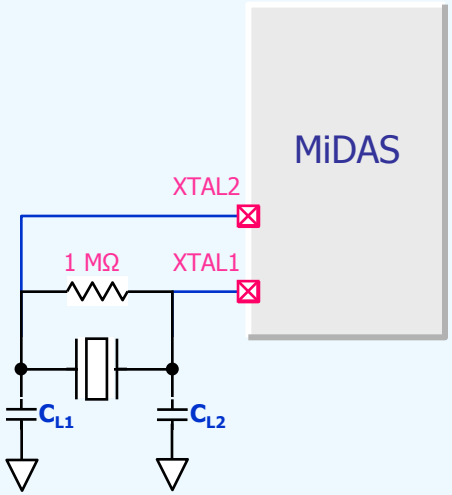


[Example Code : IAP Program for FLASH]

```
PUSH A                      ; backup acc
PUSH B                      ; backup b
PUSH DPL                    ; backup dptr
PUSH DPH
MOV R1, IE                  ; backup IE SFR
CLR IE.7                    ; Interrupt disable

MOV B, #03h                 ; IAP Function setting
MOV A, #55h                 ; Programmed Data
MOV DPTR, #08000h           ; Programmed Address

ORL  EEAEN, #01h            ; IAP routine access enable

CALL FFF0h                  ; Call IAP routine

MOV FAEN, #000h             ; IAP routine access disable

CJNE A, #83h, IAP_FAIL      ; Check return message

MOV IE, r1                  ; restore IE SFR
POP DPH                     ; restore acc, b, dptr
POP DPL
POP B
POP A
```

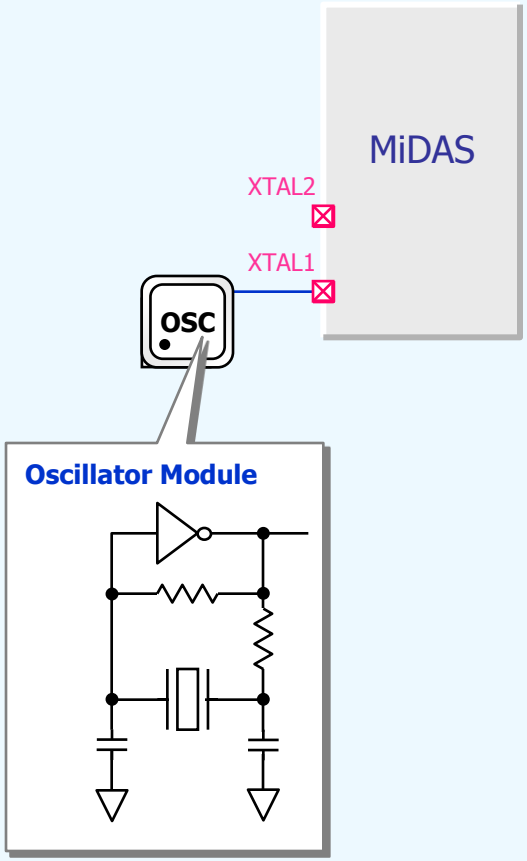
7.1. Clock Circuit : Guideline for Configuration

◆ **Crystal Oscillator**

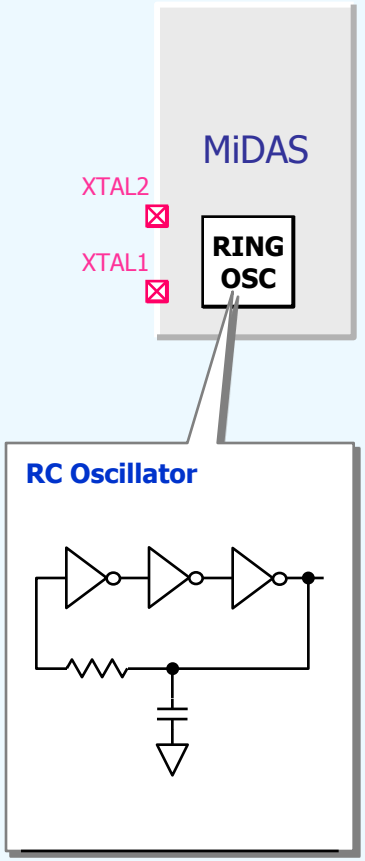


* C_{L1}/C_{L2} Value is refer to the next page

◆ **Oscillator Module**



◆ **Internal Ring Oscillator**



7.2. Clock Circuit : Guideline for Configuration

◆ **Quartz crystal tank circuit parameters**

OSC Freq (MHz)	Part Number	Package	C_{L1}/C_{L2}
2.000 M	TSE	DIP	47pF/47pF
6.144 M	SX061C	DIP	35pF/35pF
8.000 M	TXC 20JDD	SMD	35pF/35pF
8.000 M	RVR 920	SMD	35pF/35pF
8.000 M	TXC P3117	SMD	35pF/35pF
10.000 M	TXC P3116	SMD	30pF/30pF
10.000 M	TXC 32FDG	SMD	30pF/30pF
12.000M	TSE	DIP	30pF/30pF
12.000M	TXC X3041	SMD	30pF/30pF
12.000M	TXC P3111	SMD	30pF/30pF
13.560M	TXC F5X	SMD	30pF/30pF
14.318M	KDS 5L	DIP	30pF/30pF
14.318M	TXC FA02	SMD	30pF/30pF
14.318M	TXC PA106	SMD	30pF/30pF
14.745M	TXC P5118	SMD	30pF/30pF
16.000 M	TXC P3108	SMD	30pF/30pF
16.000 M	TXC F392	DIP	30pF/30pF

OSC Freq (MHz)	Part Number	Package	C_{L1}/C_{L2}
16.000 M	TXC 32KCN	SMD	30pF/30pF
16.384 M	NDK38	DIP	30pF/30pF
17.734 M	TXC XU120	SMD	30pF/30pF
17.734 M	HELE	DIP	30pF/30pF
18.432 M	MGP 9534 40	DIP	30pF/30pF
18.816 M	TXC P5118	SMD	30pF/30pF
20.000 M	TXC P4120	SMD	25pF/25pF
20.000 M	TXC F598	SMD	25pF/25pF
20.000 M	TXC 20FDD	DIP	25pF/25pF
22.118 M	TXC P5117	SMD	25pF/25pF
24.576 M	TXC P3109	SMD	25pF/25pF
24.576 M	TXC X3119	SMD	25pF/25pF
25.000 M	TXC P4119	SMD	25pF/25pF
25.000 M	RAKON	DIP	25pF/25pF
27.000 M	TSE	DIP	25pF/25pF
27.000 M	TXC X5119	SMD	25pF/25pF
28.244 M	TXC P5117	SMD	25pF/25pF

7.3. Clock Circuit : Guideline for Configuration

◆ Ceramic resonator tank circuit parameters

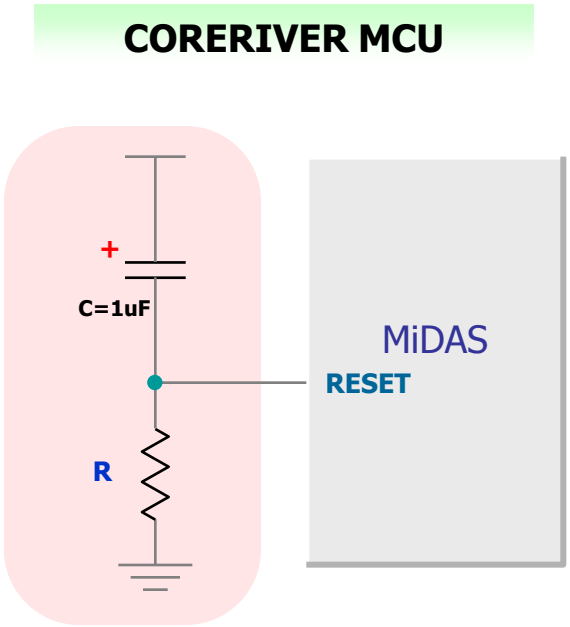
OSC Freq (MHz)	Part Number	Package	Embedded C_{L1}/C_{L2}	External C_{L1}/C_{L2}
2.000 M	CSTCC2.00MG0H6	SMD	47pF/47pF	
2.000 M	CSTCC2.00MG	SMD	15pF/15pF	
3.580 M	CSTCC3.58MG0H6	SMD	47pF/47pF	
3.580 M	CSTCC3.58MG	SMD	15pF/15pF	
4.000 M	CSTRC400MG05	SMD	39pF/39pF	
4.000 M	CSTRC400MG03	SMD	15pF/15pF	
4.194 M	CSTRC0419MG05	SMD	39pF/39pF	
4.194 M	CSTRC0419MG03	SMD	15pF/15pF	
6.000 M	CSTRC0600MG03	SMD	15pF/15pF	
6.000 M	CSTRC0600MG05	SMD	39pF/39pF	
8.000 M	CSTCC8.00MG	SMD	15pF/15pF	
8.000 M	CTCC8.00MG0H6	SMD	47pF/47pF	
10.000 M	CSTCC10.0MG	SMD	15pF/15pF	
10.000 M	CSTCC10.0MG0H6	SMD	47pF/47pF	
12.000 M	CTCV12.0MTJ0C4	SMD	22pF/22pF	
14.318 M	CSTCE14M3V53-R0	SMD	15pF/15pF	
14.318 M	CSTCV14.31MXJ0H4	SMD	22pF/22pF	

OSC Freq (MHz)	Part Number	Package	Embedded C_{L1}/C_{L2}	External C_{L1}/C_{L2}
14.318 M	CSTCV14.3MXJ0H3	SMD	15pF/15pF	
14.725 M	CSTCV14.72MXJ0H4	SMD	22pF/22pF	
14.725 M	CSTCV14.72MXJ0H3	SMD	15pF/15pF	
14.725 M	CSTCE14M7V51001-R0	SMD	5pF/5pF	
16.000 M	CSTCW1600MX03	SMD	15pF/5pF	
16.000 M	CSTCE16M0V51-R0	SMD	5pF/5pF	
16.900 M	CSTCE16M9V51-R0	SMD	5pF/5pF	
18.000 M	CSTCW1800MX03	SMD	15pF/15pF	
20.000 M	CSTCW2000MX03	SMD	15pF/15pF	
20.000 M	CSTCG20M0V51-R0	SMD	5pF/5pF	
22.579 M	CSTCW2257MX03	SMD	15pF/15pF	
24.000 M	CSTCW2400MX03	SMD	15pF/15pF	
25.000 M	CSTCW2500MX03	SMD	6pF/6pF	
25.000 M	CSACW25M0X51-R0	SMD		6pF/6pF
27.000 M	CSACW27M0X51-R0	SMD		6pF/6pF
27.000 M	CSTCW2700MX01	SMD	6pF/6pF	

8.1. Recommended External POR

- Recommendation of the value of Resistor R according to the external clock frequency

  - 10 KOhms for higher than 4MHz frequency
  - 100 KOhms for lower than 4MHz frequency



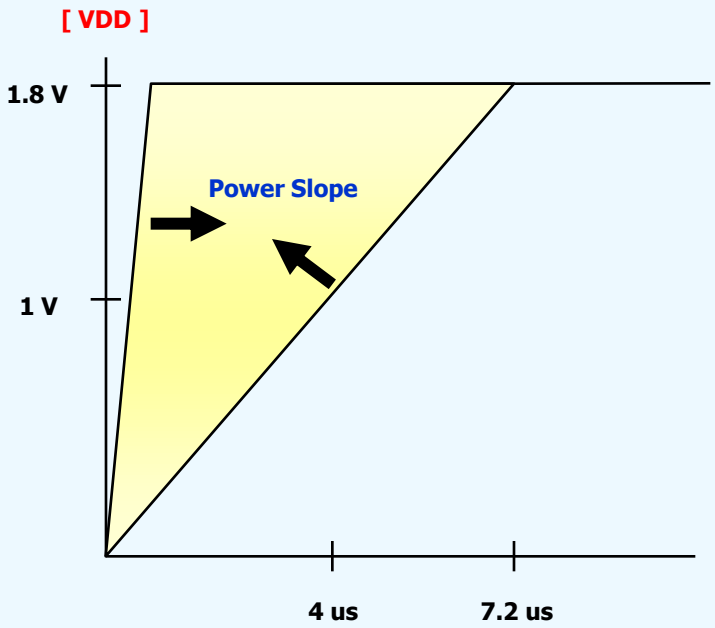
External POR Circuit

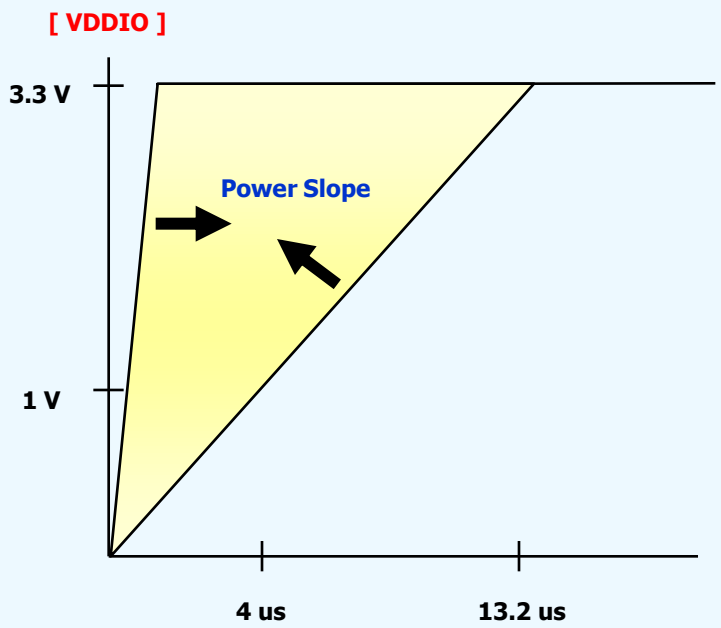
Table 1

Frequency	4MHz < F_{req}	4MHz ≥ F_{req}
R	**100 kOhms**	**10 kOhms**

8.2. Recommended Power Slope

- If using internal POR, you must meet the condition below.
- The supply voltage slope must be steeper than 1.0V/4us. (VDD : 1.8V/7.2us , VDDIO : 3.3V/13.2us)
  (Additionally, the supply voltage should be increasing monotonically until it reaches to the normal range.)





9. Absolute Maximum Ratings

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}	DC supply voltage	- 0.3 to 1.98	V
V_{DDIO}	DC IO supply voltage	- 0.3 to 3.6	V
V_{IN}	DC input voltage	-0.3 to 5.5	V
I_{IN}	DC input current	±10	mA
T_{STG}	Storage temperature	-40 to 125	°C

Recommended Operating Conditions

Symbol	Parameter	Rating	Unit
V_{DD}	DC supply voltage	1.62 to 1.98	V
V_{DDIO}	DC IO supply voltage	3.0 to 3.6	V
T_A	Industrial temperature range	-20 to 85	°C

Notes

- ✓ All electrical characteristics are applied to digital cell blocks without any analog core.

Caution

- ✓ When VDDIO use 3.3V Voltage and 5V input signal comes in input port, VDDIO Voltage Level will be able to change
- ✓ VDDIO Voltage Level changed, Internal Functions will be able to wrong operation.

10. DC Characteristics (Normal I/O)

*** TA = = -20 ºC ~ +85 ºC, V_{DDIO} = 2.7V ~ 3.6V unless otherwise specified.**

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min.	Typ.	Max.	
Input Low Voltage	V_{IL1}	RESETB,P0, P1,P2,P3	V_{DDIO} = 1.68V~3.6V	-0.5	-	$0.2V_{DDIO}$-0.1	V
Input high Voltage	V_{IH1}	P0, P1,P2,P3,RESETB	V_{DDIO} = 1.68V~3.6V	$0.2V_{DDIO}$+1.0	-	V_{DDIO}+0.5	V
Output Low Voltage	V_{OL}	ALL pin	I_{OL} = 20mA @V_{DDIO}=3.3V	-	-	$0.3V_{DDIO}$	V
Output High Voltage	V_{OH}	ALL pin	I_{OH} = -15mA @V_{DDIO}=3.3V	$0.7V_{DDIO}$	-	-	V
	V_{OHP}	Pull-up	I_{OH}= -10uA @V_{DDIO}=3.3V	$0.7V_{DDIO}$	-	-	V
Input Leakage Current	I_{IL}	All pins except XTAL1,XTAL2	V_{IN} = V_{IH} or V_{IL}	-	-	±1	μA
Pin Capacitance	C_{IO}	All	V_{DDIO} = 3.3V	-	10	-	pF

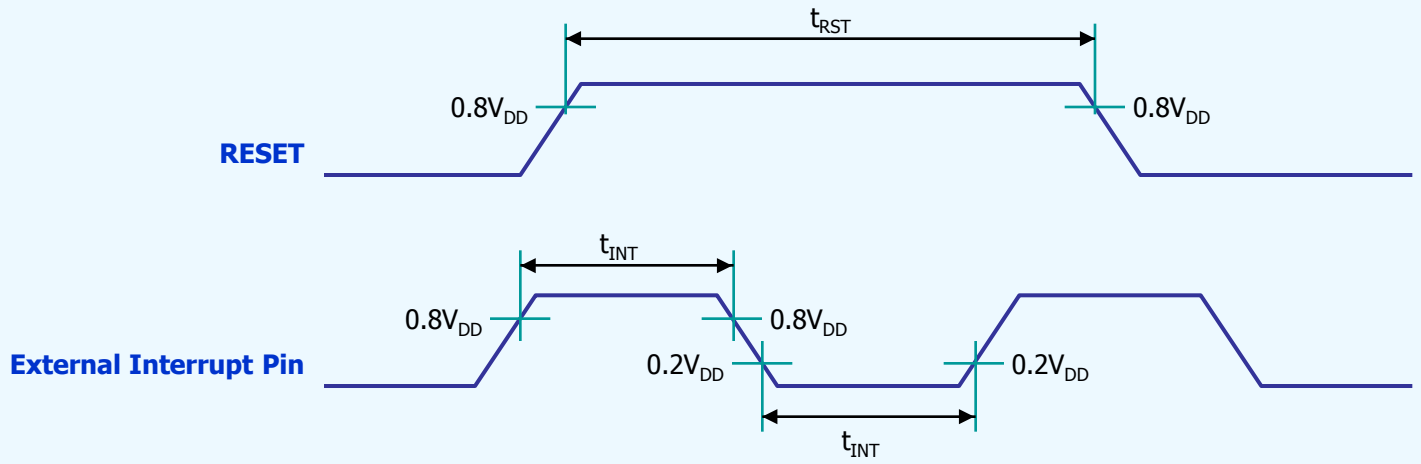
◆ PLL Clock DC Characteristic

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Input Frequency	Fref	2	-	40	MHz	
Comparison Frequency	Fcomp	2	10	20	MHz	Fcomp=Fref / Rdiv
VCO Frequency	**Fvco**	**70**	**100**	**130**	**MHz**	**Fvco = Ndiv * Fcomp**
Output System clock Frequency	**Fsys**	**8.75**	**-**	**100**	**MHz**	**Fsys = Fvco / Odiv**

11. AC Characteristics

*** T_A = -20 ºC ~ +85 ºC unless otherwise specified.**

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min.	Typ.	Max.	
Operating Frequency	F_{OSC}	XTAL1, XTAL2	V_{DDIO} = 3.3V ± 10%	-	-	40	MHz
RESET Input Width	t_{RST}	RESET	V_{DDIO} = 3.3V ± 10%	24	-	-	F_{OSC}
External Interrupt Input Width	t_{INT}	External Interrupt	V_{DDIO} = 3.3V ± 10%	4	-	-	F_{OSC}



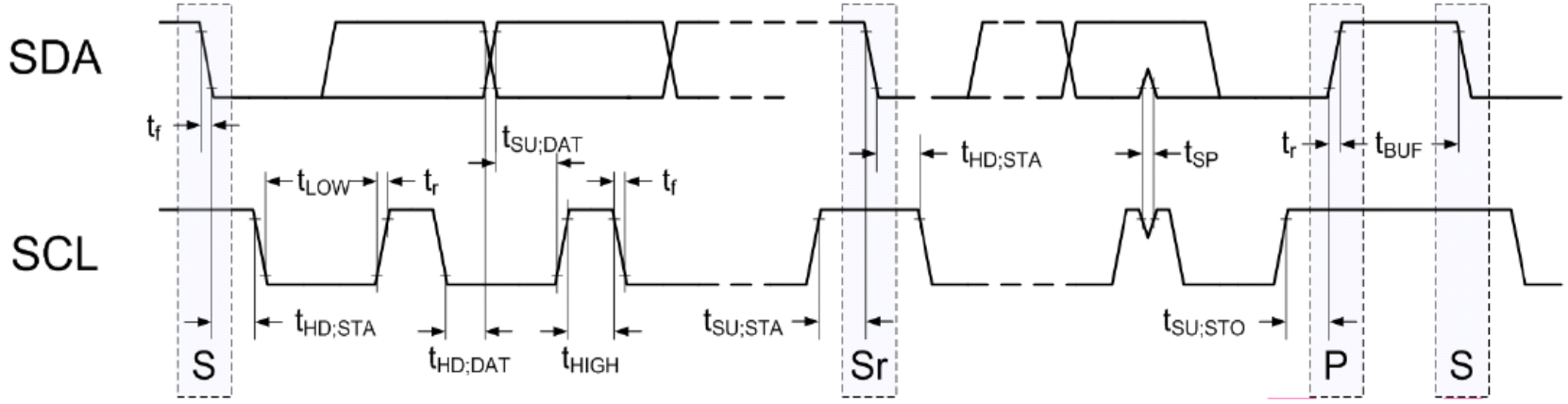
12. ADC Characteristics

Parameter		Symbol	Conditions	Value			Unit
				Min.	Typ.	Max.	
Supply Voltage		V_{DDADC}	-	1.68	-	3.3	V
Input Voltage		V_{INADC}	-	V_{SSIO}	-	V_{DDIO}	V
Resolution		RES_{ADC}	-	-	10	-	bit
Operating Frequency		F_{ADC}	V_{DDIO} = 3.0V ~ 3.6V V_{DDIO} = 1.68V ~ 1.92V	-	-	10 5	MHz
Conversion Time		t_{ADC}	-	-	96 / F_{ADC}	-	s
Overall Accuracy		OA_{ADC}	V_{DDIO} =3.3V, F_{ADC}=10MHz V_{DDIO} =1.8V, F_{ADC}=5MHz	-	±2	±4	LSB
Integral Nonlinearity		INL_{ADC}	V_{DDIO} =3.3V, F_{ADC}=10MHz V_{DDIO} =1.8V, F_{ADC}=5MHz	-	±2	±4	LSB
Differential Nonlinearity		DNL_{ADC}	V_{DDIO} =3.3V, F_{ADC}=10MHz V_{DDIO} =1.8V, F_{ADC}=5MHz	-	±0.5	±1	LSB
Zero Input Error		ZIE_{ADC}	V_{DDIO} =3.3V, F_{ADC}=10MHz V_{DDIO} =1.8V, F_{ADC}=5MHz	-	±2	±4	LSB
Full Scale Error		FSE_{ADC}	V_{DDIO} =3.3V, F_{ADC}=10MHz V_{DDIO} =1.8V, F_{ADC}=5MHz	-	±2	±4	LSB
Analog Input Capacitance		C_{INADC}	-	-	10	15	pF
ADC Current	Active	I_{ADC}	V_{DDIO} = 3.3V, F_{ADC}=10MHz	-	1	2	mA
			V_{DDIO} = 1.8V, F_{ADC}=5MHz	-	0.3	0.6	
	Power-down		V_{DDIO} = 3.3V	-	-	100	nA

13. I2C Signal Characteristics

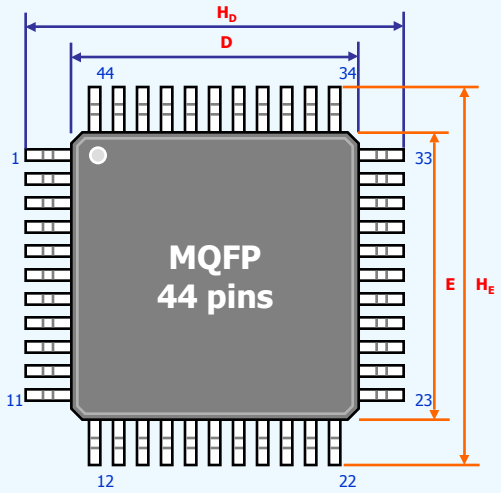
Symbol	Description	Value		Unit
		Min.	Max.	
F_{SCL}	SCL Clock frequency	0	400	kHz
t_{LOW}	LOW period of the SCL Clock	1.3	-	us
t_{HIGH}	HIGH Period of the SCL Clock	0.6	-	us
t_r	Rise Time of both SDA and SCL signals	20+0.1 C_b	300	ns
t_f	Fall time of both SDA and SCL signals	20+0.1 C_b	250	ns
$t_{HD;STA}$	Hold time START condition	0.6	-	us
$t_{SU;STO}$	Set-up time for STOP condition	0.6	-	us
$t_{HD;DAT}$	Data hold time	0	0.9	us
$t_{SU;DAT}$	Data set-up time	100	-	ns
$t_{SU;STA}$	Set-up time for a repeated START condition	0.6	-	us

C_b = Capacitance of one bus line in pF.



S : Start Condition / Sr : Repeated Start Condition / P : Stop Condition

14. Package Dimensions : 44-MQFP

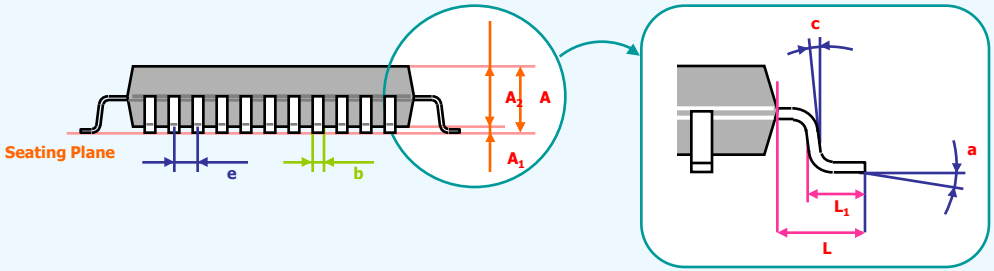


[44-MQFP]

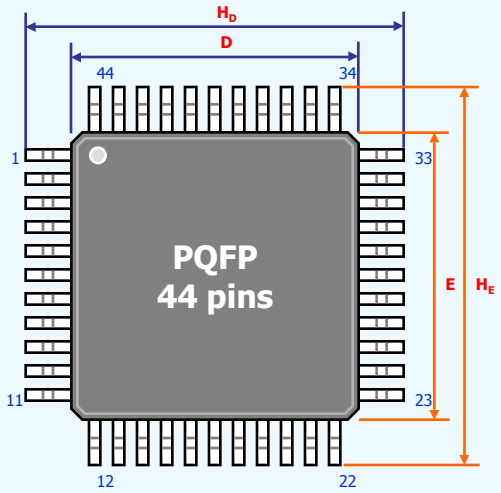
Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.091	-	-	2.30
A_1	0.002	-	0.006	0.05	-	0.15
A_2	0.077	0.081	0.085	1.95	2.05	2.15
b	0.012	0.015	0.018	0.30	0.37	0.45
D	0.394 BSC			10.00 BSC		
E	0.394 BSC			10.00 BSC		
e	0.031 BSC			0.80 BSC		
H_D	0.520 BSC			13.20 BSC		
H_E	0.520 BSC			13.20 BSC		
L	-	0.063	-	-	1.60	-
L_1	0.024	0.031	0.039	0.60	0.80	1.00
a	0°	-	8°	0°	-	8°
c	0°	-	-	0°	-	-

Notes:

1. Dimension D * E do not include interlead flash.
2. Controlling dimension: Inches
3. General appearance spec. should be based on final visual inspection spec.



14. Package Dimensions : 44-PQFP

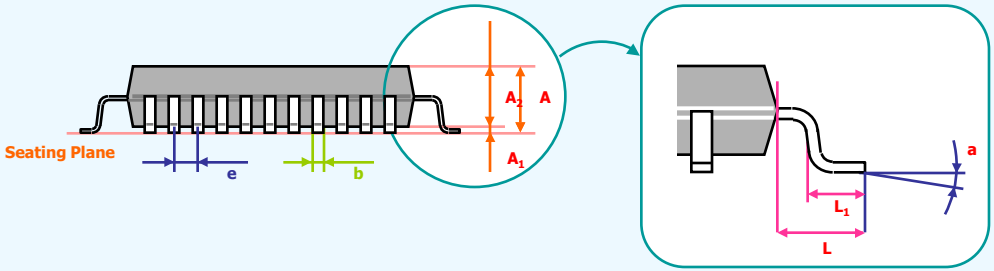


[44-PQFP]

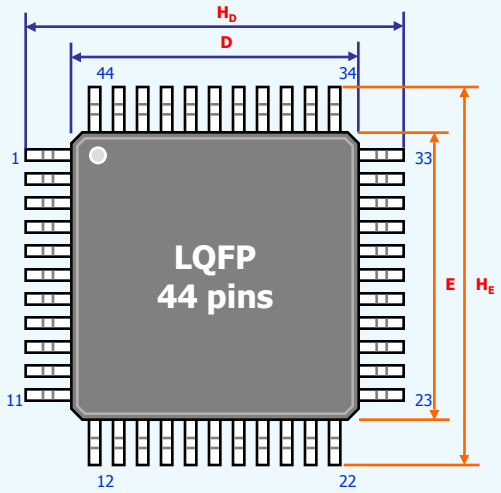
Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.091	-	-	2.30
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.079	0.083	0.087	2.00	2.10	2.20
b	0.011	-	0.015	0.29	-	0.37
D	0.386	0.394	0.402	9.80	10.00	10.20
E	0.386	0.394	0.402	9.80	10.00	10.20
e	0.031			0.80 BSC		
H_D	0.535	0.543	0.551	13.60	13.80	14.00
H_E	0.535	0.543	0.551	13.60	13.80	14.00
L	-	0.075BSC	-	-	1.90BSC	-
L_1	0.033	0.039	0.045	0.85	1.00	1.15
a	0°	-	8°	0°	-	8°

Notes:

1. Dimension D * E do not include interlead flash.
2. Controlling dimension: Inches
3. General appearance spec. should be based on final visual inspection spec.



14. Package Dimensions : 44-LQFP

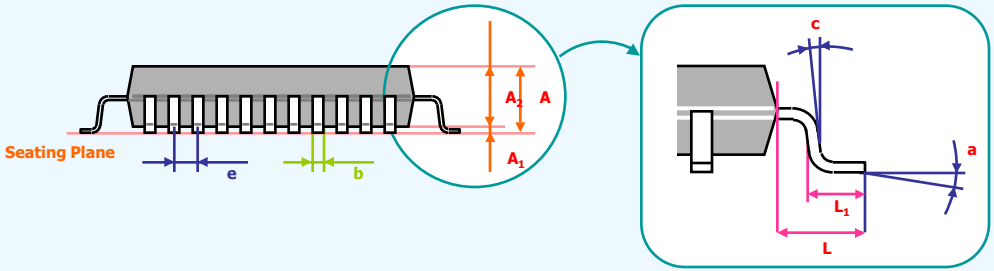


[44-LQFP]

Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.055	-	0.063	1.40	-	1.60
A_1	0.002	-	0.006	0.05	-	0.15
A_2	0.053	-	0.057	1.35	-	1.45
b	0.007	0.009	0.011	0.17	0.22	0.27
D	0.390	0.394	0.398	9.90	10.00	10.10
E	0.390	0.394	0.398	9.90	10.00	10.10
e	0.0315 BSC			0.80 BSC		
H_D	0.463	0.471	0.482	11.75	12.00	12.25
H_E	0.463	0.471	0.482	11.75	12.00	12.25
L	-	0.039	-	-	1.00	-
L_1	0.018	-	0.029	0.45	-	0.75
A	0°	-	7°	0°	-	7°
c	0°	-	-	0°	-	-

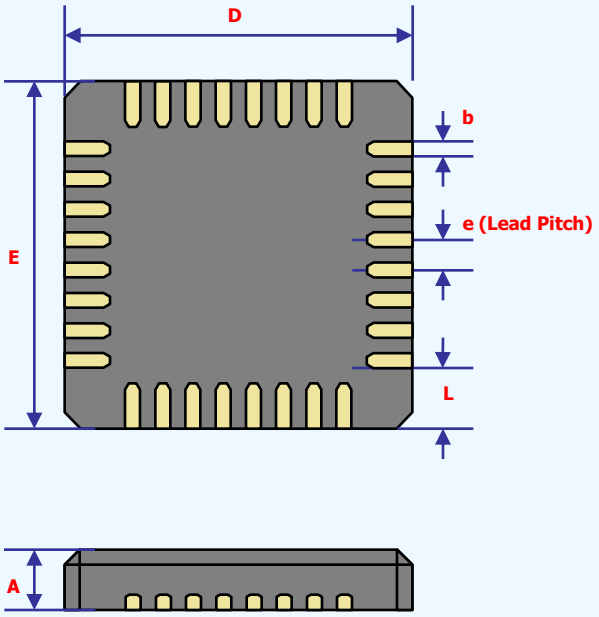
Notes:

1. Dimension D * E do not include interlead flash.
2. Dimension c_1 dose not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.

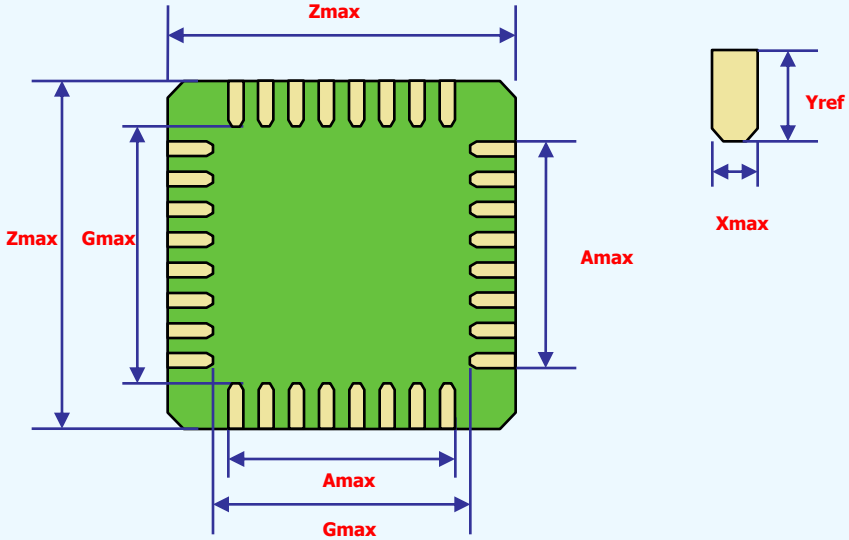


14. Package Dimensions : 32-MLF

[MLF 32]



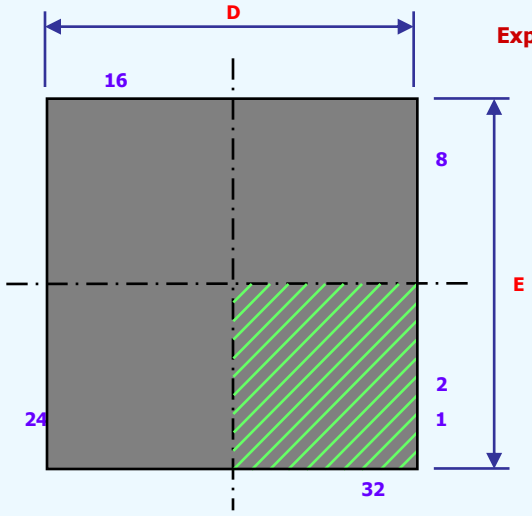
[PCB dimension]



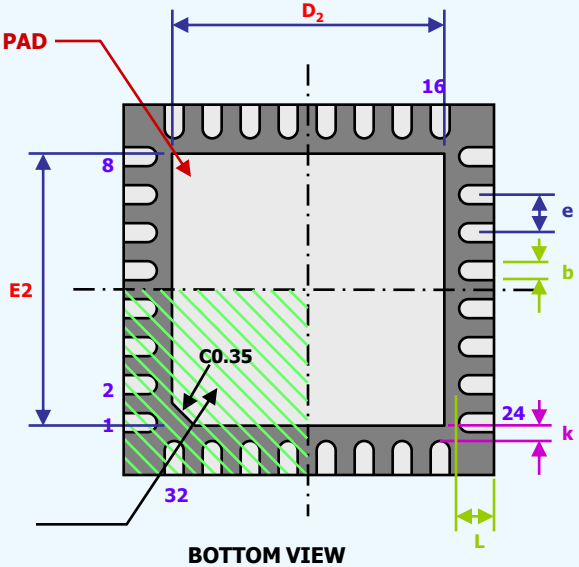
Unit : mm

Package				Package Dimensions with Tolerance										Board Land Pattern Dimensions				
Size	I/O	Leads / Side	Lead Pitch	D(min)	D(max)	E(min)	E(max)	b(min)	b(max)	L(min)	L(max)	A(typ)	A(max)	Xmax	Yref	Amax	Gmin	Zmax
5X5	32	8	0.50	4.90	5.10	4.90	5.10	0.18	0.30	0.4	0.6	0.85	0.90	0.28	0.69	3.78	3.93	5.31

14. Package Dimensions : 32-QFN



TOP VIEW



BOTTOM VIEW

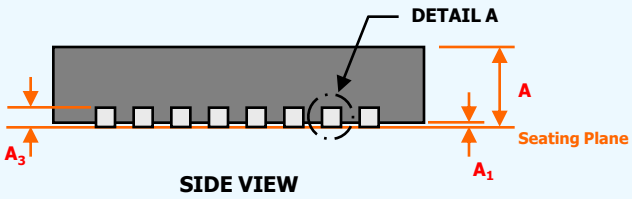
[32-QFN]

Symbol	Dimension in mm		
	Min.	Nom.	Max.
A	0.80	0.85	0.90
A_1	0.00	0.02	0.05
A_3		0.20 REF	
D		5.00 BSC	
E		5.00 BSC	
D_2	3.35	3.45	3.55
E_2	3.35	3.45	3.55
b	0.20	0.25	0.30
e		0.50 REF	
L	0.30	0.40	0.50
K	0.20	-	-

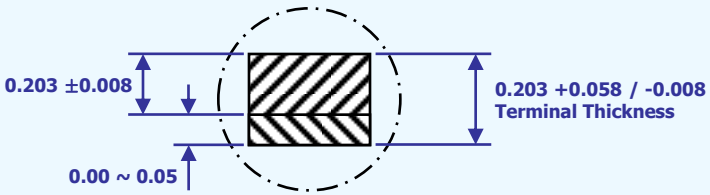
Notes:

1. All Dimension are in mm. Angles in Degrees.
2. Pin 1 visual index feature may vary, but must be located within the hatched area.
4. Package is saw singulated.
5. Refer JEDEC MO-220.
6. BSC : Basic Dimension. Theoretically exact value shown without tolerances.

REF : Reference Dimension, Usually without tolerance, for information purpose only.

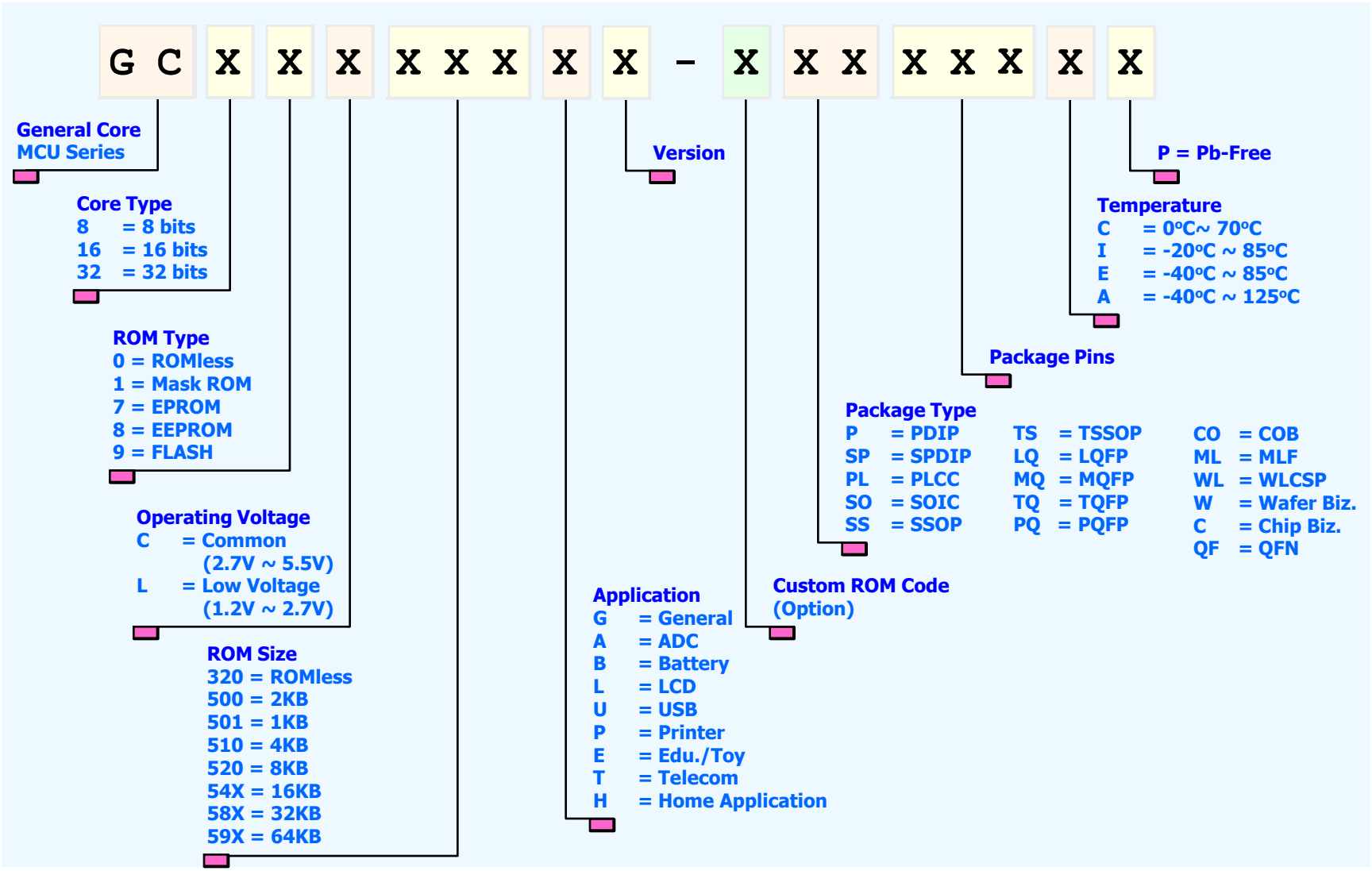


SIDE VIEW

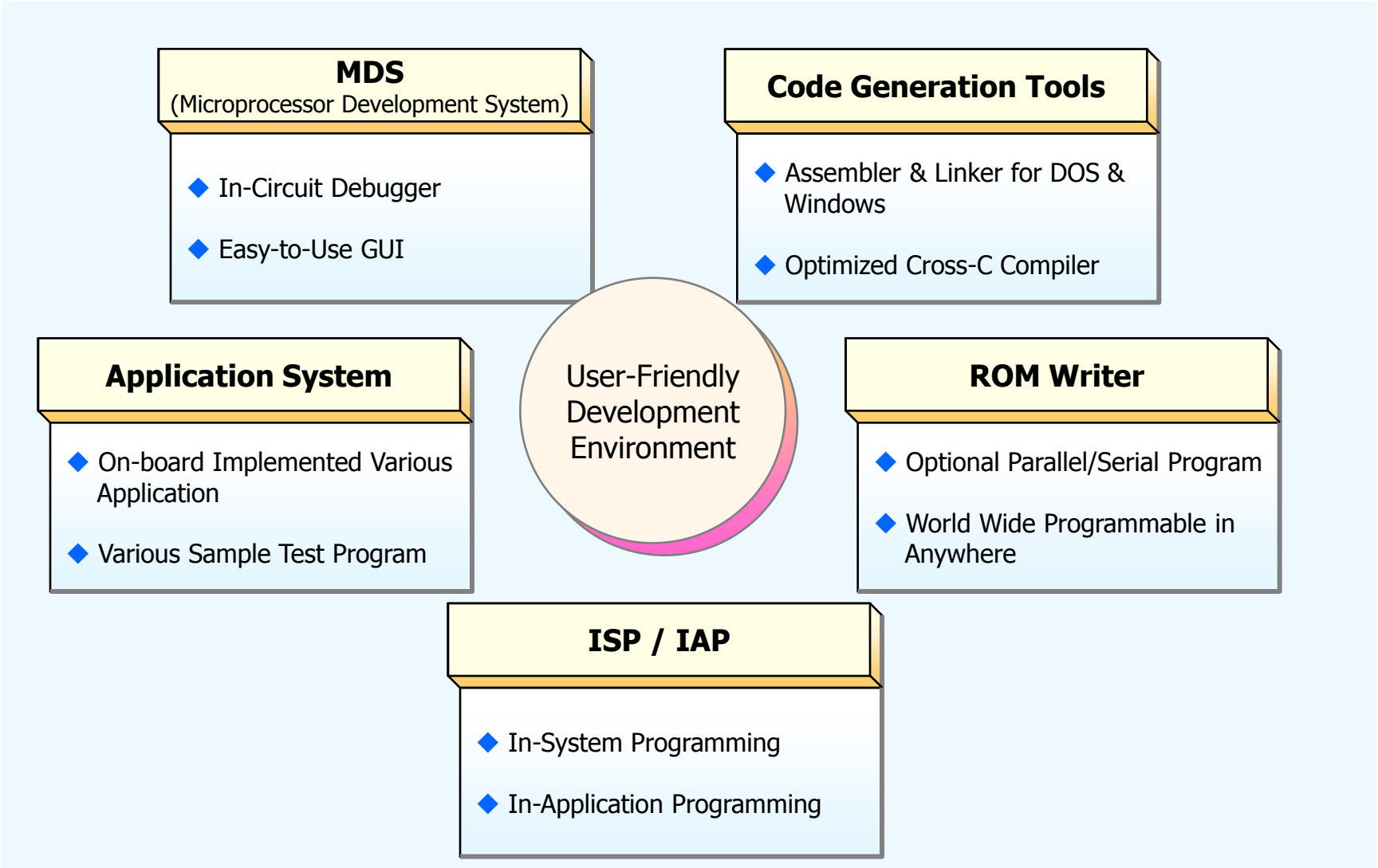


DETAIL A

15. Product Numbering System



16. Supporting tools



Appendix A : Instruction Set (1/19)

- Note on Instruction Set and Addressing Modes

Notation	Descriptions
`Rn`	Register R0 ~ R7 of the currently selected Register Bank (RB0 ~ RB3).
`direct`	The address of 8-bit internal data location. This could be an IRAM location (0x00 ~ 0x7F; 128 bytes) or a SFR (0x80 ~ 0xFF).
`@Ri`	8-bit IRAM location (0x00 ~ 0xFF; 256 bytes) addressed indirectly through register **`R0`** or **`R1`**.
`#data`	8-bit constant included in instruction.
`#data16`	16-bit constant included in instruction.
`addr16`	16-bit destination address. Used by **`LCALL`** & **`LJMP`**. The branch can be anywhere within the 64kbytes program memory address space.
`addr11`	11-bit destination address. Used by **`ACALL`** & **`AJMP`**. The branch will be within the same 2kbytes page of program memory as the first byte of the following instruction.
`rel`	Signed (2's complement number) 8-bit offset byte. Used by **`SJMP`** and all conditional jumps. Range is -128 to +127 byte relative to first byte of the following instruction.
`bit`	Direct addressed bit n IRAM of SFR.

Appendix A : Instruction Set (2/19)

ADD A, <src-byte>

1 cycle = 4 clocks

Add

ADD A, Rn

Operation : (A) ← (A) + (Rn)

Encoding : HEX: 28h, #bytes: 1, Cycles: 1

0	0	1	0	1	r	r	r

ADD A, @Ri

Operation : (A) ← (A) + ((Ri))

Encoding : HEX: 26h, #bytes: 1, Cycles: 1

0	0	1	0	0	1	1	i

ADD A, direct

Operation : (A) ← (A) + (direct)

Encoding : HEX: 25h, #bytes: 2, Cycles: 2

0	0	1	0	0	1	0	1	direct addr

ADD A, #data

Operation : (A) ← (A) + data

Encoding : HEX: 24h, #bytes: 2, Cycles: 2

0	0	1	0	0	1	0	0	immediate data

ADDC A, <src-byte>

Add with Carry

ADDC A, Rn

Operation : (A) ← (A) + (C) + (Rn)

Encoding : HEX: 38h, #bytes: 1, Cycles: 1

0	0	1	1	1	r	r	r

ADDC A, @Ri

Operation : (A) ← (A) + (C) + ((Ri))

Encoding : HEX: 36h, #bytes: 1, Cycles: 1

0	0	1	1	0	1	1	i

ADDC A, direct

Operation : (A) ← (A) + (C) + (direct)

Encoding : HEX: 35h, #bytes: 2, Cycles: 2

0	0	1	1	0	1	0	1	direct addr

ADDC A, #data

Operation : (A) ← (A) + (C) + data

Encoding : HEX: 34h, #bytes: 2, Cycles: 2

0	0	1	1	0	1	0	0	immediate data

Appendix A : Instruction Set (3/19)

SUBB A, <src-byte>

Subtract with Borrow

SUBB A, Rn

Operation : (A) ← (A) - (C) - (Rn)

Encoding : HEX: 98h, #bytes: 1, Cycles: 1

1	0	0	1	1	r	r	r

SUBB A, @Ri

Operation : (A) ← (A) - (C) - ((Ri))

Encoding : HEX: 96h, #bytes: 1, Cycles: 1

1	0	0	1	0	1	1	i

SUBB A, direct

Operation : (A) ← (A) - (C) - (direct)

Encoding : HEX: 95h, #bytes: 2, Cycles: 2

1	0	0	1	0	1	0	1	direct addr

SUBB A, #data

Operation : (A) ← (A) - (C) - data

Encoding : HEX: 94h, #bytes: 2, Cycles: 2

1	0	0	1	0	1	0	0	immediate data

INC <byte>

Increment

INC A

Operation : (A) ← (A) + 1

Encoding : HEX: 04h, #bytes: 1, Cycles: 1

0	0	0	0	0	1	0	0

INC Rn

Operation : (Rn) ← (Rn) + 1

Encoding : HEX: 08h, #bytes: 1, Cycles: 1

0	0	0	0	1	r	r	r

INC @Ri

Operation : ((Ri)) ← ((Ri)) + 1

Encoding : HEX: 06h, #bytes: 1, Cycles: 1

0	0	0	0	0	1	1	i

INC direct

Operation : (direct) ← (direct) + 1

Encoding : HEX: 05h, #bytes: 2, Cycles: 2

0	0	0	0	0	1	0	1	direct addr

INC DPTR

Operation : (DPTR) ← (DPTR) + 1

Encoding : HEX: A3h, #bytes: 1, Cycles: 1

1	0	1	0	0	0	1	1

Appendix A : Instruction Set (4/19)

DEC <byte>

Decrement

DEC A

Operation : (A) ← (A) - 1

Encoding : HEX: 14h, #bytes: 1, Cycles: 1

0	0	0	1	0	1	0	0

DEC Rn

Operation : (Rn) ← (Rn) - 1

Encoding : HEX: 18h, #bytes: 1, Cycles: 1

0	0	0	1	1	r	r	r

DEC @Ri

Operation : ((Ri)) ← ((Ri)) - 1

Encoding : HEX: 16h, #bytes: 1, Cycles: 1

0	0	0	1	0	1	1	i

DEC direct

Operation : (direct) ← (direct) - 1

Encoding : HEX: 15h, #bytes: 1, Cycles: 1

0	0	0	1	0	1	0	1	direct addr

DEC DPTR

Operation : (DPTR) ← (DPTR) - 1

Encoding : HEX: A5h, #bytes: 1, Cycles: 1

1	0	1	0	0	1	0	1

MUL AB

Multiply

Operation : $(A)_{7-0}$, $(B)_{15-8}$ ← (A) x (B)

Encoding : HEX: A4h, #bytes: 1, Cycles: 3

1	0	1	0	0	1	0	0

DIV AB

Divide

Operation : $(A)_{15-8}$, $(B)_{7-0}$ ← (A) / (B)

Encoding : HEX: 84h, #bytes: 1, Cycles: 3

1	0	0	0	0	1	0	0

Appendix A : Instruction Set (5/19)

DA A

Decimal-adjust Accumulator for Addition

Operation :

IF [[(A_{3-0})>9] ∨ [(AC)=1]]
THEN (A_{3-0}) ← (A_{3-0})+6
IF [[(A_{7-4})>9] ∨ [(C)=1]]
THEN (A_{7-4}) ← (A_{7-4})+6

Encoding : HEX: D4h, #bytes: 1, Cycles: 1

1	1	0	1	0	1	0	0

ANL <dest-byte>, <src-byte>

Logical AND for byte variables

ANL A, Rn

Operation : (A) ← (A) ^ (Rn)

Encoding : HEX: 58h, #bytes: 1, Cycles: 1

0	1	0	1	1	r	r	r

ANL A, @Ri

Operation : (A) ← (A) ^ ((Ri))

Encoding : HEX: 56h, #bytes: 1, Cycles: 1

0	1	0	1	0	1	1	i

ANL A, direct

Operation : (A) ← (A) ^ (direct)

Encoding : HEX: 55h, #bytes: 2, Cycles: 2

0	1	0	1	0	1	0	1	direct addr

ANL A, #data

Operation : (A) ← (A) ^ data

Encoding : HEX: 54h, #bytes: 2, Cycles: 2

0	1	0	1	0	1	0	0	immediate data

ANL direct, A

Operation : (direct) ← (direct) ^ (A)

Encoding : HEX: 52h, #bytes: 2, Cycles: 2

0	1	0	1	0	0	1	0	direct addr

ANL direct, #data

Operation : (direct) ← (direct) ^ data

Encoding : HEX: 53h, #bytes: 3, Cycles: 3

0	1	0	1	0	0	1	1	direct addr	immediate data

Appendix A : Instruction Set (6/19)

ANL C, <src-bit>

Logical AND for bit variables

ANL C, bit

Operation : (C) ← (C) ^ (bit)

Encoding : HEX: 82h, #bytes: 2, Cycles: 2

1	0	0	0	0	0	1	0	bit addr

ANL C, /bit

Operation : (C) ← (C) ^ ~(bit)

Encoding : HEX: B0h, #bytes: 2, Cycles: 2

1	0	1	1	0	0	0	0	bit addr

ORL <dest-byte>, <src-byte>

Logical OR for byte variables

ORL A, Rn

Operation : (A) ← (A) ∨ (Rn)

Encoding : HEX: 48h, #bytes: 1, Cycles: 1

0	1	0	0	1	r	r	r

ORL A, @Ri

Operation : (A) ← (A) ∨ ((Ri))

Encoding : HEX: 46h, #bytes: 1, Cycles: 1

0	1	0	0	0	1	1	i

ORL A, direct

Operation : (A) ← (A) ∨ (direct)

Encoding : HEX: 45h, #bytes: 2, Cycles: 2

0	1	0	0	0	1	0	1	direct addr

ORL A, #data

Operation : (A) ← (A) ∨ data

Encoding : HEX: 44h, #bytes: 2, Cycles: 2

0	1	0	0	0	1	0	0	immediate data

ORL direct, A

Operation : (direct) ← (direct) ∨ (A)

Encoding : HEX: 42h, #bytes: 2, Cycles: 2

0	1	0	0	0	0	1	0	direct addr

ORL direct, #data

Operation : (direct) ← (direct) ∨ data

Encoding : HEX: 43h, #bytes: 3, Cycles: 3

0	1	0	0	0	0	1	1	direct addr	immediate data

Appendix A : Instruction Set (7/19)

ORL C, <src-byte>

Logical OR for byte variables

ORL C, bit

Operation : (C) ← (C) ∨ (bit)

Encoding : HEX: 72h, #bytes: 2, Cycles: 2

0	1	1	1	0	0	1	0	bit addr

ORL C, /bit

Operation : (C) ← (C) ∨ ~(bit)

Encoding : HEX: A0h, #bytes: 2, Cycles: 2

1	0	1	0	0	0	0	0	bit addr

XRL <dest-byte>, <src-byte>

Logical Exclusive-OR for byte variables

XRL A, Rn

Operation : (A) ← (A) ⊕ (Rn)

Encoding : HEX: 68h, #bytes: 1, Cycles: 1

0	1	1	0	1	r	r	r

XRL A, @Ri

Operation : (A) ← (A) ⊕ ((Ri))

Encoding : HEX: 66h, #bytes: 1, Cycles: 1

0	1	1	0	0	1	1	i

XRL A, direct

Operation : (A) ← (A) ⊕ (direct)

Encoding : HEX: 65h, #bytes: 2, Cycles: 2

0	1	1	0	0	1	0	1	direct addr

XRL A, #data

Operation : (A) ← (A) ⊕ data

Encoding : HEX: 64h, #bytes: 2, Cycles: 2

0	1	1	0	0	1	0	0	immediate data

XRL direct, A

Operation : (direct) ← (direct) ⊕ (A)

Encoding : HEX: 62h, #bytes: 2, Cycles: 2

0	1	1	0	0	0	1	0	direct addr

XRL direct, #data

Operation : (direct) ← (direct) ⊕ data

Encoding : HEX: 63h, #bytes: 3, Cycles: 3

0	1	1	0	0	0	1	1	direct addr	immediate Data

Appendix A : Instruction Set (8/19)

CLR A

Clear Accumulator

Operation : (A) ← 0

Encoding : HEX: E4h, #bytes: 1, Cycles: 1

1	1	1	0	0	1	0	0

CLR <bit>

Clear bit

CLR C

Operation : (C) ← 0

Encoding : HEX: C3h, #bytes: 1, Cycles: 1

1	1	0	0	0	0	1	1

CLR bit

Operation : (bit) ← 0

Encoding : HEX: C2h, #bytes: 2, Cycles: 2

1	1	0	0	0	0	1	0	bit addr

CPL A

Complement Accumulator

Operation : (A) ← ~(A)

Encoding : HEX: F4h, #bytes: 1, Cycles: 1

1	1	1	1	0	1	0	0

CPL <bit>

Complement bit

CPL C

Operation : (C) ← ~(C)

Encoding : HEX: B3h, #bytes: 1, Cycles: 1

1	0	1	1	0	0	1	1

CPL bit

Operation : (bit) ← ~(bit)

Encoding : HEX: B2h, #bytes: 2, Cycles: 2

1	0	1	1	0	0	1	0	bit addr

Appendix A : Instruction Set (9/19)

RL A

Rotate Accumulator Left

Operation : $(A_{n+1}) \leftarrow (A_n)$ n=0~6
$(A_0) \leftarrow (A_7)$

Encoding : HEX: 23h, #bytes: 1, Cycles: 1

0	0	1	0	0	0	1	1

RLC A

Rotate Accumulator Left through the Carry flag

Operation : $(A_{n+1}) \leftarrow (A_n)$ n=0~6
$(A_0) \leftarrow (C)$
$(C) \leftarrow (A_7)$

Encoding : HEX: 33h, #bytes: 1, Cycles: 1

0	0	1	1	0	0	1	1

RR A

Rotate Accumulator Right

Operation : $(A_n) \leftarrow (A_{n+1})$ n=0~6
$(A_7) \leftarrow (A_0)$

Encoding : HEX: 03h, #bytes: 1, Cycles: 1

0	0	0	0	0	0	1	1

RRC A

Rotate Accumulator Right through the Carry flag

Operation : $(A_n) \leftarrow (A_{n+1})$ n=0~6
$(A_7) \leftarrow (C)$
$(C) \leftarrow (A_0)$

Encoding : HEX: 13h, #bytes: 1, Cycles: 1

0	0	0	1	0	0	1	1

SWAP A

Swap nibbles within the Accumulator

Operation : $(A_{3-0}) \leftrightarrow (A_{7-4})$

Encoding : HEX: C4h, #bytes: 1, Cycles: 1

1	1	0	0	0	1	0	0

Appendix A : Instruction Set (10/19)

MOV <dest-byte>, <src-byte>

Move byte variable

MOV A, Rn

Operation : (A) ← (Rn)

Encoding : HEX: E8h, #bytes: 1, Cycles: 1

1	1	1	0	1	r	r	r

MOV A, @Ri

Operation : (A) ← ((Ri))

Encoding : HEX: E6h, #bytes: 1, Cycles: 1

1	1	1	0	0	1	1	i

MOV A, direct

Operation : (A) ← (direct)

Encoding : HEX: E5h, #bytes: 2, Cycles: 2

1	1	1	0	0	1	0	1	direct addr

MOV A, #data

Operation : (A) ← data

Encoding : HEX: 74h, #bytes: 2, Cycles: 2

0	1	1	1	0	1	0	0	immediate data

MOV Rn, A

Operation : (Rn) ← (A)

Encoding : HEX: F8h, #bytes: 1, Cycles: 1

1	1	1	1	1	r	r	r

MOV Rn, direct

Operation : (Rn) ← (direct)

Encoding : HEX: A8h, #bytes: 2, Cycles: 2

1	0	1	0	1	r	r	r	direct addr

MOV Rn, #data

Operation : (Rn) ← data

Encoding : HEX: 78h, #bytes: 2, Cycles: 2

0	1	1	1	1	r	r	r	immediate data

MOV direct, A

Operation : (direct) ← (A)

Encoding : HEX: F5h, #bytes: 2, Cycles: 2

1	1	1	1	0	1	0	1	direct addr

MOV direct, Rn

Operation : (direct) ← (Rn)

Encoding : HEX: 88h, #bytes: 2, Cycles: 2

1	0	0	0	1	r	r	r	direct addr

Appendix A : Instruction Set (11/19)

MOV direct, @Ri

Operation : (direct) ← ((Ri))

Encoding : HEX: 86h, #bytes: 2, Cycles: 2

1	0	0	0	0	1	1	i	direct addr

MOV direct, direct

Operation : (direct) ← (direct)

Encoding : HEX: 85h, #bytes: 3, Cycles: 3

1	0	0	0	0	1	0	1	direct addr(src)	direct addr(dest)

MOV direct, #data

Operation : (direct) ← data

Encoding : HEX: 75h, #bytes: 3, Cycles: 3

0	1	1	1	0	1	0	1	direct addr	immediate data

MOV @Ri, A

Operation : ((Ri)) ← (A)

Encoding : HEX: F6h, #bytes: 1, Cycles: 1

1	1	1	1	0	1	1	i

MOV @Ri, direct

Operation : ((Ri)) ← (direct)

Encoding : HEX: A6h, #bytes: 2, Cycles: 2

1	0	1	0	0	1	1	i	direct addr

MOV @Ri, #data

Operation : ((Ri)) ← data

Encoding : HEX: 76h, #bytes: 2, Cycles: 2

0	1	1	1	0	1	1	i	immediate Data

MOV <dest-bit>, <src-bit>

Move bit data

MOV C, bit

Operation : (C) ← (bit)

Encoding : HEX: A2h, #bytes: 2, Cycles: 2

1	0	1	0	0	0	1	0	bit addr

MOV bit, C

Operation : (bit) ← (C)

Encoding : HEX: 92h, #bytes: 2, Cycles: 2

1	0	0	1	0	0	1	0	bit addr

Appendix A : Instruction Set (12/19)

MOV DPTR, #data16

Load Data Pointer with a 16-bit constant

Operation :
(DPTR) ← $data_{15-0}$
(DPH,DPL) ← ($data_{15-8}$,$data_{7-0}$)

Encoding : HEX: 90h, #bytes: 3, Cycles: 3

1	0	0	1	0	0	0	0	immed. data 15-8	immed. data 7-0

MOVC A, @A + <base-reg>

Move Code byte

MOVC A, @A + DPTR

Operation : (A) ← ((A) + (DPTR))

Encoding : HEX: 93h, #bytes: 1, Cycles: 2

1	0	0	1	0	0	1	1

MOVC A, @A + PC

Operation :
(PC) ← (PC) + 1
(A) ← ((A) + (PC))

Encoding : HEX: 83h, #bytes: 1, Cycles: 2

1	0	0	0	0	0	1	1

MOVX <dest-byte>, <src-byte>

Move External

MOVX A, @Ri

Operation : (A) ← ((Ri))

Encoding : HEX: E2h, #bytes: 1, Cycles: 3

1	1	1	0	0	0	1	i

MOVX A, @DPTR

Operation : (A) ← ((DPTR))

Encoding : HEX: E0h, #bytes: 1, Cycles: 3

1	1	1	0	0	0	0	0

MOVX @Ri, A

Operation : ((Ri)) ← (A)

Encoding : HEX: F2h, #bytes: 1, Cycles: 3

1	1	1	1	0	0	1	i

MOVX @DPTR, A

Operation : ((DPTR)) ← (A)

Encoding : HEX: F0h, #bytes: 1, Cycles: 3

1	1	1	1	0	0	0	0

Appendix A : Instruction Set (13/19)

XCH A, <src-byte>

Exchange Accumulator with byte variable

XCH A, Rn

Operation : (A) ↔ (Rn)

Encoding : HEX: C8h, #bytes: 1, Cycles: 1

1	1	0	0	1	r	r	r

XCH A, @Ri

Operation : (A) ↔ ((Ri))

Encoding : HEX: C6h, #bytes: 1, Cycles: 1

1	1	0	0	0	1	1	i

XCH A, direct

Operation : (A) ↔ (direct)

Encoding : HEX: C5h, #bytes: 2, Cycles: 2

1	1	0	0	0	1	0	1	direct addr

XCHD A, @Ri

Exchange Digit

Operation : $(A_{3-0}) \leftrightarrow ((Ri))_{3-0}$

Encoding : HEX: D6h, #bytes: 1, Cycles: 1

1	1	0	1	0	1	1	i

PUSH direct

Push onto stack

Operation :
(SP) ← (SP) + 1
((SP)) ← (direct)

Encoding : HEX: C0h, #bytes: 2, Cycles: 2

1	1	0	0	0	0	0	0	direct addr

POP direct

Pop onto stack

Operation :
(direct) ← ((SP))
(SP) ← (SP) – 1

Encoding : HEX: D0h, #bytes: 2, Cycles: 2

1	1	0	1	0	0	0	0	direct addr

Appendix A : Instruction Set (14/19)

SETB <bit>

Set bit

SETB C

Operation : (C) ← 1

Encoding : HEX: D3h, #bytes: 1, Cycles: 1

1	1	0	1	0	0	1	1

SETB bit

Operation : (bit) ← 1

Encoding : HEX: D2h, #bytes: 2, Cycles: 2

1	1	0	1	0	0	1	0	bit addr

JC rel

Jump if Carry is set

Operation :
(PC) ← (PC) + 2
If (C) = 1, then (PC) ← (PC) + rel

Encoding : HEX: 40h, #bytes: 2, Cycles: 3

0	1	0	0	0	0	0	0	relative addr

JNC rel

Jump if Carry is not set

Operation :
(PC) ← (PC) + 2
If (C) = 0, then (PC) ← (PC) + rel

Encoding : HEX: 50h, #bytes: 2, Cycles: 3

0	1	0	1	0	0	0	0	relative addr

JB bit, rel

Jump if Bit is set

Operation :
(PC) ← (PC) + 3
If (bit) = 1, then (PC) ← (PC)+rel

Encoding : HEX: 20h, #bytes: 3, Cycles: 4

0	0	1	0	0	0	0	0	bit addr	relative addr

JNB bit, rel

Jump if Bit is not set

Operation :
(PC) ← (PC) + 3
If (bit) = 0, then (PC) ← (PC)+rel

Encoding : HEX: 30h, #bytes: 3, Cycles: 4

0	0	1	1	0	0	0	0	bit addr	relative addr

Appendix A : Instruction Set (15/19)

JBC bit, rel

Jump if Bit is set and Clear bit

Operation :

```
(PC)  ← (PC) + 3
If (bit) = 1,
then (bit) ← 0, (PC) ← (PC) + rel
```

Encoding : HEX: 10h, #bytes: 3, Cycles: 4

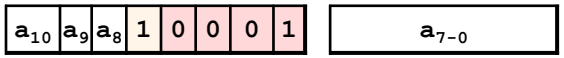
ACALL addr11

Absolute Subroutine Call

Operation :

```
(PC)    ← (PC) + 2
(SP)    ← (SP) + 1
((SP))  ← (PC7-0)
(SP)    ← (SP) + 1
((SP))  ← (PC15-8)
(PC10-0) ← page address
```

Encoding : HEX: 11h, #bytes: 2, Cycles: 3



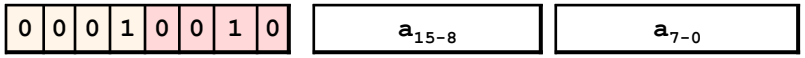
LCALL addr16

Long Subroutine Call

Operation :

```
(PC)    ← (PC) + 3
(SP)    ← (SP) + 1
((SP))  ← (PC7-0)
(SP)    ← (SP) + 1
((SP))  ← (PC15-8)
(PC)    ← addr15-0
```

Encoding : HEX: 12h, #bytes: 3, Cycles: 4



Appendix A : Instruction Set (16/19)

RET

Return from Subroutine

Operation :

$(PC_{15-8}) \leftarrow ((SP))$
$(SP) \leftarrow (SP) - 1$
$(PC_{7-0}) \leftarrow ((SP))$
$(SP) \leftarrow (SP) - 1$

Encoding : HEX: 22h, #bytes: 1, Cycles: 2

0	0	1	0	0	0	1	0

RETI

Return from Interrupt

Operation :

$(PC_{15-8}) \leftarrow ((SP))$
$(SP) \leftarrow (SP) - 1$
$(PC_{7-0}) \leftarrow ((SP))$
$(SP) \leftarrow (SP) - 1$

Encoding : HEX: 32h, #bytes: 1, Cycles: 2

0	0	1	1	0	0	1	0

AJMP addr11

Absolute Jump

Operation :

$(PC) \leftarrow (PC) + 2$
$(PC_{10-0}) \leftarrow$ page address

Encoding : HEX: 01h, #bytes: 2, Cycles: 3

a_{10}	a_9	a_8	0	0	0	0	1	a_{7-0}

SJMP rel

Short Jump (Relative address)

Operation :

$(PC) \leftarrow (PC) + 2$
$(PC_{10-0}) \leftarrow (PC) + rel$

Encoding : HEX: 80h, #bytes: 2, Cycles: 3

1	0	0	0	0	0	0	0	relative addr

LJMP addr16

Long Jump

Operation : $(PC) \leftarrow addr_{15-0}$

Encoding : HEX: 02h, #bytes: 3, Cycles: 4

0	0	0	0	0	0	1	0	a_{15-8}	a_{7-0}

Appendix A : Instruction Set (17/19)

JMP @A + DPTR

Jump Indirect Relative to the DPTR

Operation : (PC) ← (A) + (DPTR)

Encoding : HEX: 73h, #bytes: 1, Cycles: 2

0	1	1	1	0	0	1	1

JZ rel

Jump if Accumulator is Zero

Operation :
(PC) ← (PC) + 2
If (A)=0, then (PC) ← (PC) + rel

Encoding : HEX: 60h, #bytes: 2, Cycles: 3

0	1	1	0	0	0	0	0	relative addr

JNZ rel

Jump if Accumulator is Not Zero

Operation :
(PC) ← (PC) + 2
If (A)≠0, then (PC) ← (PC) + rel

Encoding : HEX: 70h, #bytes: 2, Cycles: 3

0	1	1	1	0	0	0	0	relative addr

Appendix A : Instruction Set (18/19)

CJNE <dest-byte>, <src-byte>, rel

Compare and Jump if Not Equal

CJNE A, direct, rel

Operation :

```
(PC)  ← (PC) + 3
If (A) ≠ (direct),
      then (PC) ← (PC) + rel
If (A) < (direct), then (C) ← 1
Else                  (C) ← 0
```

Encoding : HEX: B5h, #bytes: 3, Cycles: 4

1	0	1	1	0	1	0	1	direct addr	relative addr

CJNE A, #data, rel

Operation :

```
(PC)  ← (PC) + 3
If (A) ≠ data,
      then (PC) ← (PC) + rel
If (A) < data, then (C) ← 1
Else                (C) ← 0
```

Encoding : HEX: B4h, #bytes: 3, Cycles: 4

1	0	1	1	0	1	0	0	immediate data	relative addr

CJNE Rn, #data, rel

Operation :

```
(PC)  ← (PC) + 3
If (Rn) ≠ data,
      then (PC) ← (PC) + rel
If (Rn) < data, then (C) ← 1
Else                (C) ← 0
```

Encoding : HEX: B8h, #bytes: 3, Cycles: 4

1	0	1	1	1	r	r	r	immediate data	relative addr

CJNE @Ri, #data, rel

Operation :

```
(PC)  ← (PC) + 3
If ((Ri)) ≠ data,
      then (PC) ← (PC) + rel
If ((Ri)) < data, then (C) ← 1
Else                (C) ← 0
```

Encoding : HEX: B6h, #bytes: 3, Cycles: 4

1	0	1	1	0	1	1	i	immediate data	relative addr

Appendix A : Instruction Set (19/19)

DJNZ <byte>, rel

Decrement and Jump if Not Zero

DJNZ Rn, rel

Operation :

```
(PC)  ← (PC) + 2
(Rn)  ← (Rn) - 1
If (Rn)≠0, then (PC) ← (PC) + rel
```

Encoding : HEX: D8h, #bytes: 2, Cycles: 3

1	1	0	1	1	r	r	r	relative addr

DJNZ direct, rel

Operation :

```
(PC)     ← (PC) + 3
(direct) ← (direct) - 1
If (direct)≠0,
        then (PC) ← (PC) + rel
```

Encoding : HEX: D5h, #bytes: 3, Cycles: 4

1	1	0	1	0	1	0	1	direct addr	relative addr

NOP

No Operation

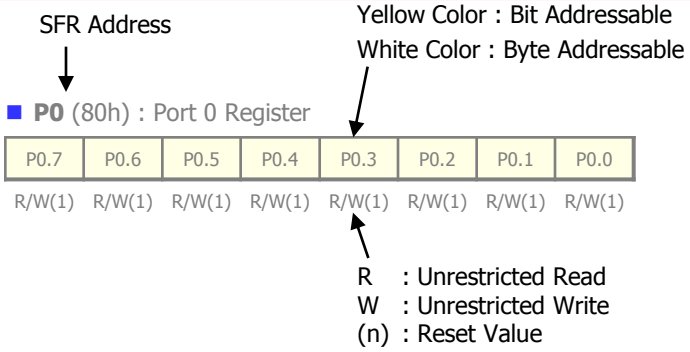
Operation : (PC) ← (PC) + 1

Encoding : HEX: 00h, #bytes: 1, Cycles: 1

0	0	0	0	0	0	0	0

Appendix B : SFR Description [80h ~ 84h] (1/20)

[How to Read a SFR Descriptions]



■ **P0** (80h) : Port 0 Register

P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- Open-drain bidirectional port.
- Multiplexing low order address/data bus during external memory access

■ **SP** (81h) : Stack Pointer Register

SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(1)	R/W(1)	R/W(1)

- Indicate where stack will start.
- Increment by PUSH and decrement by POP.

■ **DPL** (82h) : Data Pointer Low Register

DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **DPH** (83h) : Data Pointer High Register

DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **ADCON** (84h) : ADC Control & ADC Result Low Register

AD_EN	AD_REQ	AD_END	ADCF	-	-	SAR1	SAR0
R/W(0)	R/W(0)	R(1)	R/W(0)			R/W(0)	R/W(0)

- AD_EN : ADC Ready Enable
- AD_REQ : ADC Start.
  Cleared by H/W when AD_END goes to 1 from 0.
- AD_END : Current ADC Status.
  0 = ADC is running now.
  User must check the ADCF instead of AD_END.
- ADCF : ADC Interrupt Flag.
  Must be cleared by S/W.
- SAR[1:0] : Low Bits of ADC Result Value. (Total 10 bits)

Appendix B : SFR Description [85h ~ 86h] (2/20)

■ **ADCSEL** (85h) : ADC Clock and MUX Selection Register

ADIV2	ADIV1	ADIV0	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

◆ ADIV[2:0] : ADC clock selection.

[000] : FSYS / 2.
[001] : FSYS/ 4.
[010] : FSYS / 8.
[011] : FSYS / 16.
[100] : FSYS / 32.
[101] : FSYS / 64.
[110] : FSYS / 128.
[111] : FSYS / 256.

◆ ADCS[4:0] : ADC channel selection

[00000] : ADC0.0 channel selection.
[00001] : ADC0.1 channel selection.
[00010] : ADC0.2 channel selection.
[00011] : ADC0.3 channel selection.
[00100] : ADC0.4 channel selection.
[00101] : ADC0.5 channel selection.
[00110] : ADC0.6 channel selection.
[00111] : ADC0.7 channel selection.
[01000] : ADC1.0 channel selection.
[01001] : ADC1.1 channel selection.
[01010] : ADC1.2 channel selection.
[01011] : ADC1.3 channel selection.
[01100] : ADC1.4 channel selection.
[01101] : ADC1.5 channel selection.
[01110] : ADC1.6 channel selection.
[01111] : ADC1.7 channel selection.

[00000] : ADC0.0 channel selection.
[00001] : ADC0.1 channel selection.
[00010] : ADC0.2 channel selection.
[00011] : ADC0.3 channel selection.
[00100] : ADC0.4 channel selection.
[00101] : ADC0.5 channel selection.
[00110] : ADC0.6 channel selection.
[00111] : ADC0.7 channel selection.
[01000] : ADC1.0 channel selection.
[01001] : ADC1.1 channel selection.
[01010] : ADC1.2 channel selection.
[01011] : ADC1.3 channel selection.
[01100] : ADC1.4 channel selection.
[01101] : ADC1.5 channel selection.
[01110] : ADC1.6 channel selection.
[01111] : ADC1.7 channel selection.

■ **ADCR** (86h) : ADC Result High Register

SAR9	SAR8	SAR7	SAR6	SAR5	SAR4	SAR3	SAR2
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

Appendix B : SFR Description [87h ~ 8Bh] (3/20)

■ PCON (87h) : Power Control Register

SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL
R/W(0)	R/W(0)		R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ SMOD1 : Timer 1 baud rate double in UART mode 1/2/3
- ◆ SMOD0 : Enable SM0 access. Don't modify this bit.
- ◆ POF : Power off flag.
  When power-on, this bit will be set by H/W.
- ◆ GF1, GF0 : General purpose flag bit.
- ◆ PD : Stop Mode (Power-down) Bit.
- ◆ IDL : IDLE Mode Bit.

■ TCON (88h) : Timer/Counter 0/1 Control Register

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ TF1 : Timer 1 overflow flag.
- ◆ TR1 : Timer 1 run enable.
- ◆ TF0 : Timer 0 overflow flag.
- ◆ TR0 : Timer 0 run enable.
- ◆ IE1 : External interrupt 1 flag.
  If IT1 = 0, cleared by S/W (software).
  If IT1 = 1, cleared automatically when go to routine.
- ◆ IT1 : External interrupt 1 type select.
  Edge detect (IT1=1) / Level detect (IT1=0; Default)
- ◆ IE0 : External interrupt 0 flag.
  If IT0 = 0, cleared by S/W (software).
  If IT0 = 1, cleared automatically when go to routine.
- ◆ IT0 : External interrupt 0 type select.
  Edge detect (IT0=1) / Level detect (IT0=0; Default)

■ TMOD (89h) : Timer/Counter 0/1 Mode Control Register

GATE	C/T	M1	M0	GATE	C/T	M1	M0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ Timer[1]: GATE[7], C/T[6], M1:M0[5:4]
- ◆ Timer[0]: GATE[3], C/T[2], M1:M0[1:0]
- ◆ GATE : When TRx (in TCON) is set and GATE=1, Timer x will run only while INTx pin is high (hardware control). When GATE=0, Timer x will run only while TRx=1 (software control).
- ◆ C/T : Counter or Timer Selector. Cleared for Timer operation (input from internal system clock). Set for Counter
- ◆ M1, M0 : Mode Selector bits
  [00] : Mode 0. 13-bit T/C.
  [01] : Mode 1. 16-bit T/C.
  [10] : Mode 2. 8-bit Auto-Reload T/C.
  [11] : Mode 3.
  (Timer 1) stopped, (Timer 0)
  TL0: 8-bit T/C controlled by the Timer 0 control bits.
  TH0: 8-bit T/C controlled by the Timer 1 control bits.

■ TL0 (8Ah) : Timer/Counter 0 Low Byte Register

TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ TL1 (8Bh) : Timer/Counter 1 Low Byte Register

TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **TH0** (8Ch) : Timer/Counter 0 High Byte Register

TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **TH1** (8Dh) : Timer/Counter 1 High Byte Register

TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **CKCON** (8Eh) : Clock Control Register

WD1	WD0	T2M	T1M	T0M	-	U1T2DIS	U0T2DIS
R/W(1)	R/W(1)	R/W(0)	R/W(0)	R/W(0)		R/W(0)	R/W(0)

- WD1, WD0 : Watchdog timer mode select
  [0,0] : 2^{17} clocks (interrupt), 2^{17} + 512 clocks (reset)
  [0,1] : 2^{20} clocks (interrupt), 2^{20} + 512 clocks (reset)
  [1,0] : 2^{23} clocks (interrupt), 2^{23} + 512 clocks (reset)
  [1,1] : 2^{26} clocks (interrupt), 2^{26} + 512 clocks (reset)
- T2M : Timer 2 clock select. When set, base time is 4 clocks.
- T1M : Timer 1 clock select. When set, base time is 4 clocks.
- T0M : Timer 0 clock select. When set, base time is 4 clocks.
- U1T2DIS : Used to disable RCLK/TCLK control for UART1 to generate its baud rate with T1 overflow
- U0T2DIS : Used to disable RCLK/TCLK control for UART0 to generate its baud rate with T1 overflow.

■ **RINGCON** (8Fh) : Ring Control Configuration Register

S7	S6	S5	S4	S3	S2	S1	S0
R/W(0)	R/W(1)	R/W(1)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- RINGCON[7:0] : Internal Ring OSC. can be tuned.

■ **P1** (90h) : Port 1 Register

P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- Quasi-bidirectional port with internal pull-up resistors.
- When alternative function enabled, P1.X must be "1".

■ **EXIF** (91h) : External Interrupt Flag Register

IE5	IE4	IE3	IE2	XT/RG	RGMD	RGSL	BGS
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(1)	R(0)	R/W(0)	R/W(1)

- IE5~2 : External interrupt 5~2 flag.
- XT/RG : System clock selection
  0 = Internal Ring Oscillator is selected as system clock.
  1 = External clock is selected as system clock.
- RGMD : Ring mode. Now system clock is Ring or XTAL. Generally RGMD is the invert of XT/RG except when the ring Oscillator provides clock during wake-up from power-down .
- RGSL : 1 = When wake-up from power-down mode in XTAL clock, use Ring Oscillator as system clock during 65,536 XTAL clocks.
- BGS : Band-gap select. When set, LVD will run in power-down mode.

Appendix B : SFR Description [92h ~ 99h] (5/20)

■ **C0CAP0L** (92h) : Low Capture/Compare Register of PCA0 MODULE0

C0CAP0L.7	C0CAP0L.6	C0CAP0L.5	C0CAP0L.4	C0CAP0L.3	C0CAP0L.2	C0CAP0L.1	C0CAP0L.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C0CAP1L** (93h) : Low Capture/Compare Register of PCA0 MODULE1

C0CAP1L.7	C0CAP1L.6	C0CAP1L.5	C0CAP1L.4	C0CAP1L.3	C0CAP1L.2	C0CAP1L.1	C0CAP1L.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C0CAP2L** (94h) : Low Capture/Compare Register of PCA0 MODULE2

C0CAP2L.7	C0CAP2L.6	C0CAP2L.5	C0CAP2L.4	C0CAP2L.3	C0CAP2L.2	C0CAP2L.1	C0CAP2L.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C0CAP3L** (95h) : Low Capture/Compare Register of PCA0 MODULE3

C0CAP3L.7	C0CAP3L.6	C0CAP3L.5	C0CAP3L.4	C0CAP3L.3	C0CAP3L.2	C0CAP3L.1	C0CAP3L.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C0CAP4L** (96h) : Low Capture/Compare Register of PCA0 MODULE4

C0CAP4L.7	C0CAP4L.6	C0CAP4L.5	C0CAP4L.4	C0CAP4L.3	C0CAP4L.2	C0CAP4L.1	C0CAP4L.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C0CAP5L** (97h) : Low Capture/Compare Register of PCA0 MODULE5

C0CAP5L.7	C0CAP5L.6	C0CAP5L.5	C0CAP5L.4	C0CAP5L.3	C0CAP5L.2	C0CAP5L.1	C0CAP5L.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **SCON** (98h) : Serial Port Control Register of UART0

SM0	SM1	SM2	REN	TB8	RB8	TI	RI
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ SM0, SM1 : Serial Port mode select.
  [0,0] : Mode0, 8-bit shift register (F_{PERI}/4)
  [0,1] : Mode1, 8-bit UART (Variable)
  [1,0] : Mode2, 9-bit UART (F_{PERI}/32 or F_{PERI}/16)
  [1,1] : Mode3, 9-bit UART (Variable)
- ◆ SM2 : Enables the Automatic Address Recognition in Mode2 and 3.
  In Mode 1, the Validity of the Stop Bit is checked if SM2=1.
  In Mode0, SM2 should be "0".
- ◆ REN : Enable/Disable Reception.
- ◆ TB8 : 9th data bit that will be transmitted in Mode2 and 3.
- ◆ RB8 : 9th data bit that was received in Mode 2 and 3.
  In Mode1, RB8 is equal to stop bit if SM2 is "0".
  In Mode0, RB8 is not used.
- ◆ TI : Transmission interrupt flag. Must be cleared by S/W.
- ◆ RI : Reception interrupt flag. Must be cleared by S/W.

■ **SBUF** (99h) : Serial Data Buffer Register of UART0

SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ The transmission buffer and the reception buffer are separated.
- ◆ The transmission/reception buffers have the same address.

■ **C0CAP0H** (9Ah) : High Capture/Compare Register of PCA0 MODULE0

C0CAP0H.7	C0CAP0H.6	C0CAP0H.5	C0CAP0H.4	C0CAP0H.3	C0CAP0H.2	C0CAP0H.1	C0CAP0H.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C0CAP1H** (9Bh) : High Capture/Compare Register of PCA0 MODULE1

C0CAP1H.7	C0CAP1H.6	C0CAP1H.5	C0CAP1H.4	C0CAP1H.3	C0CAP1H.2	C0CAP1H.1	C0CAP1H.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C0CAP2H** (9Ch) : High Capture/Compare Register of PCA0 MODULE2

C0CAP2H.7	C0CAP2H.6	C0CAP2H.5	C0CAP2H.4	C0CAP2H.3	C0CAP2H.2	C0CAP2H.1	C0CAP2H.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C0CAP3H** (9Dh) : High Capture/Compare Register of PCA0 MODULE3

C0CAP3H.7	C0CAP3H.6	C0CAP3H.5	C0CAP3H.4	C0CAP3H.3	C0CAP3H.2	C0CAP3H.1	C0CAP3H.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C0CAP4H** (9Eh) : High Capture/Compare Register of PCA0 MODULE4

C0CAP4H.7	C0CAP4H.6	C0CAP4H.5	C0CAP4H.4	C0CAP4H.3	C0CAP4H.2	C0CAP4H.1	C0CAP4H.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C0CAP5H** (9Fh) : High Capture/Compare Register of PCA0 MODULE5

C0CAP5H.7	C0CAP5H.6	C0CAP5H.5	C0CAP5H.4	C0CAP5H.3	C0CAP5H.2	C0CAP5H.1	C0CAP5H.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **P2** (A0h) : Port 2 Register

P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- ◆ Quasi-bidirectional port with internal pull-up resistors.
- ◆ Address output when external memory access and general I/O.

■ **SBUF1** (A1h) : Serial Data Buffer Register of UART1

SBUF1.7	SBUF1.6	SBUF1.5	SBUF1.4	SBUF1.3	SBUF1.2	SBUF1.1	SBUF1.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ The transmission buffer and the reception buffer are separated.
- ◆ The transmission/reception buffers have the same address.

■ **C0CAPM0** (A2h) : Mode Control Register of PCA0 MODULE0

IPWM0	ECOM0	CAPP0	CAPN0	MAT0	TOG0	PWM0	ECCF0
R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- IPWM0 : Inverted PWM output.
  If this bit is set, the PWM output is high when C0L ≥ C0CAPmL.
  The change of this bit will take effect from the next overflow / match time of PWM.
- ECOM0 : Enable comparator.
  ECOM0 = 1 enables the comparator function.
- CAPP0 : Capture positive.
  CAPP0 = 1 enables positive edge capture.
- CAPN0 : Capture negative.
  CAPN0 = 1 enables negative edge capture.
- MAT0 : Match.
  When MAT0 = 1, a match of the PCA counter with this module's comparator/capture register causes the CCF0 bit in C0CON to be set, flagging an interrupt.
- TOG0 : Toggle.
  When TOG0 = 1, a match of the PCA counter with this module's compare/capture register causes the C0EX0 pin to toggle.
- PWM0 : Pulse width modulation mode.
  PWM0 = 1 enables the C0EX0 pin to be used as a pulse width modulated output.
- ECCF0 : Enable CCF interrupt.
  Enables compare/capture flag CCF0 in the C0CON register to generate an interrupt.

■ **C0CAPM1** (A3h) : Mode Control Register of PCA0 MODULE1

IPWM1	ECOM1	CAPP1	CAPN1	MAT1	TOG1	PWM1	ECCF1
R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C0CAPM2** (A4h) : Mode Control Register of PCA0 MODULE2

IPWM2	ECOM2	CAPP2	CAPN2	MAT2	TOG2	PWM2	ECCF2
R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C0CAPM3** (A5h) : Mode Control Register of PCA0 MODULE3

IPWM3	ECOM3	CAPP3	CAPN3	MAT3	TOG3	PWM3	ECCF3
R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C0CAPM4** (A6h) : Mode Control Register of PCA0 MODULE4

IPWM4	ECOM4	CAPP4	CAPN4	MAT4	TOG4	PWM4	ECCF4
R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C0CAPM5** (A7h) : Mode Control Register of PCA0 MODULE5

IPWM5	ECOM5	CAPP5	CAPN5	MAT5	TOG5	PWM5	ECCF5
R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

Appendix B : SFR Description [A8h ~ ADh] (8/20)

■ **IE** (A8h) : Interrupt Enable Register

EA	EADC	ET2	ES	ET1	EX1	ET0	EX0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- EA : Global interrupt enable.
- EADC : ADC interrupt enable.
- ET2 : Timer 2 interrupt enable.
- ES : Serial port interrupt enable.
- ET1 : Timer 1 interrupt enable.
- EX1 : External interrupt 1 enable.
- ET0 : Timer0 interrupt enable.
- EX0 : External interrupt 0 enable.

■ **SADDR** (A9h) : Slave Address Register of UART0

SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- Programmed with the given or broadcast address assigned to serial port 0.

■ **SADDR1** (AAh) : Slave Address Register of UART1

SADDR1.7	SADDR1.6	SADDR1.5	SADDR1.4	SADDR1.3	SADDR1.2	SADDR1.1	SADDR1.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- Programmed with the given or broadcast address assigned to serial port 1.

■ **SADEN1** (ABh) : Slave Address Mask Enable Register of UART1

SADEN1.7	SADEN1.6	SADEN1.5	SADEN1.4	SADEN1.3	SADEN1.2	SADEN1.1	SADEN1.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C0CON** (ACh) : PCA0 Counter Control Register

CF	CR	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- CF : PCA counter overflow flag.
- CR : PCA counter run control bit.
  Set by software to turn the PCA counter on.
- CCF5 : MODULE5 interrupt flag.
  Set by hardware when a match or capture occurs.
  Must be cleared by software.
- CCF[4:0] : MODULE4~0 interrupt flag.

■ **C0MOD** (ADh) : PCA0 Counter Mode Register

CIDL	PWMDYN	PWM16	CPS3	CPS2	CPS1	CPS0	ECF
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- CIDL : Counter Idle Control.
  CIDL = 0 programs the PCA counter to continue functioning during Idle Mode.
  CIDL = 1 programs it to be stop during Idle Mode.
- PWMDYN: Dynamic PWM bit.
  If this bit is set, the dynamic PWM is generated.
  C0L is cleared when a match occurs between C0L and C0H.
  The match signal replaces the overflow signal for PWM.
- PWM16 : Enable 16-bit PWM generation.
  If this bit is set, two timer counter modules are paired to generate one 16-bit PWM output.
- CPS[3:0] : PCA count rate (F_{PCA}) select.
- ECF : Enable PCA counter overflow interrupt.
  ECF = 1 enables CF bit int C0CON to generate an interrupt.
  ECF = 0 disables that function.

■ **C0L** (AEh) : Low Byte Register of PCA0 Counter

C0L.7	C0L.6	C0L.5	C0L.4	C0L.3	C0L.2	C0L.1	C0L.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C0H** (AFh) : High Byte Register of PCA0 Counter

C0H.7	C0H.6	C0H.5	C0H.4	C0H.3	C0H.2	C0H.1	C0H.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **P3** (B0h) : Port 3 Register

P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- Quasi-bidirectional port with internal pull-up resistors.
- When alternative function enabled, P3.X must be "1".

■ **SCON1** (B1h) : Serial Port Control Register of UART1

SM0	SM1	SM2	REN	TB8	RB8	TI	RI
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- SM0, SM1 : Serial Port mode select.
  [0,0] : Mode0, 8-bit shift register (F_{PERI}/4)
  [0,1] : Mode1, 8-bit UART (Variable)
  [1,0] : Mode2, 9-bit UART (F_{PERI}/32 or F_{PERI}/16)
  [1,1] : Mode3, 9-bit UART (Variable)
- SM2 : Enables the Automatic Address Recognition in Mode2 and 3.
  In Mode 1, the Validity of the Stop Bit is checked if SM2=1.
  In Mode0, SM2 should be "0".
- REN : Enable/Disable Reception.
- TB8 : 9th data bit that will be transmitted in Mode2 and 3.
- RB8 : 9th data bit that was received in Mode 2 and 3.
  In Mode1, RB8 is equal to stop bit if SM2 is "0".
  In Mode0, RB8 is not used.
- TI : Transmission interrupt flag. Must be cleared by S/W.
- RI : Reception interrupt flag. Must be cleared by S/W.

■ **IT** (B2h) : Interrupt Type Selection Register

EI2C	FI2C	PI2C	I2C_EN	IT5	IT4	IT3	IT2
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- EI2C : I2C Interrupt Enable Flag
- FI2C : I2C Interrupt Flag
- PI2C : I2C Interrupt Priority
- I2C_EN : Normal I2C Enable Flag
  [0] : Normal I2C Disable
  [1] : Normal I2C Enable
- IT5 : Interrupt5 Type Selection Flag
  [0] : Level detect
  [1] : Edge detect
- IT4 : Interrupt4 Type Selection Flag
  [0] : Level detect
  [1] : Edge detect
- IT3 : Interrupt3 Type Selection Flag
  [0] : Level detect
  [1] : Edge detect
- IT2 : Interrupt2 Type Selection Flag
  [0] : Level detect
  [1] : Edge detect

■ **P0TYPE** (B3h) : Port 0 Type Register

P0TYPE.7	P0TYPE.6	P0TYPE.5	P0TYPE.4	P0TYPE.3	P0TYPE.2	P0TYPE.1	P0TYPE.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

◆ 0 = Push-pull Output / 1 = Open-drain Output (Default)

■ **P1TYPE** (B4h) : Port 1 Type Register

P1TYPE.7	P1TYPE.6	P1TYPE.5	P1TYPE.4	P1TYPE.3	P1TYPE.2	P1TYPE.1	P1TYPE.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

◆ 0 = Push-pull Output / 1 = quasi-bidirectional Output (Default)

■ **P2TYPE** (B5h) : Port 2 Type Register

P2TYPE.7	P2TYPE.6	P2TYPE.5	P2TYPE.4	P2TYPE.3	P2TYPE.2	P2TYPE.1	P2TYPE.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

◆ 0 = Push-pull Output / 1 = quasi-bidirectional Output (Default)

■ **P3TYPE** (B6h) : Port 3 Type Register

P3TYPE.7	P3TYPE.6	P3TYPE.5	P3TYPE.4	P3TYPE.3	P3TYPE.2	P3TYPE.1	P3TYPE.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

◆ 0 = Push-pull Output / 1 = quasi-bidirectional Output (Default)

■ **IPH** (B7h) : Interrupt Priority High Register

-	PADCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
R(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

◆ PADCH : ADC interrupt priority high.
◆ PT2H : Timer 2 interrupt priority high.
◆ PSH : Serial port interrupt priority high.
◆ PT1H : Timer 1 interrupt priority high.
◆ PX1H : External interrupt 1 priority high.
◆ PT0H : Timer 0 interrupt priority high.
◆ PX0H : External interrupt 0 priority high.

■ **IP** (B8h) : Interrupt Priority Low Register

-	PADC	PT2	PS	PT	PX	PT0	PX0
R(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

◆ PADC : ADC interrupt priority low.
◆ PT2 : Timer 2 interrupt priority low.
◆ PS : Serial port interrupt priority low.
◆ PT1 : Timer 1 interrupt priority low.
◆ PX1 : External interrupt 1 priority low.
◆ PT0 : Timer 0 interrupt priority low.
◆ PX0 : External interrupt 0 priority low.

■ **SADEN** (B9h) : Slave Address Mask Enable Register of UART0

SADEN.7	SADEN.6	SADEN.5	SADEN.4	SADEN.3	SADEN.2	SADEN.1	SADEN.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **ITSEL** (BAh) : Interrupt Polarity Selection Register

-	-	ITSEL5	ITSEL4	ITSEL3	ITSEL2	ITSEL1	ITSEL0
-	-	R/W(0)	R/W(1)	R/W(0)	R/W(1)	R/W(0)	R/W(0)

◆ ITSEL5 : Interrupt5 Polarity Selection Flag
[0] : low level or negative edge detect
[1] : high level or positive edge detect

◆ ITSEL4 : Interrupt4 Polarity Selection Flag
[0] : low level or negative edge detect
[1] : high level or positive edge detect

◆ ITSEL3 : Interrupt3 Polarity Selection Flag
[0] : low level or negative edge detect
[1] : high level or positive edge detect

◆ ITSEL2 : Interrupt2 Polarity Selection Flag
[0] : low level or negative edge detect
[1] : high level or positive edge detect

◆ ITSEL1 : Interrupt1 Polarity Selection Flag
[0] : low level or negative edge detect
[1] : high level or positive edge detect

◆ ITSEL0 : Interrupt0 Polarity Selection Flag
[0] : low level or negative edge detect
[1] : high level or positive edge detect

■ **P0DIR** (BBh) : Port 0 Input/Output Control Register

P0DIR.7	P0DIR.6	P0DIR.5	P0DIR.4	P0DIR.3	P0DIR.2	P0DIR.1	P0DIR.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

◆ 1 = Input (Default) / 0 = Output

■ **P2DIR** (BDh) : Port 2 Input/Output Control Register

P2DIR.7	P2DIR.6	P2DIR.5	P2DIR.4	P2DIR.3	P2DIR.2	P2DIR.1	P2DIR.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

◆ 1 = Input (Default) / 0 = Output

■ **P3DIR** (BEh) : Port 3 Input/Output Control Register

P3DIR.7	P3DIR.6	P3DIR.5	P3DIR.4	P3DIR.3	P3DIR.2	P3DIR.1	P3DIR.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

◆ 1 = Input (Default) / 0 = Output

■ **AUXAD** (BFh) : High Address Register for MOVX with Ri

AUXAD.7	AUXAD.6	AUXAD.5	AUXAD.4	AUXAD.3	AUXAD.2	AUXAD.1	AUXAD.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

◆ If ENAUX bit (IOCFG.3) is set, "MOVX A, @Ri" and "MOVX @Ri, A" instructions refer to AUXAD instead of P2 register for high address.

■ **P1DIR** (BCh) : Port 1 Input/Output Control Register

P1DIR.7	P1DIR.6	P1DIR.5	P1DIR.4	P1DIR.3	P1DIR.2	P1DIR.1	P1DIR.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

◆ 1 = Input (Default) / 0 = Output

■ PLLCON (C1h) : PLL Control Register

LOCK	-	icp1	icp0	Dly_ctr	Ph_sel	PLLPD	PLLBP
R (0)		R/W(0)	R/W(1)	R/W(1)	R/W(0)	R/W(1)	R/W(0)

- ◆ PLLBP : [1] : PLL Bypass Mode (Input ☐ Output)
  [0] : PLL Normal Mode
- ◆ PLLPD : [1] : PLL Power Down
  [0] : PLL Active
- ◆ Ph_sel : PFD phase control
- ◆ Dly_ctr : PFD delay control
- ◆ icp[1:0] : CP current control
- ◆LOCK : [1] : PLL Lock
  [0] : PLL unlock

■ PLLNR (C2h) : PLL Input Divider Register

-	-	-	-	Odiv1	Odiv0	Rdiv1	Rdiv0
-	-	-	-	R/W(1)	R/W(0)	R/W(1)	R/W(0)

- ◆ Rdiv[1:0] : Input 2-bit divider
- ◆ Odiv[1:0] : Output 2-bit divider

■ PLLFR (C3h) : PLL Feedback Divider Register

F7	F6	F5	F4	F3	F2	F1	F0
R/W (0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ F[7:0] : Feedback 8-bit divider

■ PMR (C4h) : Power Management Control Register

-	-	-	-	XTOFF	ALEOFF	WCLKE	WIOE
				R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ XTOFF : [1] : External crystal Oscillator disable.
  [0] : External crystal will restart (Default).
- ◆ ALEOFF : [1] : ALE toggling disable.
  [0] : ALE toggling enable (Default).
- ◆ WUCLK_EN : [1] : Wakeup CLK Enable
  [0] : Wakeup CLK Disable (Default)
- ◆ WUIO_EN : [1] : Wakeup IO Enable
  [0] : Wakeup IO Disable (Default)

■ STATUS (C5h) : Crystal Status Register

-	-	-	XTUP	-	-	-	-
			R(1)				

- ◆ XTUP : Crystal Oscillator warm-up status.
  It represents if the crystal clock is stable(1) or not(0).
  Cleared by H/W if XTOFF is set or if PD is set and WDT is not enabled.
  Set by H/W after crystal stabilization time.

■ OSCICN (C6h) : Internal Ring Oscillator Control Register

-	-	-	-	DIV2	RINGON	DIV1	DIV2
				R/W(0)	R/W(1)	R/W(0)	R/W(0)

- RINGON : 1 = Internal ring Oscillator is running.
  0 = Internal ring Oscillator is killed.
  Don't clear RINGON bit when XTRG = 0.
- DIV[2:0] : Ring Oscillator divider. (F_{OSC} : 12MHz)
  [0,0,0] = $F_{OSC}/3$
  [0,0,1] = $F_{OSC}/6$
  [0,1,0] = $F_{OSC}/12$
  [0,1,1] = $F_{OSC}/24$
  [1,0,0] = $F_{OSC}/1$
  [1,0,1] = $F_{OSC}/2$
  [1,1,0] = $F_{OSC}/4$
  [1,1,1] = $F_{OSC}/8$

■ IOCFG (C7h) : I/O Configuration Register

-	-	-	-	ENAUX	-	-	-
				R/W(0)			

- ENAUX : Select AUXAD for MOVX with Ri.
  1 = AUXAD register serves high address for MOVX with Ri.
  0 = P2 register serves high address for MOVX with Ri.

■ T2CON (C8h) : Timer/Counter 2 Control Register

TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- TF2 : Timer 2 overflow flag.
- EXF2 : Timer 2 external flag.
- RCLK : Receive clock flag.
- TCLK : Transmit clock flag.
- EXEN2 : Timer 2 external enable flag.
- TR2 : Timer 2 run flag.
- C/T2 : Timer 2 Timer/Counter select. When set, counter by T2.
- CP/RL2 : Capture/Reload flag.
  CP/RL2 = 0, Reload. (TH2,TL2) ← (RCAP2H,RCAP2L)
  CP/RL2 = 1, Capture. (RCAP2H,RCAP2L) ← (TH2,TL2)

■ T2MOD (C9h) : Timer/Counter 2 Mode Control Register

-	-	-	-	-	-	T2OE	DCEN
						R/W(0)	R/W(0)

- T2OE : Timer 2 clock output enable. When set, clock output to P1.0.
- DCEN : Timer 2 down count enable. When set, count down.

■ **RCAP2L** (CAh) : Timer/Count 2 Capture/Reload Low Byte Register

RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **RCAP2H** (CBh) : Timer/Counter 2 Capture/Reload High Byte Register

RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **TL2** (CCh) : Timer/Counter 2 Low Byte Register

TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **TH2** (CDh) : Timer/Counter 2 High Byte Register

TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C1CON** (CEh) : PCA1 Counter Control Register

CF	CR	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ CF : PCA counter overflow flag.
- ◆ CR : PCA counter run control bit.
  Set by software to turn the PCA counter on.
- ◆ CCF5 : MODULE5 interrupt flag.
  Set by hardware when a match or capture occurs.
  Must be cleared by software.
- ◆ CCF4 : MODULE4 interrupt flag.
- ◆ CCF3 : MODULE3 interrupt flag.
- ◆ CCF2 : MODULE2 interrupt flag.
- ◆ CCF1 : MODULE1 interrupt flag.
- ◆ CCF0 : MODULE0 interrupt flag.

■ **C1MOD** (CFh) : PCA1 Counter Mode Register

CIDL	PWMDYN	-	CPS3	CPS2	CPS1	CPS0	ECF
R/W(0)	R/W(0)		R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ CIDL : Counter Idle control.
  CIDL = 0 programs the PCA counter to continue functioning during Idle Mode.
  CIDL = 1 programs it to be stop during Idle Mode.
- ◆ PWMDYN: Dynamic PWM bit.
  If this bit is set, the dynamic PWM is generated.
  C1L is cleared when a match occurs between C1L and C1H.
  The match signal replaces the overflow signal for PWM.
- ◆ CPS[3:0] : PCA prescaler rate (F_{PCA}) selection.
- ◆ ECF : Enable PCA counter overflow interrupt.
  ECF = 1 enables CF bit int C1CON to generate an interrupt.
  ECF = 0 disables that function.

■ **PSW** (D0h) : Program Status Word Register

CY	AC	F0	RS1	RS0	OV	F1	P
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R(0)

- CY : Carry Flag.
- AC : Auxiliary carry flag.
- F0 : User flag 0.
- RS1, RS0 : Register bank select
  [0,0] : Bank 0
  [0,1] : Bank 1
  [1,0] : Bank 2
  [1,1] : Bank 3
- OV : Overflow flag.
- F1 : User flag 1.
- P : Parity bit. Set/clear by H/W according to ACC odd parity.

■ **P0SEL** (D1h) : Port 0 Pull-up Control Register

P0SEL.7	P0SEL.6	P0SEL.5	P0SEL.4	P0SEL.3	P0SEL.2	P0SEL.1	P0SEL.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- 0 = Pull-up resistor ON
- 1 = Pull-up resistor OFF when ADC_EN (ADCON[7]) = 1 (Default)

■ **C1CAP0L** (D2h) : Low Capture/Compare Register of PCA1 MODULE0

C1CAP0L.7	C1CAP0L.6	C1CAP0L.5	C1CAP0L.4	C1CAP0L.3	C1CAP0L.2	C1CAP0L.1	C1CAP0L.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C1CAP1L** (D3h) : Low Capture/Compare Register of PCA1 MODULE1

C1CAP1L.7	C1CAP1L.6	C1CAP1L.5	C1CAP1L.4	C1CAP1L.3	C1CAP1L.2	C1CAP1L.1	C1CAP1L.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C1CAP2L** (D4h) : Low Capture/Compare Register of PCA1 MODULE2

C1CAP2L.7	C1CAP2L.6	C1CAP2L.5	C1CAP2L.4	C1CAP2L.3	C1CAP2L.2	C1CAP2L.1	C1CAP2L.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C1CAP3L** (D5h) : Low Capture/Compare Register of PCA1 MODULE3

C1CAP3L.7	C1CAP3L.6	C1CAP3L.5	C1CAP3L.4	C1CAP3L.3	C1CAP3L.2	C1CAP3L.1	C1CAP3L.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C1CAP4L** (D6h) : Low Capture/Compare Register of PCA1 MODULE4

C1CAP4L.7	C1CAP4L.6	C1CAP4L.5	C1CAP4L.4	C1CAP4L.3	C1CAP4L.2	C1CAP4L.1	C1CAP4L.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C1CAP5L** (D7h) : Low Capture/Compare Register of PCA1 MODULE5

C1CAP5L.7	C1CAP5L.6	C1CAP5L.5	C1CAP5L.4	C1CAP5L.3	C1CAP5L.2	C1CAP5L.1	C1CAP5L.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **WDCON** (D8h) : Watchdog Timer & Power Status Register

-	POR	EPFI	PFI	WDIF	WTRF	EWT	RWT
	R/W(1)	R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- POR : Power-on reset flag.
- EPFI : Enable power-fail interrupt.
- PFI : Power-fail interrupt flag.
- WDIF : Watchdog timer interrupt flag.
- WTRF : Watchdog timer reset flag.
- EWT : Watchdog timer reset enable.
- RWT : Restart watchdog tier.

■ **P1SEL** (D9h) : Port 1 Pull-up Control Register

P1SEL.7	P1SEL.6	P1SEL.5	P1SEL.4	P1SEL.3	P1SEL.2	P1SEL.1	P1SEL.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- 0 = Pull-up resistor ON (Default)
- 1 = Pull-up resistor OFF when ADC_EN (ADCON[7]) = 1

■ **C1CAP0H** (DAh) : High Capture/Compare Register of PCA1 MODULE0

C1CAP0H.7	C1CAP0H.6	C1CAP0H.5	C1CAP0H.4	C1CAP0H.3	C1CAP0H.2	C1CAP0H.1	C1CAP0H.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C1CAP1H** (DBh) : High Capture/Compare Register of PCA1 MODULE1

C1CAP1H.7	C1CAP1H.6	C1CAP1H.5	C1CAP1H.4	C1CAP1H.3	C1CAP1H.2	C1CAP1H.1	C1CAP1H.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C1CAP2H** (DCh) : High Capture/Compare Register of PCA1 MODULE2

C1CAP2H.7	C1CAP2H.6	C1CAP2H.5	C1CAP2H.4	C1CAP2H.3	C1CAP2H.2	C1CAP2H.1	C1CAP2H.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C1CAP3H** (DDh) : High Capture/Compare Register of PCA1 MODULE3

C1CAP3H.7	C1CAP3H.6	C1CAP3H.5	C1CAP3H.4	C1CAP3H.3	C1CAP3H.2	C1CAP3H.1	C1CAP3H.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C1CAP4H** (DEh) : High Capture/Compare Register of PCA1 MODULE4

C1CAP4H.7	C1CAP4H.6	C1CAP4H.5	C1CAP4H.4	C1CAP4H.3	C1CAP4H.2	C1CAP4H.1	C1CAP4H.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C1CAP5H** (DFh) : High Capture/Compare Register of PCA1 MODULE5

C1CAP5H.7	C1CAP5H.6	C1CAP5H.5	C1CAP5H.4	C1CAP5H.3	C1CAP5H.2	C1CAP5H.1	C1CAP5H.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **ACC** (E0h) : Accumulator

ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **P2SEL** (E1h) : Port 2 Pull-up Control Register

P2SEL.7	P2SEL.6	P2SEL.5	P2SEL.4	P2SEL.3	P2SEL.2	P2SEL.1	P2SEL.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- 0 = Pull-up resistor ON (Default)
- 1 = Pull-up resistor OFF when ADC_EN (ADCON[7]) = 1

■ **C1CAPM0** (E2h) : Mode Control Register of PCA1 MODULE0

IPWM0	ECOM0	CAPP0	CAPN0	MAT0	TOG0	PWM0	ECCF0
R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- IPWM0 : Inverted PWM output.
  If this bit is set, the PWM output is high when C1L ≥ C1CAPmL.
  The change of this bit will take effect from the next overflow / match time of PWM.
- ECOM0 : Enable comparator.
  ECOM0 = 1 enables the comparator function.
- CAPP0 : Capture positive.
  CAPP0 = 1 enables positive edge capture.
- CAPN0 : Capture negative.
  CAPN0 = 1 enables negative edge capture.
- MAT0 : Match.
  When MAT0 = 1, a match of the PCA counter with this module's comparator/capture register causes the CCF0 bit in C1CON to be set, flagging an interrupt.
- TOG0 : Toggle.
  When TOG0 = 1, a match of the PCA counter with this module's comparator/capture register causes the C0EX0 pin to toggle.
- PWM0 : Pulse width modulation mode.
  PWM0 = 1 enables the C0EX0 pin to be used as a pulse width modulated output.
- ECCF0 : Enable CCF interrupt.
  Enables compare/capture flag CCF0 in the C1CON register to generate an interrupt.

Appendix B : SFR Description [E3h ~ EBh] (18/20)

■ **C1CAPM1** (E3h) : Mode Control Register of PCA1 MODULE1

IPWM1	ECOM1	CAPP1	CAPN1	MAT1	TOG1	PWM1	ECCF1
R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C1CAPM2** (E4h) : Mode Control Register of PCA1 MODULE2

IPWM2	ECOM2	CAPP2	CAPN2	MAT2	TOG2	PWM2	ECCF2
R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C1CAPM3** (E5h) : Mode Control Register of PCA1 MODULE3

IPWM3	ECOM3	CAPP3	CAPN3	MAT3	TOG3	PWM3	ECCF3
R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C1CAPM4** (E6h) : Mode Control Register of PCA1 MODULE4

IPWM4	ECOM4	CAPP4	CAPN4	MAT4	TOG4	PWM4	ECCF4
R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C1CAPM5** (E7h) : Mode Control Register of PCA1 MODULE5

IPWM5	ECOM5	CAPP5	CAPN5	MAT5	TOG5	PWM5	ECCF5
R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **EIE** (E8h) : Extended Interrupt Enable Register

EPCA1	EPCA0	ES1	EWDT	EX5	EX4	EX3	EX2
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- EPCA1 : PCA1 interrupt enable
- EPCA0 : PCA0 interrupt enable
- ES1 : UART1 interrupt enable
- EWDT : Watchdog timer interrupt enable
- EX5 : External interrupt 5 enable.
- EX4 : External interrupt 4 enable.
- EX3 : External interrupt 3 enable.
- EX2 : External interrupt 2 enable.

■ **P3SEL** (E9h) : Port 3 Pull-up Control Register

P3SEL.7	P3SEL.6	P3SEL.5	P3SEL.4	P3SEL.3	P3SEL.2	P3SEL.1	P3SEL.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- 0 = Pull-up resistor ON (Default)
- 1 = Pull-up resistor OFF when ADC_EN (ADCON[7]) = 1

■ **C1L** (EAh) : Low Byte Register of PCA1 Counter

C1L.7	C1L.6	C1L.5	C1L.4	C1L.3	C1L.2	C1L.1	C1L.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C1H** (EBh) : High Byte Register of PCA1 Counter

C1H.7	C1H.6	C1H.5	C1H.4	C1H.3	C1H.2	C1H.1	C1H.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **ADCENB0** (ECh) : ADC Channel Enable Bar Register (P0 port)

ADCENB0.7	ADCENB0.6	ADCENB0.5	ADCENB0.4	ADCENB0.3	ADCENB0.2	ADCENB0.1	ADCENB0.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

◆ 0 = ADC0 channel ON / 1 = ADC0 channel OFF (Default)

■ **ADCENB1** (EDh) : ADC Channel Enable Bar Register (P1 port)

ADCENB1.7	ADCENB1.6	ADCENB1.5	ADCENB1.4	ADCENB1.3	ADCENB1.2	ADCENB1.1	ADCENB1.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

◆ 0 = ADC1 channel ON / 1 = ADC0 channel OFF (Default)

■ **ADCENB2** (EEh) : ADC Channel Enable Bar Register (P2 port)

ADCENB2.7	ADCENB2.6	ADCENB2.5	ADCENB2.4	ADCENB2.3	ADCENB2.2	ADCENB2.1	ADCENB2.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

◆ 0 = ADC2 channel ON / 1 = ADC0 channel OFF (Default)

■ **ADCENB3** (EFh) : ADC Channel Enable Bar Register (P3 port)

ADCENB3.7	ADCENB3.6	ADCENB3.5	ADCENB3.4	ADCENB3.3	ADCENB3.2	ADCENB3.1	ADCENB3.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

◆ 0 = ADC3 channel ON / 1 = ADC0 channel OFF (Default)

■ **B** (F0h) : Second Accumulator

B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **FAEN** (F7h) : IAP Routine Access Enable Register

-	-	-	-	-	-	-	FLASH_AEN
							R/W(0)

◆ FLASH_AEN : IAP routine access enable.

■ **EIP** (F8h) : Extended Interrupt Priority Register

PPCA1	PPCA0	PS1	PWDT	RX5	PX4	PX3	PX2
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

◆ PPCA1 : PCA1 interrupt priority bit.
◆ PPCA0 : PCA0 interrupt priority bit.
◆ PS1 : UART1 interrupt priority bit.
◆ PWDT : Watchdog timer interrupt priority bit.
◆ PX5 : External interrupt 5 priority bit.
◆ PX4 : External interrupt 4 priority bit.
◆ PX3 : External interrupt 3 priority bit.
◆ PX2 : External interrupt 2 priority bit.

Appendix B : SFR Description [F9h ~ FBh] (20/20)

■ **UINDX** (F9h) : Wakeup/I2C Index Register

I2C_BS	I2C_RXP	-	UINDX4	UINDX3	UINDX2	UINDX1	UINDX0
R (0)	R/W(1)	-	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

◆ I2C_BS : I2C Busy Flag
[0] : Idle
[1] : Busy

◆ I2C_RXP : I2C RX FIFO pop
[0] : Idle
[1] : Pop FIFO, and move data to UDATA SFR (cleared automatically by H/W)

◆ UINDX[4:0] : Wakeup Index Register
[10000] : I2C RX FIFO read indirect address
[10001] : I2C TX FIFO write indirect address
[10010] : I2C RX FIFO pointer indirect address
[10011] : I2C TX FIFO pointer indirect address
[0XXXX] : Wakeup Register

■ **UDATA** (FAh) : Wakeup/I2C Data Register

UDAT7	UDAT6	UDAT5	UDAT4	UDAT3	UDAT2	UDAT1	UDAT0
R/W(0)	R/W(1)	R/W(1)	R/W(0)	R/W(0)	R/W(1)	R/W(1)	R/W(1)

◆ UDATA[7:0] : Wakeup Data Register

■ **CLKSEL** (FBh) : Wakeup/I2C Data Register

-	-	-	XR/HF	WDEM	XR/PL	RG/PR	OSC32EB
-	-	-	R/W(0)	R/W(0)	R/W(1)	R/W(1)	R/W(0)

◆ XT/HF : XTAL division flag ([1] : XTAL/2 division)

◆ WDEM : Watchdog timer extension mode select
[0] : default mode
CKCON.WD[1:0] [0,0] : 217 clocks (interrupt), 217 + 512 clocks (reset)
CKCON.WD[1:0] [0,1] : 220 clocks (interrupt), 220 + 512 clocks (reset)
CKCON.WD[1:0] [1,0] : 223 clocks (interrupt), 223 + 512 clocks (reset)
CKCON.WD[1:0] [1,1] : 226 clocks (interrupt), 226 + 512 clocks (reset)
[1] : extension mode
CKCON.WD[1:0] [0,0] : 25 clocks (interrupt), 25 + 512 clocks (reset)
CKCON.WD[1:0] [0,1] : 28 clocks (interrupt), 28 + 512 clocks (reset)
CKCON.WD[1:0] [1,0] : 211 clocks (interrupt), 211 + 512 clocks (reset)
CKCON.WD[1:0] [1,1] : 214 clocks (interrupt), 214 + 512 clocks (reset)

◆ XR/PL : PLL clock / XTRG clock selection
[0] : PLL clock
[1] : XTAL / RING MUX clock

◆ RG/PR : Ring clock selection.
[0] : 32KHz ring clock for WDT power down.
[1] : 4MHz ring clock for normal operation.

◆ OSC_32K_ENB : 32KHz RING Enable Bar
[0] : 32KHz RING Enable
[1] : 32KHz RING DISABLE

Appendix C : Update History

- V1.1
  - ✓ Page 23 : Revise the default value of P0TYPE SFR
  - ✓ Page 24 : Revise the default value of P1TYPE SFR
  - ✓ Page 25 : Revise the default value of P2TYPE SFR
  - ✓ Page 26 : Revise the default value of P3TYPE SFR
  - ✓ Page 74 : Modify Crystal Oscillator Circuit
  - ✓ Page 76 : Modify ISP Connection
- V1.2
  - ✓ Page 66 : Revise the default value of ITSEL SFR
  - ✓ Modify SFR Register Name (CKSEL => CLKSEL)
- V1.3
  - ✓ Clock classify
    Fosc : F_{SYS} (System Clock) , F_{PERI} (Peripheral Clock)
  - ✓ Page 30 : Add Watch Dog Timer Example
  - ✓ Page 76 : Add PLL Fvco, Fsys Range
  - ✓ Page 79 : Add Power Down Mode Example
  - ✓ Page 90 : Add I2C Signal Characteristics
- V1.4
  - ✓ Remove LVD
  - ✓ Page 22~26 : Revise PnSEL SFR Control
  - ✓ Page 63 : Revise I2C Block diagram
  - ✓ Page 75 : Revise on the PLL Clock Setting slide
  - ✓ Page 79 : Revise ISP Connection
  - ✓ Page 85 : Add on the Power Slope slide
  - ✓ Page 86 : Add on the VDDIO Level
- V1.5
  - ✓ Remove Strong Point
  - ✓ Page 83~85: Add Clock Circuit Guideline
  - ✓ Page : Add recommended external POR
- V1.6
  - ✓ Page 9 : Add 32QFN package
  - ✓ Page 97 : Add 32QFN package dimension
- V1.7
  - ✓ Page 5 : Flash Endurance
- V1.8
  - ✓ Page 9 : Revise Pin1 Configurations(MLF/QFN32)