

age	Max. current
	100 mA
	100 mA
	100 mA
	20 mA
	20 mA

, which we extensively  
Spice and has proved to

t voltage and biases the  
431 reduces its cathode  
back set point, and the  
w the target, the TL431  
ED. As a result, the pri-  
ncrease the output volt-  
n accept two different

ular controllers such as  
duces the peak current  
X-based designs where

lls high the FB pin to  
y requires an inverting

whereas the divider net-  
drive the TL431 output  
r  $R_{upper} - R_{lower}$ . Thanks  
ole and thus roll off the  
ncy range, because  $C_{zero}$   
s as a controlled zener  
controls the shunt regu-  
sketch thus simplifies to  
ole zener diode. For the  
with its internal imped-  
these dynamic resistors  
alculation.

(3-53)

linking the quantity  
engender:  $I_c = I_1 CTR$ .  
ivative terms are zero

(3-54)

(3-55)

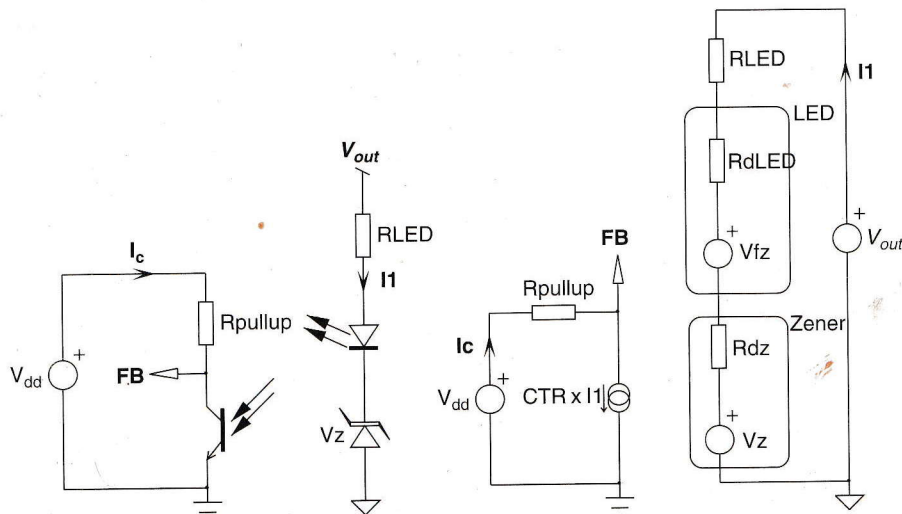


FIGURE 3-36 The small-signal model includes various dynamic resistors, but they are of low value compared to the series resistor  $R_{LED}$ .

This equation describes the "fast lane" gain that you simply cannot roll off. It also sheds light on the selection of  $R_{LED}$ : it obviously cannot be made solely on bias current considerations as it affects the loop gain. Bias current will rely on the resistor  $R_{bias}$  whose current does not cross the optocoupler LED and thus does not play a role in the gain definition. For Fig. 3-35b solution B, the result is almost similar to the Eq. (3-55) result, except that there is no phase reversal as with the common collector structure.

Once the operating principle is understood, the final TL431 representation makes more sense, as Fig. 3-37 shows. You can see the standard op amp having a capacitor  $C_{zero}$  but followed by an adder network representative of the fast lane. Note in Fig. 3-35b that the LED

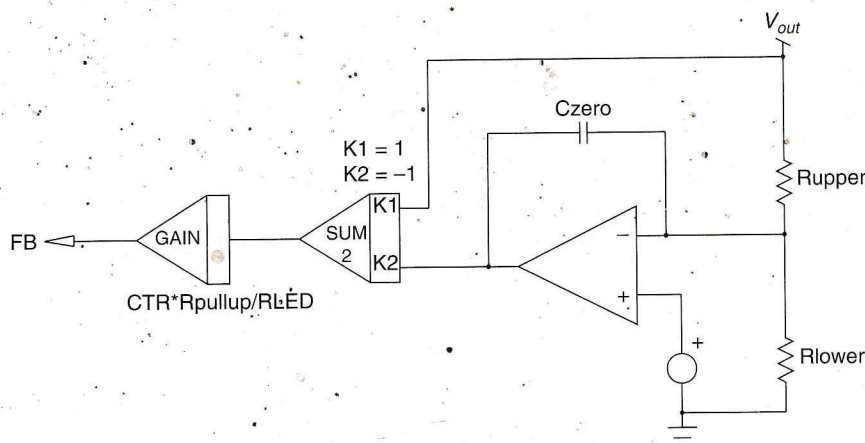


FIGURE 3-37 From this sketch, the fast lane can easily be identified.