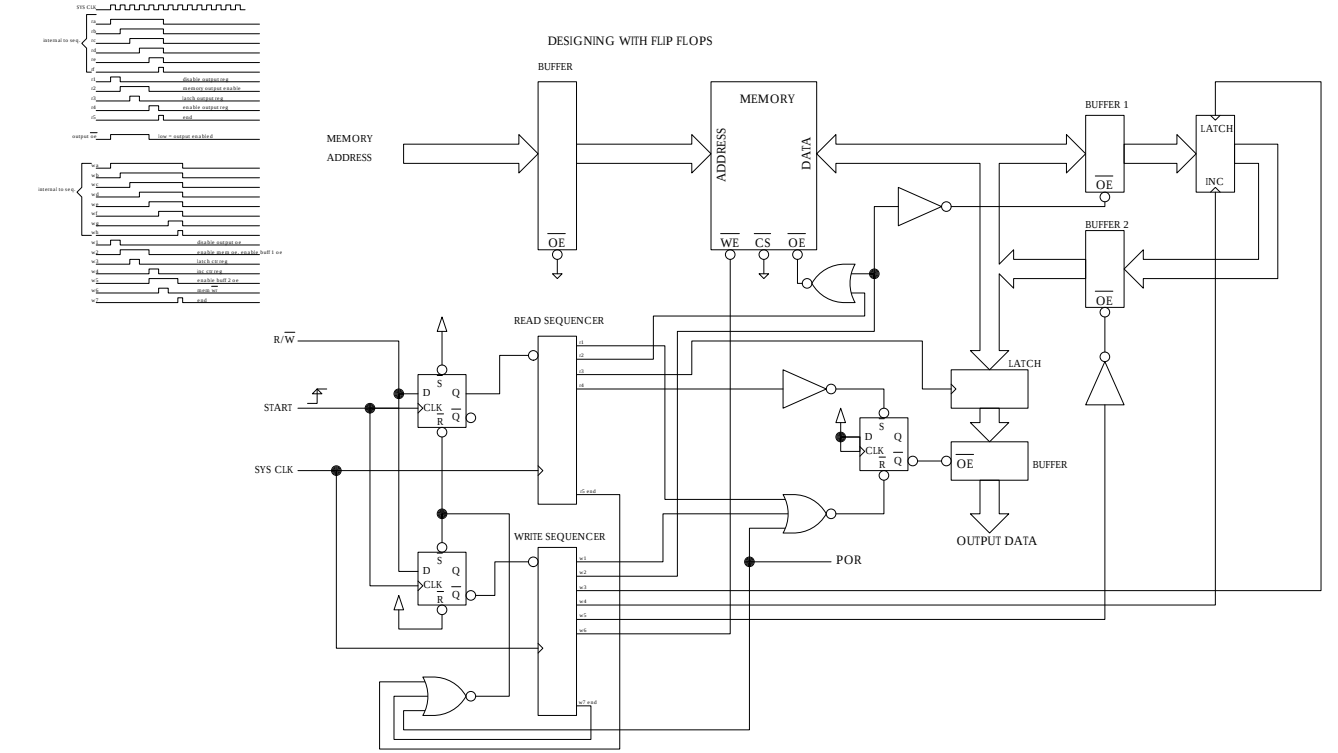
DESIGNING WITH FLIP FLOPS
BUFFER
MEMORY
MEMORY ADDRESS
ADDRESS
DATA
WE
CS
OE
BUFFER 1
BUFFER 2
LATCH
INC
READ SEQUENCER
WRITE SEQUENCER
R/W
START
SYS CLK
POR
LATCH
BUFFER
OUTPUT DATA
SYS CLK
internal to seq
output oe
low = output enabled
internal to seq
disable output reg
memory output enable
latch output reg
enable output reg
read
disable output oe
enable mem oe, enable buff 1 oe
latch ctr reg
dec ctr reg
enable buff 2 oe
mem wr
read