An Automotive Onboard 3.3-kW Battery Charger for PHEV Application

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***Abstract*—An onboard charger is responsible for charging the battery pack in a plug-in hybrid electric vehicle (PHEV). In this paper, a 3.3-kW two-stage battery charger design is presented for a PHEV application. The objective of the design is to achieve high efficiency, which is critical to minimize the charger size, charging time, and the amount and cost of electricity drawn from the utility. The operation of the charger power converter configuration is provided in addition to a detailed design procedure. The mechanical packaging design and key experimental results are provided to verify the suitability of the proposed charger power architecture.**

***Index Terms*—AC–DC power converters, batteries, dc–dc power converters, energy conservation, energy storage, power conversion.**

I. Introduction

A PLUG-IN hybrid electric vehicle (PHEV) is a hybrid vehicle with rechargeable batteries that can be restored to full charge by connecting the vehicle plug to an external electric power source. In recent years, PHEV motor drive and energy storage technology has developed at a rapid rate in response to expected market demand for PHEVs. Battery chargers are another key component required for the emergence and acceptance of PHEVs. For PHEV applications, the accepted approach involves using an onboard charger [1]. An onboard 3.3-kW charger can charge a depleted 16-kWh battery pack in PHEVs to 95% charge in about 4 h from a 240-V supply. The most common charger power architecture includes an ac–dc converter with power factor correction (PFC) [2] followed by an isolated dc–dc converter. Selecting the optimal topology and evaluating power loss in power semiconductors are important steps in the design and development of these battery chargers [3]. In this paper, a two-stage battery charger is presented, including an ac–dc converter with an interleaved boost PFC followed by a pulsewidth-modulated (PWM) zero-voltage switching (ZVS) full-bridge dc–dc converter. The charging solution presented achieves a peak efficiency of 93.6% while maintaining the ability to operate over a wide output voltage variation of 200 to 450 V. The solution achieves a compact size of 5.46 L, 6.2 kg in weight, and has dimensions of 273 × 200 × 100 mm. This paper presents the operation, design, and experimental results of the battery charging solution proposed.

Manuscript received December 9, 2011; revised May 4, 2012; accepted June 20, 2012. Date of publication July 25, 2012; date of current version October 12, 2012. This work was supported by the Delta-Q Technologies Corporation. This is a revised version of the paper that was presented at 2011 IEEE Vehicle Power Propulsion Conference, Chicago, IL. The review of this paper was coordinated by Dr. W. Zhuang.

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Digital Object Identifier 10.1109/TVT.2012.2210259

II. Proposed Two-Stage Battery Charger

The two-stage battery charger configuration is shown in Fig. 1. In this configuration, an interleaved boost PFC circuit is used for the front-end converter, which is followed by an isolated full-bridge dc–dc converter.

A. Front-End First-Stage AC–DC PFC Rectifier

The interleaved PFC consists of two continuous conduction mode (CCM) boost converters in parallel, which operate 180° out of phase [4]–[6]. The input current is the sum of the inductor currents in L_{B1} and L_{B2}, as shown in Fig. 2. Since the inductor ripple currents are out of phase, they tend to cancel each other and reduce the input ripple current. The maximum input inductor ripple current cancelation occurs at 50% of the duty cycle. Fig. 3 shows the ratio of the input current ripple to the inductor current ripple as a function of duty cycle.

The output capacitor current is the sum of the two boost diode currents minus the dc output current. Interleaving reduces the output capacitor ripple current as a function of the duty cycle [7]. As the duty cycle approaches 0%, 50%, and 100% duty cycles, the sum of the two diode currents approaches dc. At these points, the output capacitor only has to filter the inductor ripple current. Fig. 4 shows the normalized output capacitor current as a function of the duty cycle.

The interleaved boost converter inherently takes advantage of paralleled semiconductors to reduce conduction loss. Furthermore, by having the converters switched out of phase, it doubles the effective switching frequency, therefore reducing the input current ripple and resulting in a reduction of the size of the input electromagnetic interference (EMI) filter.

B. Second-Stage ZVS Full-Bridge DC–DC Converter

The phase-shifted ZVS PWM dc–dc full-bridge converter was presented in [8]–[10]. ZVS for the switches is realized by using the leakage inductance of the transformer, in addition to

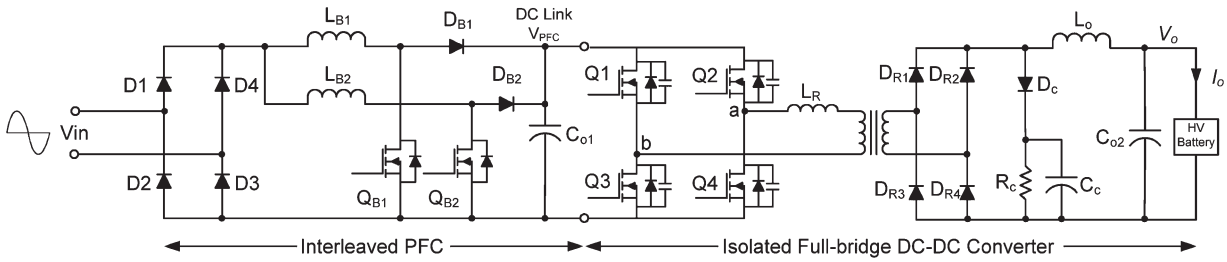

Fig. 1. Proposed battery charger configuration for a PHEV application.

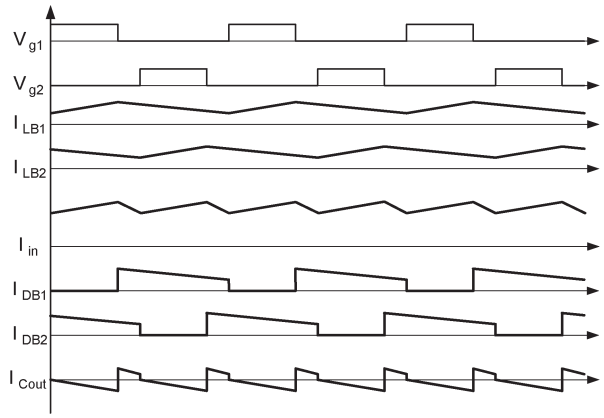

Fig. 2. Typical operating waveforms in an interleaved PFC converter with duty cycles less than 50%.

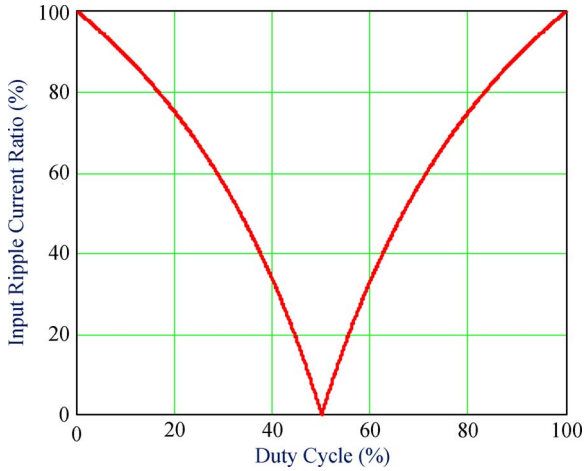

Fig. 3. Input ripple current ratio as a function of duty cycle in a two-channel interleaved PFC converter.

an external inductor and the output capacitance of the switch. Although various improvements have been suggested for this converter [11]–[20], all of them increase the component count and suffer from one or more disadvantages, including a limited ZVS range, high-voltage (HV) ringing on the secondary-side rectifier diodes, or loss of duty cycle. Wide ZVS range of operation is discussed in [12] and [17]–[19]. The HV ringing on the secondary-side rectifier diodes is addressed in [13], [15], [16], and [20]. The loss of duty cycle is reviewed in [14]. A new complementary gating scheme for the full-bridge dc–dc PWM converter is presented in [21]. This gating scheme requires an additional ZVT circuit to achieve ZVS for all the switches for a wide variation in the load current.

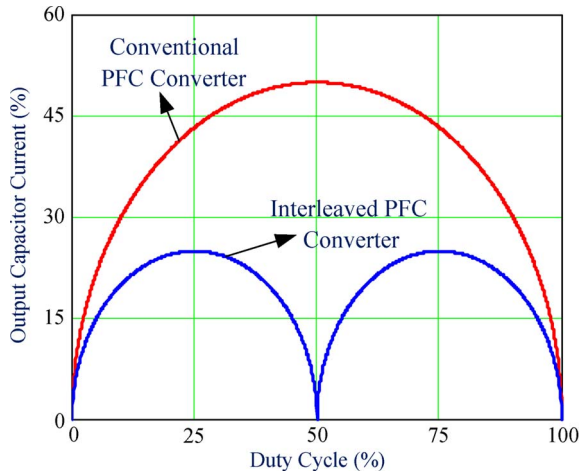

Fig. 4. Normalized output capacitor current as a function of duty cycle in a conventional PFC and a two-channel interleaved PFC converter.

The full-bridge ZVS converter presented here behaves similar to a traditional hard-switched topology, but rather than simultaneously driving the diagonal bridge switches, the lower switches (Q3 and Q4) are driven at a fixed 50% duty cycle, and the upper switches (Q1 and Q2) are PWM on the trailing edge [22], [23].

As shown in Fig. 1, the power semiconductor switches have been modeled with parallel diodes and parasitic capacitance. All parasitic capacitance values in the circuit, including winding and heat-sink capacitance, have been lumped together as switch capacitance.

The output rectifiers are considered ideal, and the external resonant inductor also includes the transformer leakage inductance. The beginning of the cycle, which is shown in Fig. 5, is arbitrarily set as having switches Q1 and Q4 on and Q2 and Q3 off. This is a power transfer period, and the primary current flows through Q1–transformer primary–L_R–Q4. This power transfer period terminates when switch Q1 turns off, as determined by the PWM signal. As the current flowing in the primary cannot be instantaneously interrupted, it finds an alternate path and flows through the parasitic switch capacitance of Q3 and Q1, which discharges the node b to 0 V and then forward biases the body diode D3.

The primary resonant inductor L_R maintains the current that circulates around the path of D3–transformer primary–L_R–Q4. When switch Q1 opens, the output inductor current freewheels through all four output diodes, i.e., $D_{R1}-D_{R4}$. During this transition, the output inductor current assists the resonant inductor in charging the upper and lower bridge metal-oxide semiconductor field-effect transistor (MOSFET) capacitances.

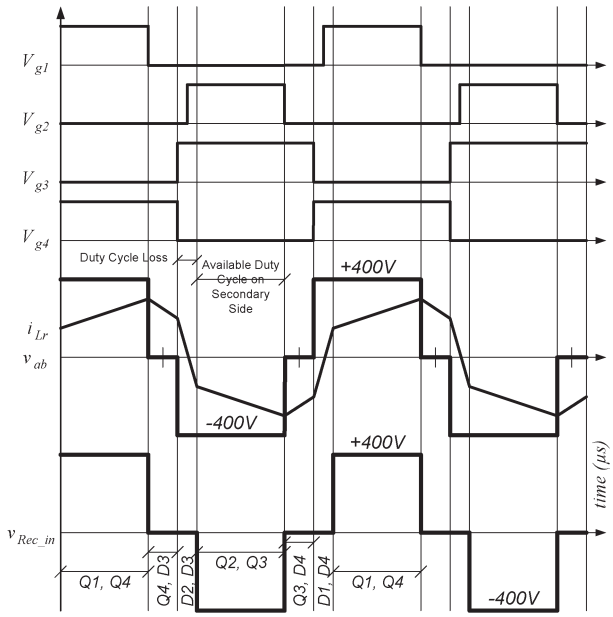

Fig. 5. Typical operating waveforms to illustrate the operation of the ZVS full-bridge converter.

At the end of the freewheeling period, Q3 and Q4 toggle. The actual timing of this toggle is dependent on the resonant delay that occurs prior to Q2 turning on.

The ZVS transition occurs during this resonant delay period after Q3 and Q4 toggle and before Q2 turns on. The required resonant delay is one fourth of the period of the $L_R \times C$ resonant frequency of the circuit formed by the resonant inductor and the parasitic capacitance. The resonant transition may be estimated by

$$\tau = \frac{\pi}{2} \frac{1}{\sqrt{\frac{1}{L_R \times C} - \frac{R^2}{4 \times (L_R)^2}}} \tag{1}$$

where τ is the resonant transition time, L_R is the leakage inductance, C is the parasitic capacitance, and R is the equivalent resistance in series with L_R and C.

When Q3 and Q4 toggle, the primary current that was flowing through Q4 now finds an alternate path and it charges/discharges the parasitic capacitance of switches Q4 and Q2 until the body diode of Q2 is forward biased. If the resonant delay is properly set, switch Q2 will be turned on with ZVS at this time. The output inductor does not assist this transition. It is purely a resonant transition driven by the resonant inductor.

The second power transfer period commences when Q2 turns on and primary current flows through Q2–L_R–transformer primary–Q3. The rest of the circuit operation can be explained in a similar manner.

A clamp network consisting of D_C, R_C, and C_C is needed across the output rectifier to clamp the voltage ringing due to diode junction capacitance with the leakage inductance of the transformer. This dc–dc converter also suffers from duty cycle loss, as shown in Fig. 5. Duty cycle loss occurs for converters requiring inductive output filters when the output rectifiers commutate, enabling all of the diodes to conduct, which effectively shorts the secondary winding [24]. This causes a decrease in the output voltage; thus, a higher transformer turn ratio is needed, which increases the primary peak current.

TABLE I
DESIGN SPECIFICATIONS OF THE PROPOSED CHARGER

Parameters	Value[Units]
Input AC Voltage	85 – 265 [V]
Maximum Input AC Current	16 [A]
Power Factor @ F.L. and 240 V in	99 [%]
AC Input Frequency	47 – 70 [Hz]
THD at F.L. and 240V in	< 5 [%]
Overall Efficiency	Up to 94 [%]
Output DC Voltage Range	200 to 450 [V]
Maximum Output DC Current	11 [A]
Maximum Output Power	3.3 [kW]
Output Voltage Ripple	< 2 [Vp-p]
Cooling	Liquid
Dimensions	273 x 200 x 100 [mm]
Mass/Volume	6.2 [Kg] / 5.46 [L]
Operating Temperature	-40°C to +105°C Ambient
Coolant Temperature	-40°C to +70°C

III. SPECIFICATIONS AND DESIGN OF THE PROPOSED CHARGER

Here, the design details for the two-stage 3.3-kW battery charger are provided. The charger is designed to meet the specifications given in Table I. The switching frequencies for the PFC and the dc–dc converter stages are selected to be 70 and 200 kHz, respectively. To achieve high efficiency (e.g., $> 97\%$) for the hard-switched interleaved PFC and to limit the fundamental switching frequency ripple to below 150 kHz to meet the EMI requirements, a switching frequency of 70 kHz was selected. An experimental efficiency comparison for the ZVS full-bridge dc–dc converter is provided in Fig. 6 at half-load power, (i.e., 1.65 kW) for switching frequencies between 66 and 250 kHz. At 66 kHz, the converter has maximum overall efficiency. Since the converter components, including the resonant inductor, the transformer, and the output inductor, were optimized for a 66-kHz operation, the efficiency is lower at 150, 200, and 250 kHz. However, since the difference in losses at full load is limited to 2.3%, a 200-kHz switching frequency was selected for the dc–dc stage. Finally, the magnetic components were redesigned for the final selected switching frequency of 200 kHz.

To design the interleaved PFC converter, it should be treated as two conventional boost PFC converters with each operating at half of the load power rating. With this approach, all

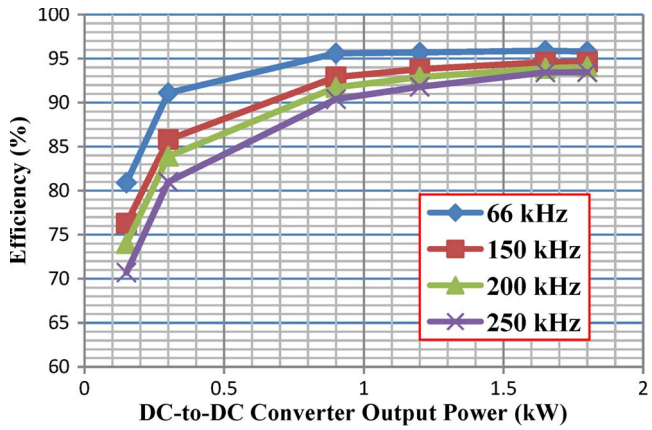

Fig. 6. Experimental measured efficiency for the second-stage dc–dc converter as a function of output power for different switching frequencies at $V_o = 300$ V and $P_o = 1.65$ kW.

equations for the inductor, the switch, and the diode in the conventional PFC remain valid since the stresses are unchanged, with the only exception being the reduced ripple current through the output capacitors.

The minimum required boost inductor value in each phase for a low line is given by

$$L_B = \frac{\sqrt{2}V_{\text{in\_min}} \times D_{\text{min\_LL}}}{f_s \times \Delta I_{\text{L-LL}}} \approx 400\ \mu\text{H} \tag{2}$$

where the minimum duty cycle at the low line is defined by

$$D_{\text{min\_LL}} = 1 - \frac{\sqrt{2}V_{\text{in\_min}}}{V_{\text{PFC\_bus}}} \sin\left(\frac{\pi}{2}\right). \tag{3}$$

In addition, $\Delta I_{\text{L-LL}}$ is the desired inductor current ripple at the low line.

The PFC bus capacitor is determined by the following:

$$C_{\text{PFC}} = \frac{2P_o \times T_{\text{Hold\_up}}}{{V_{\text{PFC\_bus}}}^2 (V_{\text{PFC\_bus}} - \Delta V_{\text{PFC\_bus}})^2} \tag{4}$$

where the maximum hold-up time required for the PFC bus is given by

$$T_{\text{Hold\_up}} = \frac{1}{4}\frac{1}{2 \times f_{\text{Line}}}. \tag{5}$$

Further, $\Delta V_{\text{PFC-bus}}$ is the intended low-frequency ripple across the PFC bus capacitor.

The high-frequency ripple current of the PFC capacitor contributed by the PFC stage can be obtained by

$$I_{\text{C\_HF}} = I_o \sqrt{\frac{16 \times V_{\text{PFC\_bus}}}{6\pi\sqrt{2} \times V_{\text{in\_min}}} - {\eta_{\text{PFC}}}^2} \tag{6}$$

where

$$I_o = \frac{P_o}{V_{\text{PFC\_bus}}}. \tag{7}$$

In addition, η_{PFC} is the efficiency of the PFC stage.

The low-frequency ripple current of the PFC capacitor can be obtained by

$$I_{\text{C\_LF}} = \frac{I_o}{2}. \tag{8}$$

For the PFC section, a 600-V 99-mΩ MOSFET was selected for each channel of the interleaved boost converter. A 600-V, 6-A silicon carbide diode was selected for the boost diodes. Iron-powder toroidal cores were used to obtain inductance values of 400 μH for each of the boost inductors. A standard two-phase interleaved CCM PFC controller from Texas Instruments, i.e., UCC28070, was used to implement the control for the PFC front end.

The full-bridge dc–dc converter was designed to operate at a PFC bus voltage, with V_{PFC} of 400 V and an output voltage V_o of 400 V at full load. Initially, a peak-to-peak output ripple current ΔI_o of 1 A was assumed. Including dead time and duty cycle loss, an effective duty cycle of 0.75 was assumed. Following these assumptions, the transformer turn ratio is determined to be 0.75 using the following [24]:

$$n_t = \frac{D_{\text{eff}} \times V_{\text{in}}}{V_o} = 0.75. \tag{9}$$

A custom planar-type ferrite transformer was designed using a turn ratio of $12(N_p) : 16(N_s)$.

An output filter inductor value of 400 μH was selected using (10)

$$L_o = \frac{\left(\frac{V_{\text{in}}}{n_t} - V_o\right) \times D_{\text{eff}}}{\Delta I_d \times 2f_s} \tag{10}$$

$$L_R = \frac{n_t \times V_{\text{in}}(1 - D_{\text{eff}})}{4\Delta I_d \times f_s} \approx 8\ \mu\text{H}. \tag{11}$$

A 6-μH resonant inductor was selected, which is smaller, as compared with the value calculated using (11). A toroidal (iron-powder core) inductor was used to obtain 4 μH, and an additional 2 μH was obtained using the transformer leakage inductance. Using a 6-μH inductor, ZVS can be achieved for Q1 and Q2 from load current of $I_o = 11$ A down to 5.5 A. Below 5.5 A, Q1 and Q2 will have turn on switching losses, but the total losses at 5.5 A are 16 W, which are considerably lower than the 20 W of the total loss with ZVS at 11-A load. The heat sink around the primary MOSFETs is designed to extract 20 W from each primary device, which is sufficient to handle the light load losses when the MOSFETs lose ZVS. Furthermore, the battery charger normally operates to provide an output current between 5.5 and 11 A to charge a discharged battery; thus, reduced efficiency below 5.5 A is not a significant concern. Finally, a lower resonant inductor value reduces the duty cycle loss and helps achieve higher full-load efficiency by minimizing the circulating current conduction loss.

A 600-V, 80-mΩ MOSFET with a fast body diode was selected for the four dc-dc stage primary switches. A 12-A silicon carbide diode was selected for the four output rectifier diodes. A 33-μF/500 V electrolytic capacitor was selected for output filter capacitance.

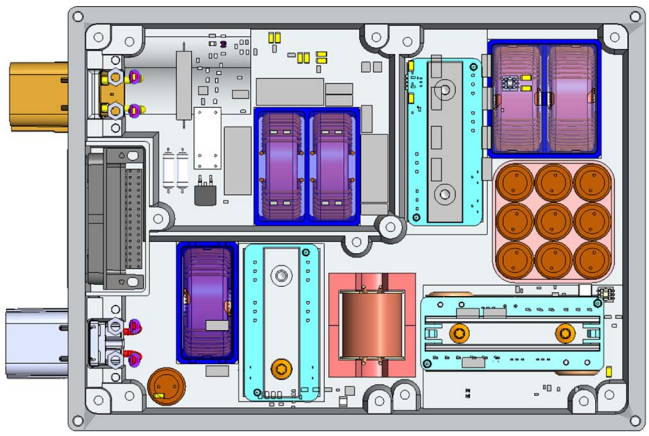

Fig. 7. Internal component organization of the charger.

TABLE II
KEY COMPONENTS USED FOR THE BATTERY CHARGER

Device	Part # / Value	# of devices
PFC Slow Diode	20ETS08S	4
PFC Fast Diode	IDH06S60C	2
PFC MOSFET	IPP60R099CP	2
PFC Inductor	77438 core / 400 µH	2
PFC Capacitor	EKXJ451ELL101 / 100 µF	9
SMD CT 1:100	B78302A7760A003	2
PFC Controller	UCC28070	1
PFC Driver	MIC4124	1
DC/DC MOSFET	SPW47N60CFD	4
DC/DC Diode	IDH12S60C	4
Transformer	ERP 12x34x49	1
Filter Inductor	77438 core / 400 µH	1
Filter Capacitor	ECST501ELL330MLN / 33 µF	1
DC/DC Controller	ISL6753	1
DC/DC Driver	IR2110	2

IV. EXPERIMENTAL RESULTS

The key powertrain and control circuit component information is summarized in Table II. The internal component organization of the battery charger is provided in Fig. 7. The ac input power is fed through the top left connector, which then feeds the inrush current protection circuit followed by the EMI filter. The inrush protection and EMI filter circuit is placed in a shield to meet stringent FCC Class B conducted and radiated emission requirements.

The interleaved PFC circuit consists of the PFC block where the ac rectifier diodes, boost converter MOSFETs, and diodes are mounted. There are two boost inductors and nine 100-μF 450-V PFC bus capacitors. The 400-V dc PFC output is fed to the HV primary block on which the full-bridge MOSFETs and resonant inductor are mounted. The HV transformer is placed in between the primary and secondary blocks. The output rectifier diodes and the clamp resistor R_C are mounted on the secondary block. The output filter inductor and capacitor are also shown. Finally, the HV dc output power is delivered through the bottom left connector. All of the power components and blocks are connected to the base plate of the chassis for cooling through the liquid channels. A photo of the mechanical packaging is provided in Fig. 8.

Fig. 8. Mechanical packaging of the charger.

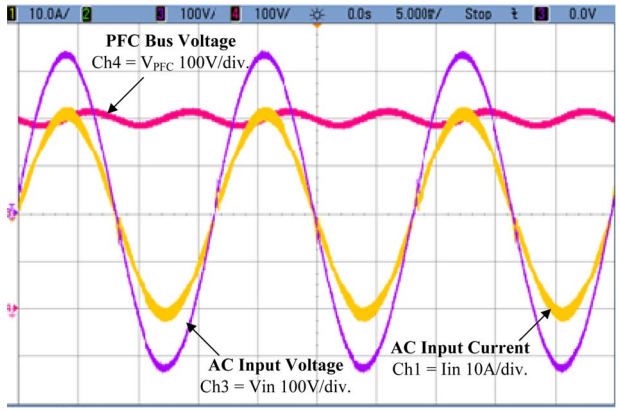

Fig. 9. Experimental waveforms of the input current, input voltage, and PFC bus voltage of the interleaved PFC boost converter at $V_{\rm in} = 240$ V and full load. Ch1 $= I_{\rm in}$ 10 A/div. Ch3 $= V_{\rm in}$ 100 V/div. Ch4 $= V_{\rm PFC}$ 100 V/div.

Waveforms of the input voltage, input current, and PFC bus voltage of the charger are provided in Fig. 9 for the following test conditions: $V_{\rm in} = 240$ V, $I_{\rm in} = 15$ A, $P_o = 3300$ W, $V_o = 300$ V, $f_{\rm sw} = 70$ kHz (PFC), and 200 kHz (dc–dc). The input current is in phase with the input voltage, and its shape is nearly perfectly sinusoidal, as expected.

The ac input current and the inductor current in phases 1 and 2 are shown in Fig. 10. The input current ripple frequency is two times the inductor current ripple, and the input current ripple is half the amplitude of the inductor current ripple.

The HV output voltage and current are provided in Fig. 11 for $V_o = 400$ V and $I_o = 8$ A. The HV output has nearly zero low-frequency ripple. This is an important characteristic in battery charging applications.

The power factor is another useful parameter to show the quality of the input current. The charger input ac power factor is provided in Fig. 12 for the entire load range at 120- and 240-V inputs. The power factor is greater than 0.99 from half load to full load.

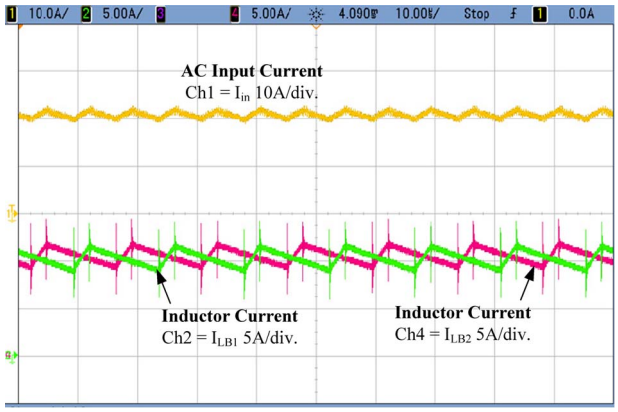

Fig. 10. Experimental waveforms of the input current, both inductors current in the interleaved boost converter at Vin = 240 V, and full load. Ch1 = $I_{\rm in}$ 10 A/div. Ch2 = $I_{\rm LB1}$ 5 A/div. Ch4 = $I_{\rm LB2}$ 5 A/div.

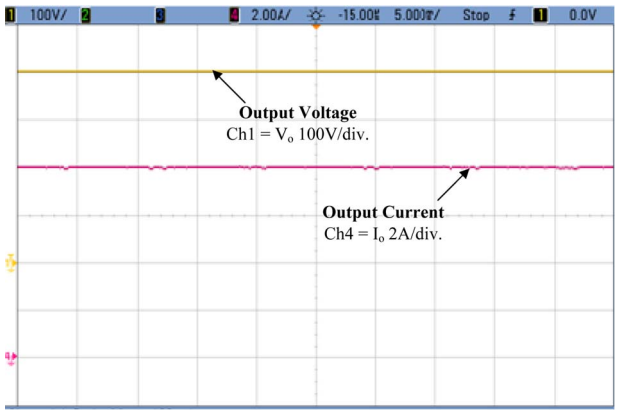

Fig. 11. Experimental waveforms of the HV output voltage and current. Ch1 = V_o 100 V/div. Ch4 = I_o 2 A/div.

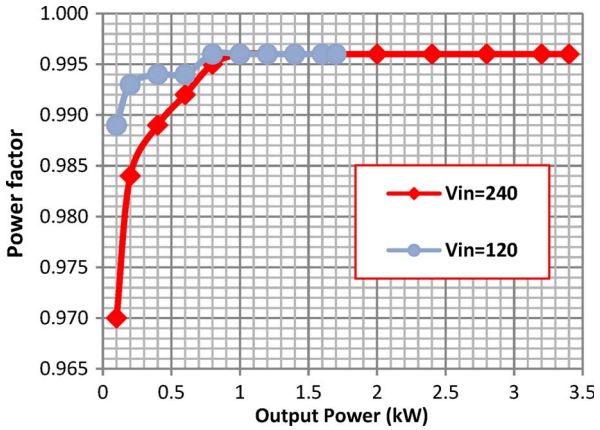

Fig. 12. Measured PF as a function of output power at 240- and 120-V inputs.

Curves of the ac input current total harmonic distortion (THD) are provided in Fig. 13 for full load at 120- and 240-V inputs. It is noted that the input current THD is less than 5% from half load to full load.

To verify the quality of the input current in the proposed topology, its harmonics up to the 39th harmonic are given and compared with the IEC 1000-3-2 standard in Fig. 14 for 120- and 230-V inputs. All converter harmonics are well below the IEC standard, which is required for PHEV chargers.

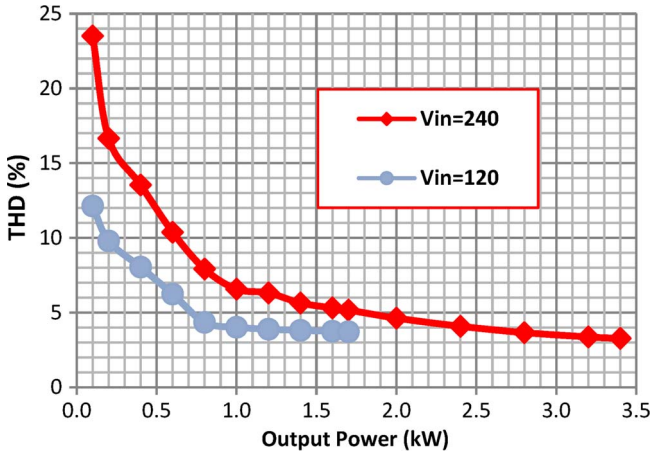

Fig. 13. Experimental measured THD as a function of output power at 240- and 120-V inputs.

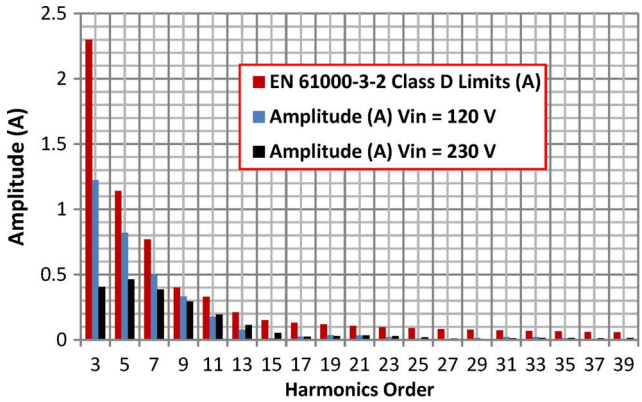

Fig. 14. Experimental measured individual harmonics as a function of the harmonic number for 120-V and 1700-W condition and 230-V and 3300-W condition.

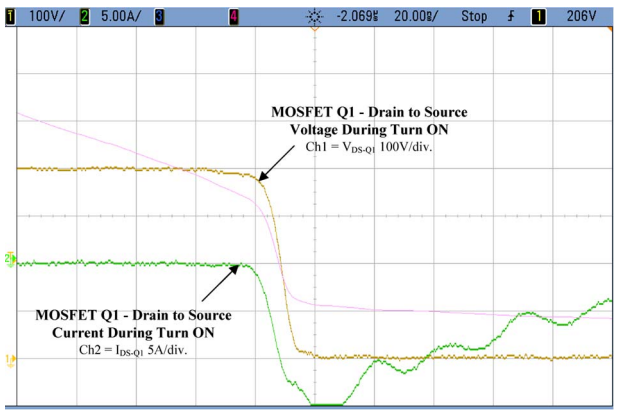

Fig. 15. Experimental waveforms of MOSFET Q1 voltage and current during turn-on at V_o = 300 V and I_o = 11 A. Ch1 = $V_{\rm DS-Q1}$ 100 V/div. Ch2 = $I_{\rm DS-Q1}$ 5 A/div.

Zero-voltage turn-on for MOSFETs Q1 and Q3 is shown in Figs. 15 and 16, respectively, at 300-V output voltage and 3.3-kW load.

Efficiency curves as a function of output power for the PFC stage, the dc–dc stage, and the overall battery charger are provided in Figs. 17–19, respectively.

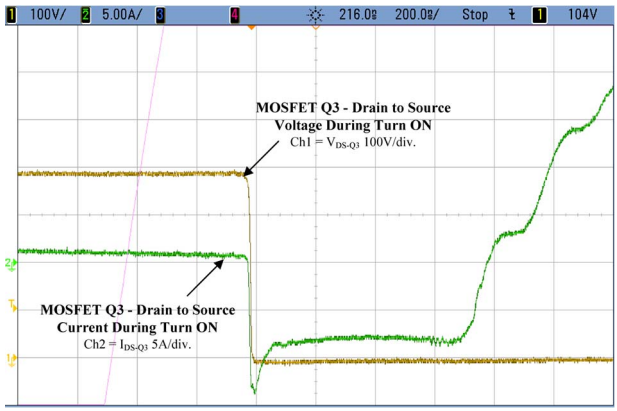

Fig. 16. Experimental waveforms of MOSFET Q3 voltage and current during turn-on at $V_o = 300$ V and $I_o = 11$ A. Ch1 $= V_{\mathrm{DS}-\mathrm{Q3}}$ 100 V/div. Ch2 $= I_{\mathrm{DS}-\mathrm{Q3}}$ 5 A/div.

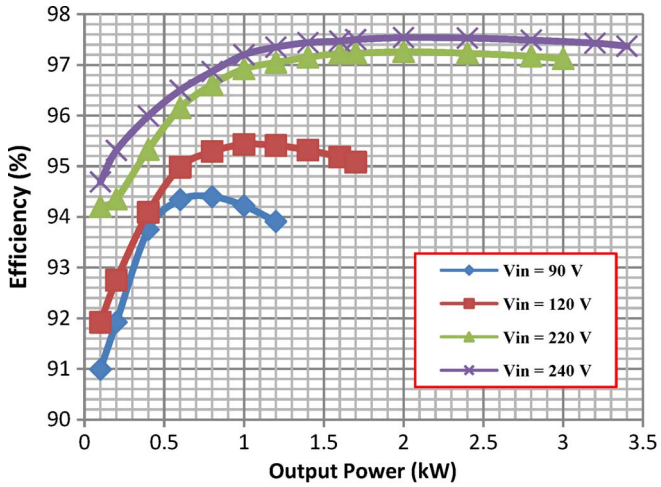

Fig. 17. Experimental measured efficiency for the interleaved PFC boost converter as a function of output power.

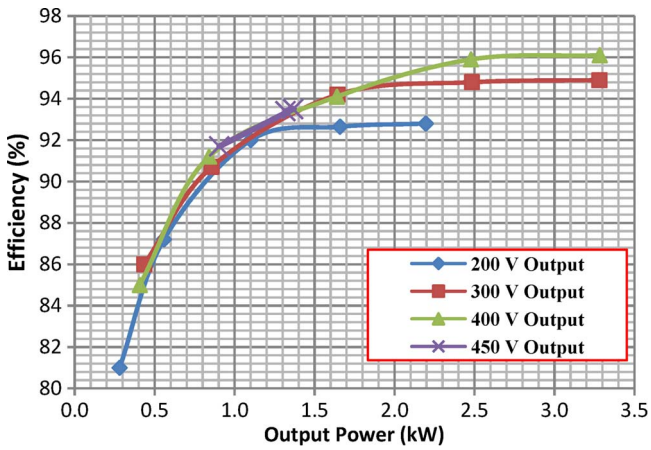

Fig. 18. Experimental measured efficiency for the second-stage dc–dc converter as a function of output power.

With the proposed charging solution, a peak charger efficiency of 93.6% was reached at 240-V input and 3.3-kW output power. High efficiency over the entire load range is achieved with this solution. Furthermore, high efficiency means that more of the limited input power is available to charge the batteries, reducing charging time and electricity costs.

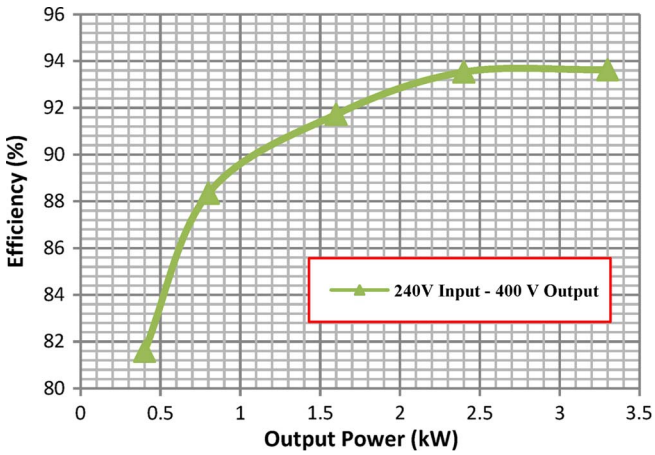

Fig. 19. Experimental measured efficiency of the complete charger as a function of output power at 240-V input and 400-V output voltage.

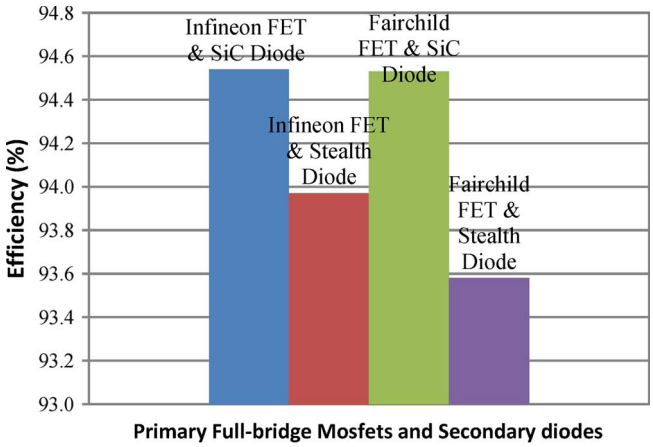

Fig. 20. Measured efficiency comparison with different combination of primary MOSFETs and secondary diodes at $V_o = 300$ V and $I_o = 11$ A.

Fig. 20 shows a measured full-load efficiency comparison for various semiconductor combinations, which were evaluated. Based on this comparison, Infineon's SPW47N60CFD MOSFET and IDH12S60C silicon carbide diode were selected. It is also noted that the use of hyperfast diode (i.e., Fairchild's stealth diode, ISL9R860) is not suitable for this application due to the high reverse recovery losses.

The experimental thermal measurements of the internal components of the charger are provided in Fig. 21 for $V_{\mathrm{in}} = 240$ V, $V_o = 300$ V, and $I_o = 11$ A ($P_o = 3.3$ kW). The hottest spot is the PFC inductor windings at 97 °C. This test was done with the ambient temperature of 105 °C, whereas the base-plate temperature was kept constant at 70 °C.

V. Conclusion

A high-performance two-stage ac–dc battery charger topology has been presented in this paper for PHEV battery charging applications. The detailed operation, design, and performance characteristics of the proposed converter are presented.

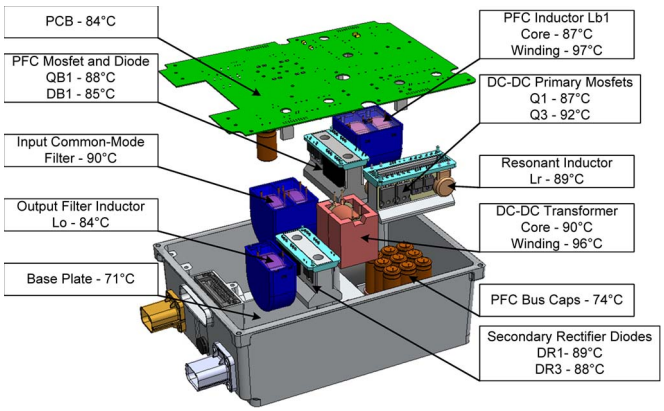

Fig. 21. Experimental thermal measurement results of the charger powertrain components at 240-V input and 300-V output voltage and 3.3-kW output power.

Experimental results presented include waveforms, as well as efficiency and input current harmonic data. The input current harmonics at each harmonic order were compared with the IEC 1000-3-2 standard limits. The input current THD is less than 5% from half-load to full load, and the converter is compliant with the IEC 1000-3-2 standard. The charger power factor was also provided for the full-load power range at 120- and 240-V inputs. The power factor is greater than 0.99 from half-load to full load. The proposed charger achieved a peak efficiency of 93.6% at 70- and 200-kHz switching frequencies for PFC and DC–DC stages, respectively, with 240-V input and 3.3-kW output power. The converter meets all required design specifications. It operates over a wide output voltage range of 200–450 V and is packaged in a compact size of 5.5 L.

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