

16F88 Instruction Set

Mnemonic	Description	Operation	Status bits	
ADDLW k	Add Literal and W	w + k → destination	C, DC, Z	1
ADDWF f, d	Add W and f	w + f → destination	C, DC, Z	1
ANDLW k, d	AND Literal and W	w and k → destination	Z	1
ANDWF f, d	AND W and f	w and f → destination	Z	1
BCF f, b	Bit Clear f	0 → f		1
BSF f, b	Bit Set f	1 → f		1
BTFSC f, b	Bit Test f, Skip if Clear	skip if f = 0 (2 Cycles)		1
BTFSS f, b	Bit Test f, Skip if Set	skip if f = 1 (2 Cycles)		1
CALL k	Call Subroutine	PC → TOS, k → PC[10:0] PCLATH[4:3] → PC[12:11]		2
CLRF f	Clear f	0x00 → f, 1 → Z	Z	1
CLRW	Clear W	0x00 → w, 1 → Z	Z	1
CLRWD	Clear Watchdog Timer	0x00 → WDT, 1 → TO, 1 → PD	TO, PD	1
COMF f, d	Compliment f	f - 0xFF → destination	Z	1
DECf, d	Decrement f	f - 1 → destination	Z	1
DECFSZ f, d	Decrement f and Skip if Zero	f - 1 → destination skip if result = 0 (2 Cycles)		1
GOTO k	Go to address	k → PC[10:0] PCLATH[4:3] → PC[12:11]		2
INCF f, d	Increment f	F + 1 → destination	Z	1
INCFSZ f, d	Increment f and Skip if Zero	F + 1 → destination skip if result = 0 (2 Cycles)		1
IORLW k, d	Inclusive OR Literal with W	w or k → destination	Z	1
IORWF f, d	Inclusive OR w with f	w or f → destination	Z	1
MOVf, d	Move f	f → destination	Z	1
MOVLW k	Move literal to W	k → w		1
MOVWF f	Move W to f	w → f		1
NOP	No Operation	No Operation		1
RETFIE	Return from interrupt	TOS → PC, 1 → GIE		2
RETLW k	Return with Literal in W	k → w, TOS → PC		2
RETURN	Return from Subroutine	TOS → PC		2
RLF f, d	Rotate Left f through Carry	C << f << C → destination	C	1
RRF f, d	Rotate Right f through Carry	C >> f >> C → destination	C	1
SLEEP	Enter Standby Mode	0x00 → WDT, stop oscillator	TO, PD	1
SUBLW k	Subtract W from Literal	k - w → destination	C, DC, Z	1
SUBWF f, d	Subtract W from f	f - w → destination	C, DC, Z	1
SWAPF f, d	Swap nibbles in f	f[3:0] → destination [7:4] f[7:4] → destination [3:0]		1
XORLW k, d	Exclusive OR Literal with W	w xor k → destination	Z	1
XORWF f, d	Exclusive OR W with f	w xor f → destination	Z	1

k = 8 bit Literal or 11 bit Address, f = File Register, d = Destination (w or f) if omitted will default to f
 skip instructions add an extra cycle if condition is true (BTFSC, BTFSS, DECFZ, INCFSZ)

MPASM Pseudo Instruction Set (mini macros for the midrange PIC)

Mnemonic	Description	Operation	Status bits	
ADDCF f, d	Add Carry to File Register	btfsc STATUS, C incf f, d	Z	2
ADDDCF f, d	Add Digit Carry to File Register	btfsc STATUS, DC incf f, d	Z	2
BC k	Branch on Carry	btfss STATUS, C goto k		2
BNC k	Branch on Not Carry	btfsc STATUS, C goto k		2
BDC k	Branch on Digit Carry	btfss STATUS, DC goto k		2
BNDC k	Branch on Not Digit Carry	Btfsc STATUS, DC goto k		2
BZ k	Branch on Zero	btfss STATUS, Z goto k		2
BNZ k	Branch on Not Zero	btfsc STATUS, Z goto k		2
CLRC	Clear Carry	bcf STATUS, C	C	1
CLRDC	Clear Digit Carry	bcf STATUS, DC	DC	1
CLRZ	Clear Zero	bcf STATUS, Z	Z	1
LCALL k	Long Call	bcf/bsf STATUS, RP0 bcf/bsf STATUS, RP1 call k		3
LGOTO k	Long Goto	bcf/bsf STATUS, RP0 bcf/bsf STATUS, RP1 goto k		3
MOVFW f	Move File Register to W	movf, 0	Z	1
NEGF f, d	Negate File Register	comf f, 1 incf f, d	Z	2
SETC	Set Carry	bsf STATUS, C	C	1
SETDC	Set Digit Carry	bsf STATUS, DC	DC	1
SETZ	Set Zero	bsf STATUS, Z	Z	1
SKPC	Skip on Carry	btfss STATUS, C <i>(2 Cycles)</i>		1
SKPNC	Skip on Not Carry	btfsc STATUS, C <i>(2 Cycles)</i>		1
SKPDC	Skip on Digit Carry	btfss STATUS, DC <i>(2 Cycles)</i>		1
SKPNDC	Skip on Not Digit Carry	btfsc STATUS, DC <i>(2 Cycles)</i>		1
SKPZ	Skip on Zero	btfss STATUS, Z <i>(2 Cycles)</i>		1
SKPNZ	Skip on Not Zero	btfsc STATUS, Z <i>(2 Cycles)</i>	Z	1
SUBCF f, d	Subtract Carry from File Register	btfsc STATUS, C decf f, d	Z	2
SUBDCF f, d	Subtract Digit Carry from File Register	btfsc STATUS, DC decf f, d	Z	2
TSTF	Test File Register for Zero	movf f, 1	Z	1