Step-up/step-down converter takes 2 to 16V inputs

LUCIANO BORDOGNA AND LUCA VASALLI, MAXIM INTEGRATED PRODUCTS, MILAN, ITALY

The circuit in **Figure 1** is a low-cost step-up/step-down dc/dc converter. By definition, its input can range above and below the regulated voltage. The circuit includes a simple switch-mode boost converter (IC_1) that contains a comparator normally used to detect low battery voltage. In this case, the comparator controls an external pnp transistor that operates as a linear regulator. IC_1 steps up V_{IN} (2V minimum) to the level of V_X, as determined by the jumper block, J_1.

A 2-3 jumper selects the internal divider, producing V_X=12V. A 2-1 jumper selects feedback resistors R_1 and R_2, producing $V_X = 1.5V(R_1+R_2)/R_2$. You should set V_X to 1 to 2V above the desired output voltage. The Q_1 linear regulator steps V_X down to an output level determined by R_3 and R_4: $V_{OUT}= 1.5V(R_3+R_4)/R_4$, where $V_X>V_{OUT}$. When $V_{IN}>V_X$, the switching regulator turns off, and the linear regulator alone controls V_{OUT}. C_6 reduces output ripple. The circuit accommodates a wide range of input and output voltages and supplies output currents as high as 500 mA (**Figure 2**). (DI #2218) EDN

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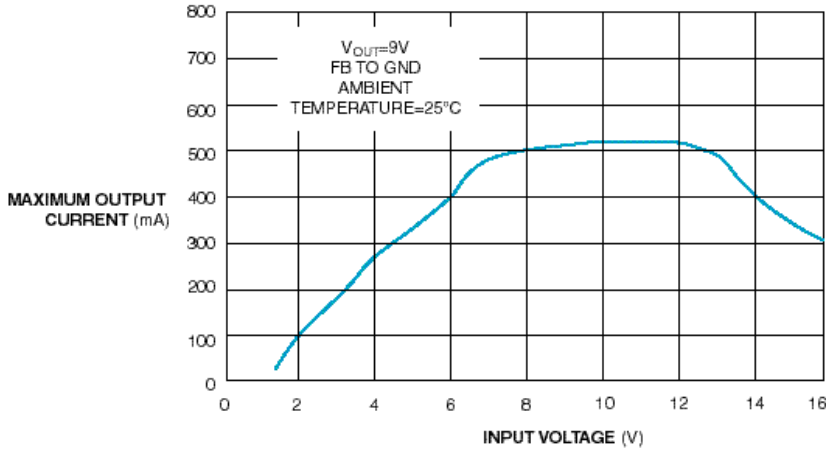
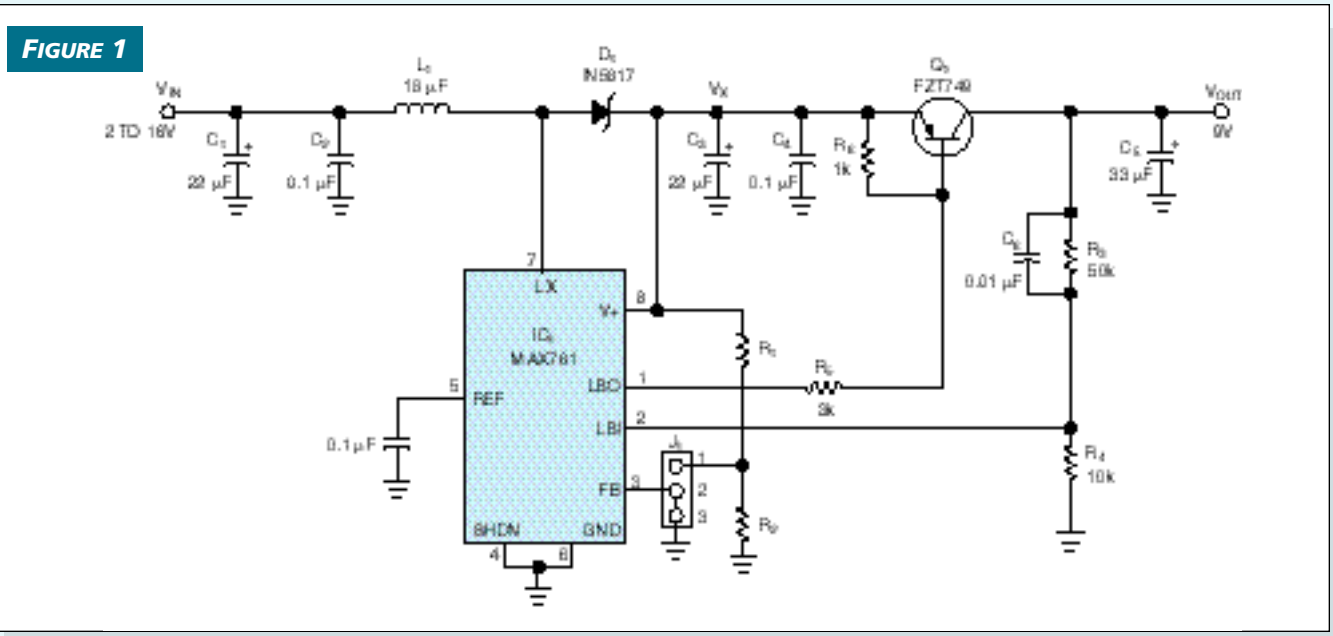
FIGURE 2



Delivering more than 100 mA over its 2 to 16V useful input-voltage range, the regulator in Figure 1 provides 500 mA over an 8 to 13V range.

FIGURE 1



Toggling between switching and linear operation, this regulator operates with input voltages above and below the desired output voltage.

Battery booster delivers 75W

DONALD V COMISKEY, POWER TRENDS INC, WARRENVILLE, IL

The circuit in **Figure 1** defies no laws of physics; it just makes creative use of an isolated dc/dc converter. The application uses the isolated converter in a nonisolated configuration to boost a 48V battery voltage to 60V. The PT3102 is a 15W isolated dc/dc converter that normally uses a 36 to 75V (48V-nominal) input voltage to provide a floating, or isolated, 12V output capable of 1.25A. The trick is to connect the negative-output lead and positive-input lead of the converter, thereby effectively stacking the 12V output on top of the 48V input. (Be aware that the original isolation and safety properties of the converter no longer exist in this configuration.)

A load connected across the converter's positive-output and negative-input leads now sees a total output voltage of 60V. As **Figure 1** indicates, the load-current path is through the battery and the output section of the dc/dc converter. Assuming that the battery is capable of the same 1.25A as the converter, the total power available to the load is 60V31.25A, or 75W.

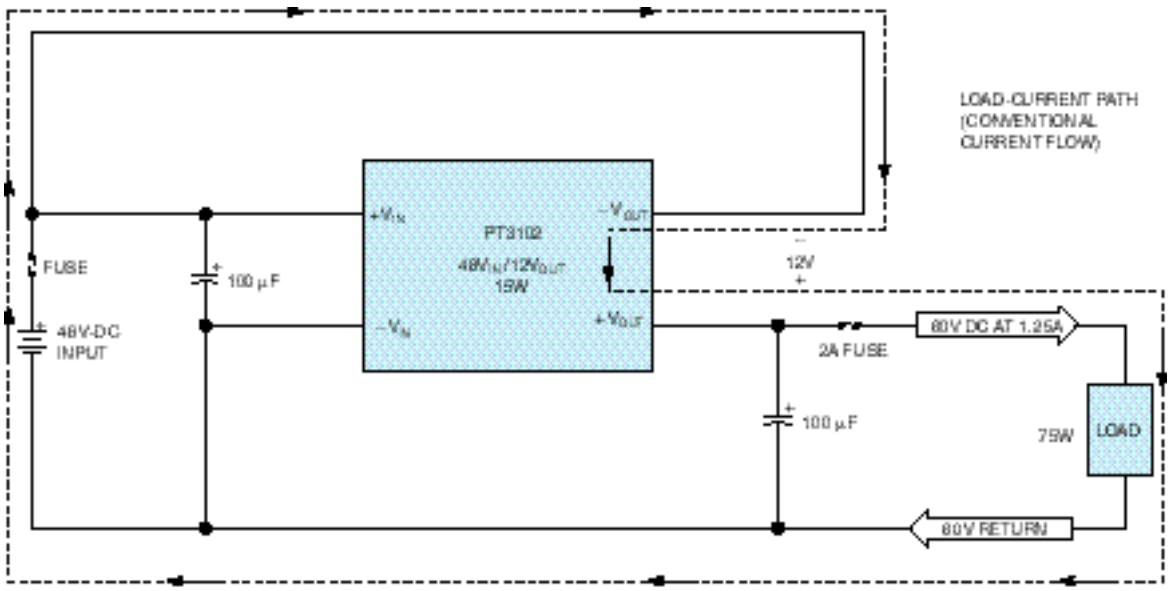
The dc/dc converter regulates its 12V output to within ±2%. The magnitude of the overall output voltage, however, depends on both the 12V output and the battery voltage. If the battery voltage droops to 40V, for example, the overall output voltage is 40+12=52V. If you replace the battery with a 48V power supply with ±5% regulation, the overall output voltage is 60V ±7%.

The dc/dc converter is 80% efficient, meaning it dissipates 3.75W while delivering its rated 15W (12V31.25A). When comparing this 3.75W of power dissipation with the load power of 75W, the overall efficiency is 95%.

The scheme isn't limited to 48V applications. Another application, for example, may need to boost a 24V battery to 36V. You can simply replace the PT3102 with the related PT3105 converter, which operates from 18 to 40V and provides an output voltage of 12V at 1.25A. This 12V output stacked on top of the 24V input provides 36V to the load and results in an efficiency of 3.75W/(36V31.25A)=92%.

In this stacking configuration, use of either converter's on/off control is not recommended, because activating this control succeeds only in disabling the 12V portion of the total output voltage. Even with a disabled converter, a path still exists through the output section of the converter, which comprises a forward-biased diode, causing the input voltage minus the diode drop to appear across the load. For similar reasons, you can't rely on the converter's built-in current

FIGURE 1



The negative-output lead and positive-input lead of the PT3102 dc/dc converter connect to effectively "stack" the converter's 12V output on top of the 48V input, providing 60V total across a 75W load.

limit for overload protection. Instead, use a 2A fuse in series with the output of the converter to protect against excessive load currents.

Because medium- and high-power boost converters are not commonly available off the shelf, custom or build-your-own designs are often necessary. This idea uses a common off-the-shelf converter, normally intended for step-down applications, to accomplish the boost function. Higher power applications, of course, require appropriately sized converters. If regulation of the overall output voltage is necessary, you can consider using an adjustable converter. (DI #2223) EDN

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KURK MATHEWS, LINEAR TECHNOLOGY CORP, MILPITAS, CA

It is often desirable to synchronize a switching power supply to a system clock or to a second supply. If the power-supply controller has no synchronization pin, you can add a low-value resistor in series with the oscillator capacitor, thereby developing a synchronization pulse to sum into the oscillator ramp. Depending on the controller, this method may have drawbacks. Primarily, the wider the synchronization range, the higher the sync-pulse amplitude required (without exceeding the controller's internal reference voltage). Further problems arise if the controller IC uses the oscillator ramp for voltage-mode control, slope compensation, or timing. Under these circumstances, modifying the amplitude of the oscillator ramp may not be an option. Such is the case with IC_1 in **Figure 1**, an LT1509 PWM and power-factor controller, which depends on ramp amplitude for determining the phase relationship between the power-factor and PWM sections and for determining duty cycles.

The circuit in **Figure 1** uses a PLL to adjust the oscillator-ramp charge current, providing a wide synchronization range without changing oscillator voltage levels. Q_1 to Q_3 form a comparator that supplies a square wave (at the oscillator frequency) to IC_2. IC_2's phase comparator II output adjusts the oscillator-ramp charge current until the oscillator frequency equals the input frequency. The method provides synchronization and preserves the oscillator waveform and the IC's function. With the values shown, the frequency-lock range is 90 to 150 kHz. The circuit requires less than 1 mA from a 12V supply. (DI #2233) EDN

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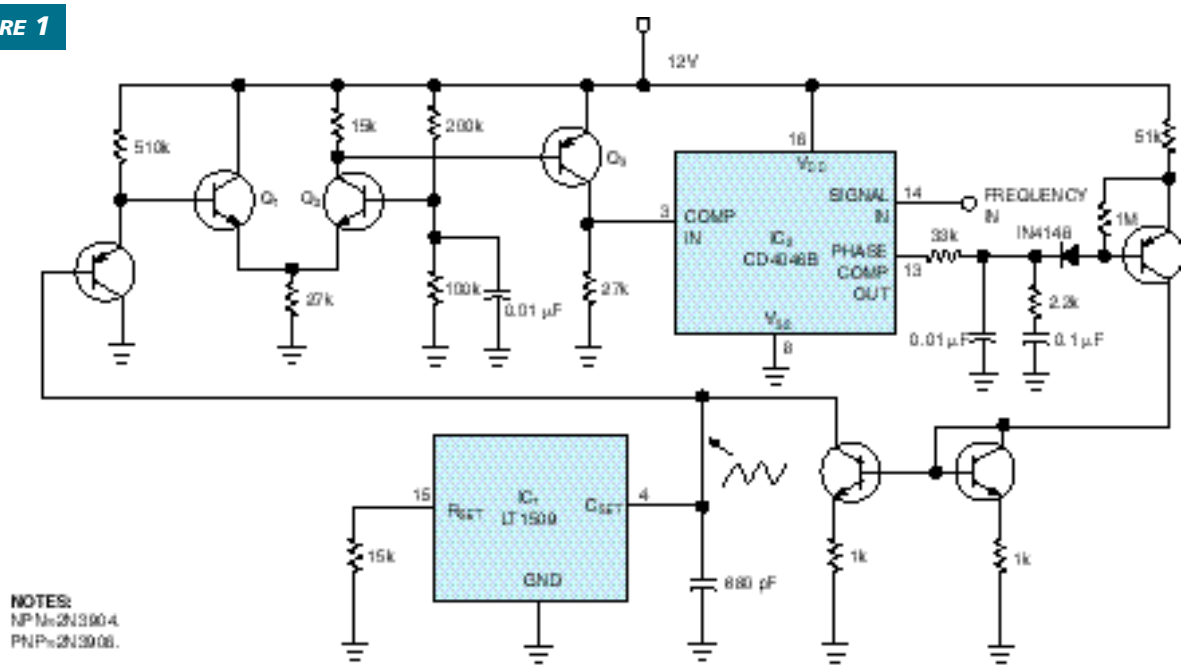
FIGURE 1



A PLL provides frequency synchronization for a PWM and power-factor-controller IC.

Simple Spice model simulates laser diode

LUKASZ SLIWCZYNSKI, UNIVERSITY OF MINING AND METALLURGY, KRAKOW, POLAND

When you design drive circuitry for laser diodes, you must consider safety measures. Laser diodes are delicate devices, and excessive reverse voltage or forward current can easily destroy them. Usually, a laser-diode driver circuit comprises the laser diode and a monitor photodetector in a common package and a low-frequency feedback loop that stabilizes the diode's optical output power. Computer simulation of the driver before you turn it on can be helpful in thwarting laser-diode mortality.

Improperly designed driver circuitry can provoke laser-diode failure in two ways: large transients during the turn-on or -off phase and circuit instability. The first failure mechanism is unamenable to computer simulation, because it would require a reliable model of the power supply's switching behavior. However, even a laser diode with well-defined turn-on and -off transients may be in peril if its frequency characteristic shows high peaks or a tendency to oscillate. It's relatively easy to check oscillation with computer simulation using a Spice model. The model uses the simplified equations describing the relationship between the laser diode's current, the monitor's current, and the optical output power:

$$P_{LAS} = \begin{cases} 0 & \text{IF } I_{LAS} < I_{TH} \text{ AND } I_{MON} = S_{MON} P_{LAS} \\ \varepsilon (I_{LAS} - I_{TH}) & \text{IF } I_{LAS} \geq I_{TH} \end{cases},$$

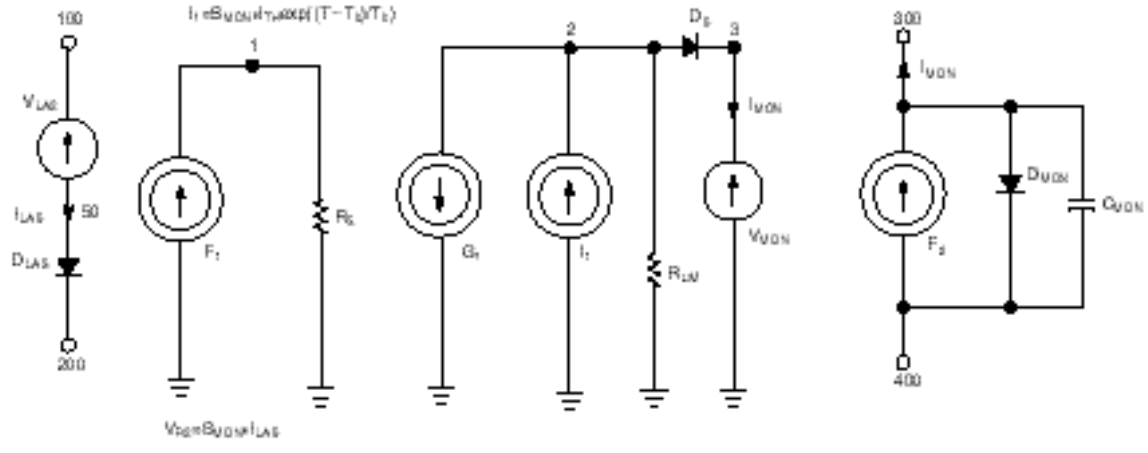
where
P_{LAS}=laser-diode output optical power,
I_{LAS}=forward laser-diode current,
I_{TH}=laser-diode threshold current,
I_{MON}=monitor-photodetector current (proportional to laser-diode power),

$$\varepsilon = \frac{dP_{LAS}}{dI_{LAS}}\Big|_{I_{LAS} \geq I_{TH}} = \text{LASER-DIODE SLOPE EFFICIENCY, AND}$$

$$S_{MON} = \frac{P_{LAS}}{I_{MON}} = \text{MONITOR-EFFICIENCY COEFFICIENT.}$$

Figure 1 shows the simple Spice model of the laser diode with its associated monitor photodetector. **Listing 1** gives the Spice netlist. The laser-diode pin assignments are 100 (anode) and 200 (cathode); the monitor assignments are 300 (anode) and 400 (cathode). Because the laser diode's junction operates forward-biased under normal conditions, the Spice model represents it as voltage source V_{LAS} in series with diode D_{LAS}. You should choose the value of V_{LAS} to match the emitted wavelength (approximately 1V for 820 nm and approximately 0.8V for 1300 nm). Current source I_1 models the laser diode's threshold-current-temperature dependence. R_{LIM} limits the voltage at Node 2 when $I_{LAS}<I_{TH}$. Diode D_S starts to conduct when the laser-diode current rises above the threshold

FIGURE 1



A simple Spice model can prevent destruction of laser diodes by providing a forewarning of dynamic instability.

value. Under normal operating conditions, the monitor photodetector is reverse-biased; for the purpose of ac analysis, the Spice routine models the photodetector as capacitance C_{MON}. This component is the only one affecting the dynamic behavior in this model, because the laser diode itself is much faster than any component in the driver circuit (1- to 3-GHz or higher cutoff frequency). You can download **Listing 1** from *EDN*'s Web site, www.ednmag.com. At the registered-user area, go into the Software Center to download the file from DI-SIG, #2227. (DI #2227) EDN

LISTING 1—SPICE NETLIST FOR LASER/MONITOR DIODE PAIR

```
Vlas        100 50 1
Dlas        50 200 diode1

F1          0 1 Vlas 1
Rs          1 0 {Sm*eps}

I1          2 0 {Sm*eps*Ith*exp((T/25)-1)}
G1          0 2 1 0 1
Rlim        2 0 1Meg
Ds          2 3 diode
Vm          3 0 0

F2          300 400 Vm 1
Dmon        300 400 diode
Cmon        300 400 Cmon

.model      diode    d
.model      diode    d rs=5

.ENDS
```

References

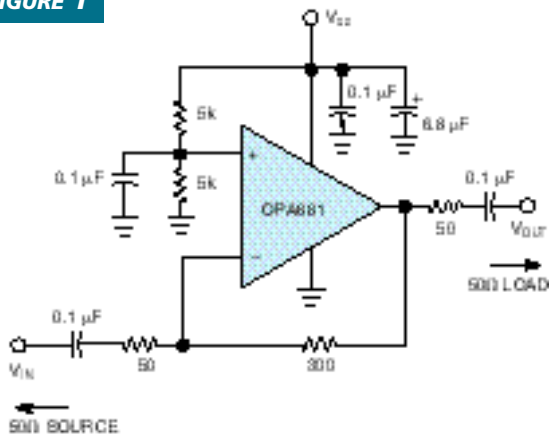
1. *Fiber Optics Handbook*, Hewlett-Packard, 1989.
2. Kressel, H, *Semiconductor Devices for Optical Communication*, Springer-Verlag, 1980.

To Vote For This Design, Circle No. 421

MICHAEL STEFFES, BURR-BROWN CORP, TUCSON, AZ

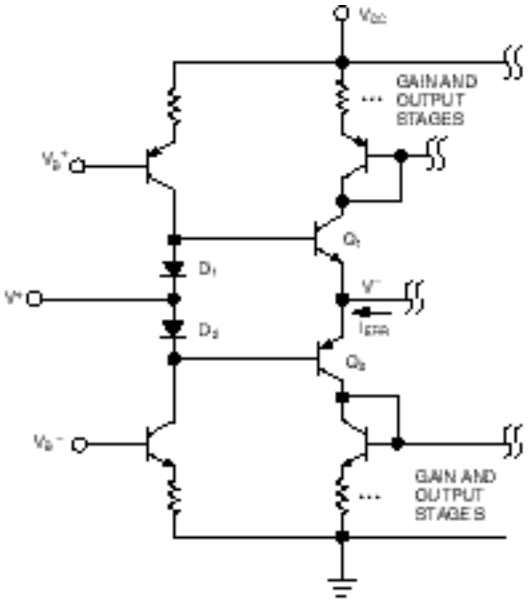
Most of the recent wideband, single-supply op amps use a voltage-feedback design. The error signal (differential input voltage) for a voltage-feedback op amp can operate over a range of common-mode input voltages, and its common-emitter output stage can provide output voltages near the supply rails. Current-feedback op amps are becoming available with wide output swings, but they still typically require at least 1.5V input head room for proper operation of the input stage's voltage buffer and inverting-node error-current

FIGURE 1



This current-feedback amplifier retains high bandwidth and a wide input-voltage swing, even with its input-stage transistors saturated.

FIGURE 2

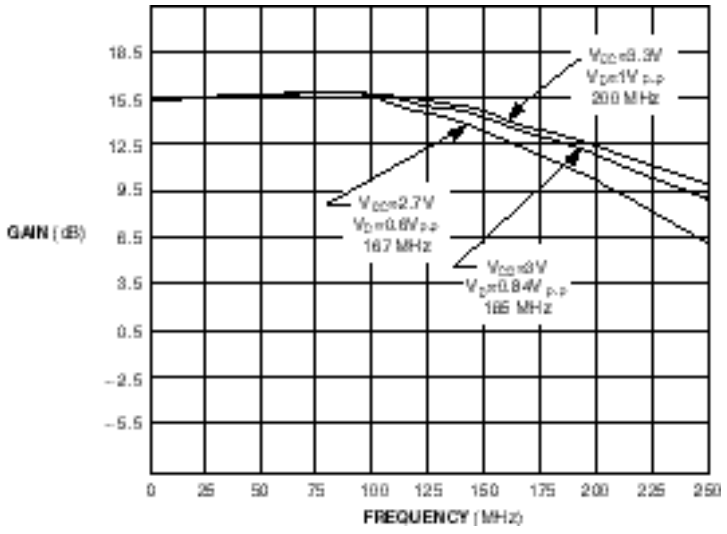


Saturation reduces the gain of Q_1 and Q_2, but the transistors still retain enough gain to provide adequate bandwidth in the amplifier.

sensing in the noninverting configuration. A current-feedback op amp offers the main advantage of wideband operation at higher gains. A subtler and previously overlooked advantage is the fact that you can operate most devices with a total supply voltage lower than the rated total input-stage head-room requirement. **Figure 1** shows a wideband, current-feedback op amp operating with a saturated input stage.

The OPA681 current-feedback op amp has a bandwidth greater than 200 MHz and a high-power output that can swing to within 1V of the supply rails. The input, however, requires 1.5V head room for proper operation. This requirement implies that, with a 3V power supply, the input stage is off while the output should still offer a 1V p-p swing. The circuit in **Figure 1** establishes a bias voltage on the noninverting input, set to the supply midpoint. The inverting signal path has an ac-coupled gain of 6. For test purposes, set the signal-input resistor to match the 50V source; the output drives a 50V matching resistor, through a dc-blocking capacitor, to a 50V load.

FIGURE 3



By ignoring the input-range specs of a current-feedback op amp, you can obtain extended wideband operation with low supply voltages.

In actual applications, you may not require this input match, and the output load may not need to be a doubly terminated line. However, the frequency response strongly depends on the selected value for the feedback resistor. Increasing it bandlimits the design; reducing it peaks the response. This circuit provides more than 150-MHz bandwidth, even for supplies lower than 3V, which would appear to violate the input-range spec. To understand this unique feature of a current-feedback topology, consider a simplified input-stage architecture in **Figure 2** .

If the noninverting input connects to $V_{CC}/2$ (**Figure 1**) and you steadily reduce the supply voltage, the first junctions to saturate are in Q_1 and Q_2. These two transistors provide the essence of the current-feedback operation. In normal operation, they provide voltage buffering for the input voltage (signal) at the noninverting input while acting as common-base stages to cascode the error-current signal into the inverting node through to the current-mirror gain stages. Consider what happens as these transistors saturate. The voltage-buffer aspect of the circuit still operates in a dc sense with a considerable drop-off in bandwidth if the signal were injected into the noninverting input. The error current still effectively cascodes through these transistors with a decreased a (the collector-emitter current gain in common-base configuration).

Under normal operation, a is nearly 1. As Q_1 and Q_2 saturate, a decreases, effectively reducing the dc open-loop gain for the forward signal path internal to the current-feedback amplifier. Because this open-loop gain is already high, an a even as low as 0.5 reduces the dc open-loop gain by only 6 dB with little effect on the open-loop frequency response. Q_1 and Q_2 can operate well into saturation, with little input on frequency response. This effect is a unique aspect of a current-feedback design, because similar operation for the differential input stage of a voltage-feedback op amp is impossible with the input-stage transistors saturated. You can use this feature to extend the range of low-voltage operation for current-feedback op amps that offer higher output swing than input range.

Figure 3 shows the results of tests with 3.3, 3, and 2.7V supplies. In each case, the output-voltage swing increased to just below the onset of gain compression. You can determine the required output-voltage head room for each supply voltage by subtracting the peak-to-peak output from V_{CC} and then dividing by two. You obtain slightly more output-voltage swing with light loads, such as an ADC input. With a 2.7V supply, the inverting-input transistors, Q_1 and Q_2 in **Figure 2**, are well-saturated, yet the amplifier still provides more than 150-MHz bandwidth with an inverting gain of 6V/V (15.5 dB from input to output), with a 0.6V p-p output swing. Small-signal operation maintains more than 100-MHz bandwidth with a supply as low as 2.2V. This bandwidth would have required an equivalent single-supply, voltage-feedback op amp with approximately 600-MHz gain-bandwidth product and a greater-than-300V/msec slew rate. (DI #2232) EDN

To Vote For This Design, Circle No. 422

CRAIG VARGA, LINEAR TECHNOLOGY CORP, MILPITAS, CA

To power a load that requires a high-compliance current source (for example, a plasma tube, such as an ion laser), a circuit must provide very accurate current control with a wide bandwidth and a voltage compliance of several hundred volts. You can use a high-speed linear-regulator controller to perform just such a function **Figure 1** . The bandwidth of this circuit measures more than 1 MHz. Because no part of the control circuit connects to the input supply, only the selected MOSFET and the ratings of the input supply's bypass capacitors limit the voltage compliance.

The typical application of the LT1575 linear regulator (IC_1) is to drive a MOSFET as an overdriven source follower, providing a high-speed and accurately regulated output voltage. The internal error amplifier and output buffer drive the large capacitive loads presented by MOSFET gates with an open-loop bandwidth of more than 15 MHz. You can implement a current source by replacing the output-voltage feedback divider with a current-sense resistor. The internal reference is nominally 1.21V with an accuracy of ±0.6%. Thus, you can program very accurate currents. IC_1 continuously adjusts the FET's gate voltage to maintain a constant load current, regardless of the voltage across Q_1. The input capacitors' voltage rating limits the circuit to 100V. The FET has a rating of 250V. Only the voltage ratings of the FET and input capacitor limit the circuit's compliance.

With a current-command voltage of 0V, the load current is approximately 1A. As the current command increases, the load current decreases. At approximately 2.42V, the load current drops to zero. By changing the values of R_1, R_3, and R_5, you can alter the scale factor. R_2, C_1, and C_2 provide loop compensation. R_4 and C_4 compensate for a slight drop in gain between approximately 80 and 200 kHz. These values are likely to depend on layout and may need adjusting in another implementation. When a high-compliance voltage is necessary, C_3 connects from the FET's drain to ground. The FET's drain-to-source capacitance decreases substantially at high stand-off voltages. C_3 swamps the FET capacitance, ensuring stability under all conditions.

Obviously, Q_1 needs a substantial heat sink if high voltage and even moderate currents are simultaneously present. If the power dissipation level becomes unmanageable, you can achieve a manageable level by making as many identical stages parallel as necessary to reduce each stage's current. (DI #2234) EDN

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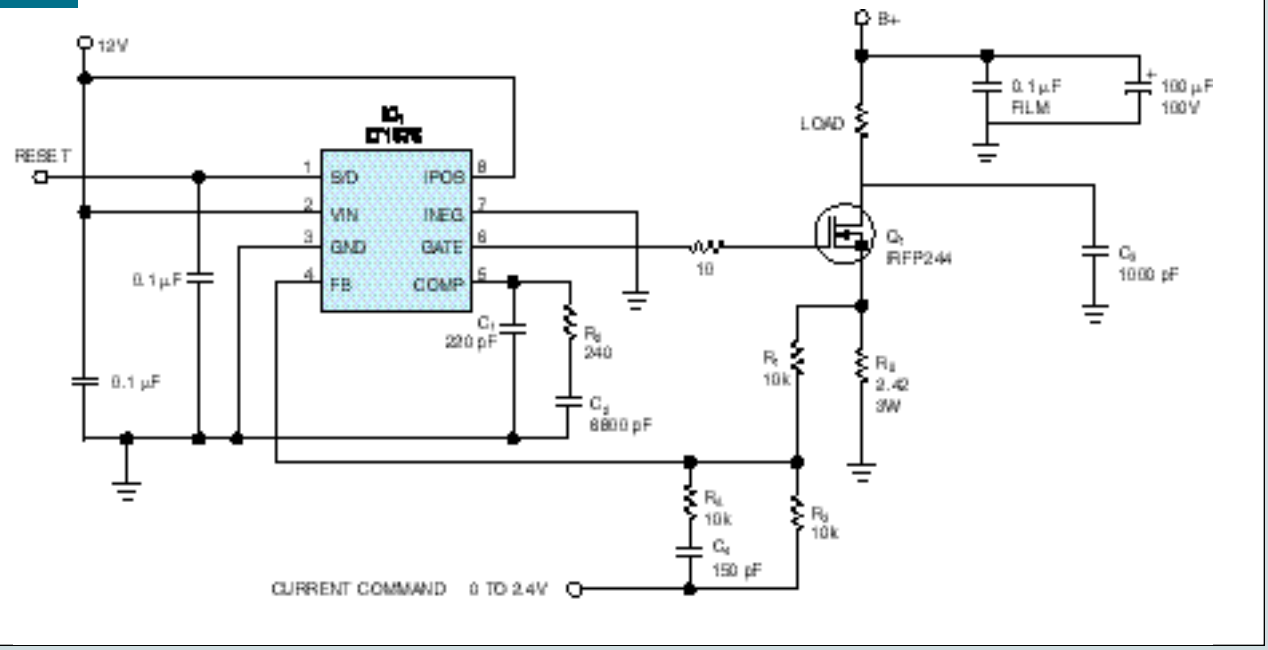
FIGURE 1



A high-speed linear regulator (IC_1) can provide accurate current control with a wide bandwidth and a voltage compliance of as many as several hundred volts.

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