High and Low Light CMOS Imager Employing Wide Dynamic Range Expansion and Low Noise Readout

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***Abstract*— A high and low light imager (HALLI) developed in a CMOS process is presented. The HALLI utilizes a single column parallel partitioned pixel amplifier with variable topology for the detection of both high and low light levels in the same frame. For high light level detection, a wide dynamic range algorithm is utilized in which multiple resets via real-time feedback are employed. Each pixel in the field of view is independent and can automatically set its exposure time according to its illumination. For low light level detection, two noise reduction techniques are employed, active reset and active column sensor readout technique. Due to the commonalities in the high and low light level readout techniques, and the fact that they occur in staggered instances of time, a single partitioned pixel amplifier which can be configured in various modes of operation is used. The advantages of using a single column parallel partitioned pixel amplifier are simplicity in the analog readout path, reduced chip size, and lower power consumption than using individual dedicated blocks for each technique. The CMOS imager was designed and fabricated in a mixed signal 0.18 μm CMOS technology. System architecture, operation and results are presented.**

***Index Terms*— Active column sensor, active reset, CMOS imagers, column parallel architecture, low light level detection, multiple reset, rolling shutter, wide dynamic range.**

I. Introduction

DEVELOPMENT of miniature CMOS image sensors triggers their penetration to various fields of our daily life. CMOS imagers offer significant advantages in terms of low power, low-voltage, flexibility, cost and monolithic integration over rivaling traditional CCDs [1]. These features make them suitable for a variety of applications where both high and low light illuminated scenes are present. Such applications include bio-medical, digital still and video cameras, cellular phones and web / security cameras [2]–[5]. The lower light intensity that a CMOS sensor can successfully image is limited by the signal-to-noise ratio (SNR). Many groups have reported on techniques to reduce imager noise. The common techniques being low dark current photodetectors, low-noise differential circuits, Active Reset (AR), correlated multiple sampling, and multiple digitizations and averaging to reduce read noise [6]–[9]. To the best of our knowledge no one has yet to report on a low-noise imager with wide dynamic range capability for high and low light level detection.

With increased miniaturizing of CMOS imagers by technology scaling, the supply voltage is also lowered which leads to a decrease in the output swing of the sensor and in turn decreasing the dynamic range (DR) [10]. With a narrower DR the image sensor pixels will saturate under lower illumination levels, i.e. will saturate earlier, and information will be lost. Different solutions for widening the DR in CMOS image sensors have been presented in recent years. A comprehensive summary of existing solutions and their comparison have been presented in [11] and more recent solutions with the advantages and disadvantages are described in [12]. The imager described in this paper utilizes a multi-reset algorithm for each pixel when crossing a pre-determined threshold [13]. If the pixel crosses the threshold it will be reset using the AR scheme to further reduce the reset noise and its integration time is reduced, following the algorithm as described in section II.

The figures of merit for analyzing a Wide Dynamic Range (WDR) technique are Noise Figure (NF), minimal number of transistors required for pixel implementation, absolute DR and sensitivity of the pixel [12]. The two main competing WDR techniques to the multiple reset sensor are the logarithmic sensor [14] and the multiple-capture sensor [15]. The logarithmic sensor has a very simple pixel structure; however it's NF is rather high due to increased offset Fixed Pattern Noise (FPN) and it requires more complex color processing due to the nonlinear response. The logarithmic sensor has high spatial resolution but large FPN due to threshold variations, low sensitivity under low light conditions due to leakage current, slow response time under low light conditions and large image lag. The logarithmic sensor also has lower sensitivity in extended DR due to its companding ability in comparison to medium light levels. The multiple capture sensor has a very high DR while keeping the pixel structure very simple. The drawback of the multiple-capture sensor is that it requires extensive periphery Digital Signal Processing (DSP) circuitry. The data processing involves multiple Analog to Digital (A-D) conversions and frequent readout cycles from memory units that store the digitized pixel values from the previous captures. The multiple reset technique similar to the multiple capture technique has high DR and simple pixel circuitry but doesn't require extensive DSP capabilities, only an on chip memory to store the number of resets each pixel had

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undergone. The novel technique proposed in this paper is also superior to other multiple reset techniques in that it performs an AR not only for a new frame reset but every time a reset is needed for shortening the integration time. This method reduces gain FPN because the reset noise which is consistently quoted as a main contributor to the overall noise in CMOS APS imagers [16] is kept to a minimum when starting a new shorter integration time.

The variable topology partitioned pixel amplifier was first reported by our group in the sensors conference [17], here we will review the main concepts. The amplifiers architecture is an expansion of the design reported in [8], utilizing a single partitioned pixel amplifier with variable topology to satisfy the following schemes; 1) AR technique to minimize the reset noise for every time the pixel requires a reset, either for a new frame or for the Conditional Active Reset (CAR) of the wide dynamic range expansion 2) Active Column Sensor (ACS) readout technique to suppress pixel gain and offset variations 3) WDR expansion in which the pixel voltage is compared with a pre-determined threshold during certain integration times so that the pixel can be reset if it is going to enter saturation. The partitioned pixel amplifier reported in [8] satisfied the first two techniques using multiplexing. The HALLI utilizes the partitioned pixel amplifier design reported in [17] to satisfy the third technique as well, which will be described in detail in the following section. The advantages of the proposed column level partitioned pixel amplifier are; simplicity in the analog readout path, reduced chip size, and lower power consumption than using individual dedicated blocks for each technique.

The remainder of this paper is organized as follows. Section II presents a description of the system architecture. In section III, the sensor operation and circuit is described. Imager results are presented in Section IV. The conclusion is presented in Section V.

II. System Architecture

The novel imager architecture satisfies the AR technique combined with ACS readout technique for low light, low noise operation as described in [8]. For high light levels the WDR algorithm is employed utilizing a CAR technique for each pixel. The CAR technique is an improvement on the multiple reset technique described in [8], in which an active reset is used when resetting the photodiode to a shorter integration time instead of just performing a hard or soft conditional reset to the diode. The HALLI uses a single column parallel amplifier to satisfy the three techniques. A detailed explanation of the original AR technique can be found in [16]–[17]. We will just give the basic functionality of the method, as we use the AR technique not only when resetting the pixel for the next frame but every time we perform a conditional reset for the WDR expansion [15]. The AR technique employs a high gain amplifier in negative-feedback configuration to accurately sense and compare fluctuations in reset photodiode voltage against a reference waveform, while correspondingly suppressing these fluctuations by controlling the opposing reset current of the reset transistor used to charge the photodiode capacitance. A gradually increasing waveform is required to modulate the unidirectional drain current of the reset transistor. Temporal reset noise suppression is based on two feedback mechanisms: an amplification of the feedback capacitance via the Miller effect and modulation of the reset transistor drain current in negative feedback.

When higher illuminated scenarios are detected without some sort of WDR technique, the pixels will saturate and information will be lost. The implementation of our WDR expansion can be regarded as a multi reset algorithm as described in [13]. We propose here the use of a CAR scheme when implementing the WDR algorithm. The CAR scheme is described more in detail in section III, The WDR algorithm is described in detail in [13], and we will outline here the multiple reset technique given in [13]. The outputs of a selected row are read through the regular column parallel output scheme and are compared with an appropriate threshold, at certain time points. If a pixel value exceeds the threshold, a reset is given at that time point to that pixel. The binary information concerning having the reset applied or not is saved in a digital storage, to enable proper scaling of the value read. This enables the pixel value to be described as a floating-point representation. In this representation, the exponent will describe the scaling factor for the actual integration time, while the mantissa will be the regular analog output. Therefore, the light intensity of the pixel is calculated as:

$$Value = Mantissa \cdot X^{EXP}. \tag{1}$$

Where *Value* relates to the incident light intensity, *Mantissa* is the analog or digitized output value that has been read out at the end of the integration period, X is a chosen constant ($X > 1$), for example 2, that relates to the division of the integration time into progressively shorter intervals and EXP represents how many times the given pixel was reset over the entire integration period, i.e. the exponent. When using the rolling shutter method we use the combined time-space algorithm described in detail [13], we will give an overview of the algorithm. For a certain pixel instead of checking at different time points to get the exponential (scaling) term, we look at the pixels of different rows to get the same information. Every time we check the appropriate row and it is decided that a CAR is needed, the integration time of the pixel is reduced because the pixel readout is done in a rolling shutter manner. If we choose $X = 2$ as an example, we could look at row η at time zero to get the mantissa for row η, while we look at the pixels in row $\eta - N/2$ (where N is the total number of rows that set the frame time) to get the first exponent bit, as a result of the logic circuit decision for that row. We look at row $\eta - N/4$ to get the second bit for that row, at $\eta - N/8$ to get the third bit, etc. Therefore after a certain amount of comparisons we automatically get the required information, and scale the mantissa accordingly.

The general architecture of the proposed imager is presented in Fig. 1. The imager includes the sensor array, row decoder, column decoder, the variable topology partitioned pixel amplifier, sample and hold circuitry, processing element, SRAM memory and the memory row decoder. The imager works on a parallel column based readout using the rolling shutter

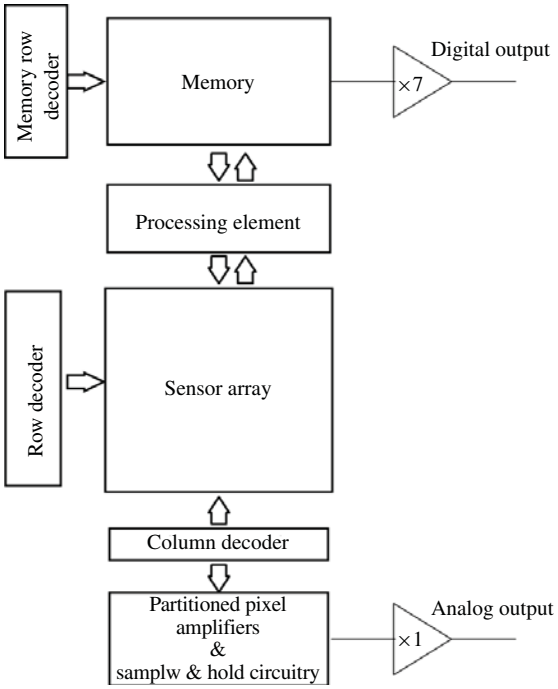


Fig. 1. General architecture of the proposed high and low light level CMOS imager.

technique as described in [13]. The sample and hold circuitry will sample the row that is being readout through the analog output and while each column is being readout in a serial mode the partitioned pixel amplifier is free for implementation of the WDR expansion. Therefore our proposed architecture does not affect the frame rate in comparison to the previously proposed imager in [8]. The processing element uses the information on the pixel read from the memory to decide whether a CAR is needed for higher light intensities. The condition on the AR to be performed is that the pixel voltage currently checking for the WDR information has to have crossed the threshold and that the previous row checked for the WDR information has to have reset as well. If these two conditions are not met, then the CAR is not employed on that pixel and the pixel voltage when readout will not saturate. The memory is independent from the rest of the circuitry and only shares the memory data bus with the processing element. Therefore the exponent value stored for the pixel that is being read out from the sample and hold circuitry, can be read out (on the Digital Output bus) along with the mantissa (through the analog Output line).

III. Sensor Operation

Due to the commonalities in the AR technique, ACS technique and the WDR expansion and the fact that they occur in staggered instances of time during a row access period, a single partitioned pixel amplifier with variable topology is proposed to accommodate all three techniques. Fig. 2. shows a simplified schematic of the circuit and feedback desired to accommodate the three techniques. In (a) we see the modified AR technique which is used to suppress temporal KT/C noise during the reset phase for both the new frame and the conditional WDR reset.

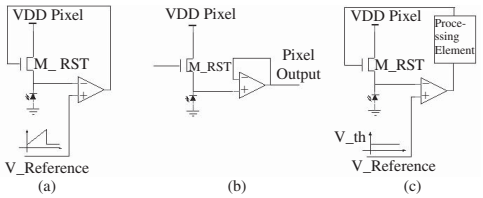


Fig. 2. Simplified schematic of the circuit topology to accommodate the three techniques. (a) Modified AR technique. (b) ACS readout technique. (C) WDR expansion-comparator mode (CM).

In the modified AR technique the V_Reference is a gradually increasing waveform required to modulate the unidirectional drain current of the reset transistor until it is driven rapidly low causing the amplifiers output to be driven rapidly to ground as it attempts to equalize the sensed photodiode node with the reference waveform. As a result, the gate of the reset transistor is lowered, and the negative feedback reset voltage is latched onto the photodiode. In (b) the ACS technique employs a high gain amplifier in unity gain configuration during readout for the suppression of spatial gain nonlinearity and offsets. In (c) the WDR expansion is employed by using the partitioned pixel amplifier as a comparator. The V_Reference is changed to the pre-determined threshold voltage and the voltage on the pixel is compared to that threshold. If the pixel voltage has crossed the threshold voltage (an indication that the pixel is going to saturate before the integration time is over) the comparator output is driven high and this signals the processing element. The processing element decides if a CAR is needed based on the information from the comparator (if the pixel crossed the threshold) and the information from the memory if the previous integration time point for that pixel was reset as well, i.e. if the previous integration time did not cross the threshold previously then the pixel will not saturate at the end of the pixels current integration time. If both values are true a CAR is activated by returning to (a) and the processing element stores the information for the current integration time point in the memory.

A schematic diagram of the proposed implementation showing a single column of the circuitry is presented in Fig. 3. The pixel architecture and column based partitioned pixel amplifier is based on [8]. We will give a description of the operation and describe more in detail our additions to satisfy the CAR WDR expansion. The partitioned pixel amplifier is implemented as a single stage folded-cascode amplifier consisting of the folded-cascode branch (M3-M10), the differential pair inputs (M1-M2) and the differential pair current source (M0, M_RS) as shown in Fig. 3. A current mirror is formed by transistors M7-M10, the polarity of the amplifier is toggled by switching the orientation of the current mirror connection from the common gate connection of M9 and M10 to either the drain of M7 or the drain of M8, thereby defining which branch serves as the input reference current to the current mirror and which branch serves as the amplifier output. Vb1-Vb4 are constant biasing voltages and ensure all transistors are in saturation throughout the operations.

Multiplexer A defines the polarity of the amplifier so the configurations of Fig. 2 can be established. Multiplexer B

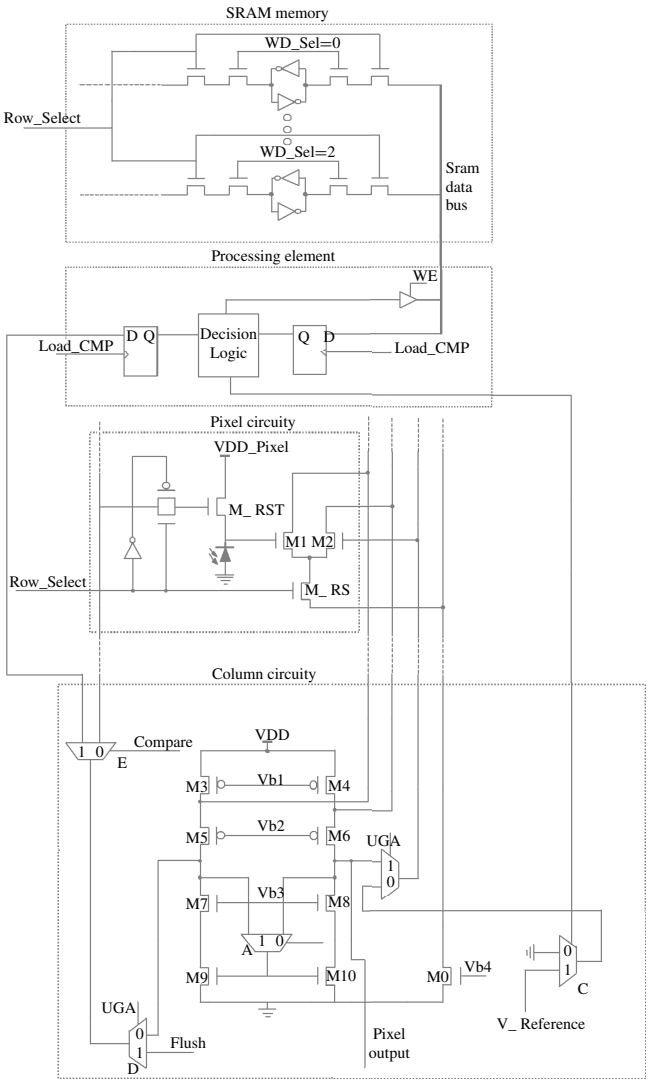


Fig. 3. Schematic of a single column of the proposed high and low level light imager.

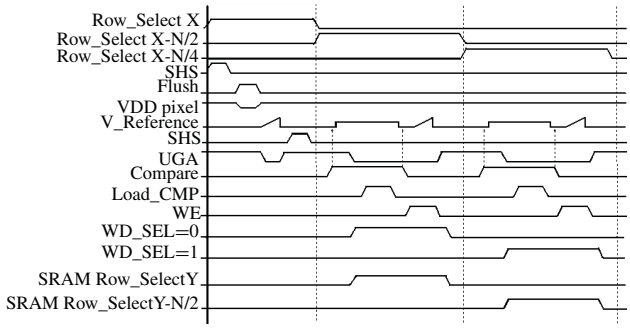


Fig. 4. Timing diagram of the proposed imager operation.

establishes unity gain feedback during sampling and connects the AR reference voltage to the positive amplifier terminal during AR. Multiplexer C controls the conditional CAR during the WDR algorithm and the AR during the pixel reset for a new frame, i.e. if a CAR is false the select signal coming from the processing element will be low thereby driving the positive terminal of the amplifier with GND and the pixel is not reset. Multiplexer D connects the feedback loop during AR and provides an optional flush signal to apply a hard reset to the pixel prior to the AR. The technique for applying a flush reset pulse to reduce image lag is described in [20]. Demultiplexer E controls the output of the amplifier during the WDR expansion. During WDR the amplifier is a comparator and the output of the amplifier is low if the pixel voltage did not cross the threshold voltage and high if it did cross the threshold voltage. The information regarding if the pixel crossed the threshold or not is driven to the processing element and the input to the reset transistor (M_RST) is held low so that the pixel will not reset until the CAR is given (only if the condition is true). The timing of the procedure can be seen in Fig. 4.

The processing element consists of two latches, the decision logic and a tri state buffer. The two latches hold the WDR information for the pixel being checked so that once the information is latched, the memory and the partitioned pixel amplifier are free to do other tasks, such as perform a CAR. The first latch stores the information from the partitioned pixel amplifier in comparator mode (CM) (giving the information if the pixel has crossed the threshold or not), the second latch holds the information from the memory regarding if the previous integration time point value has crossed the threshold. Only if these two conditions are true then the decision logic allows for a CAR, which is controlled through the select of multiplexer C in the column circuitry. The decision for the row being checked in the WDR algorithm is stored in the memory by enabling the tri-state buffer to drive the SRAM_DATA bus.

For the HALLI prototype, the memory consists of three SRAM cells for each pixel but more cells can be implemented thereby increasing the DR of the imager. The WD_SEL in Fig. 3, is used to select which SRAM cell to access out of the available three cells per pixel. SRAM implementation was chosen due to simplicity for a prototype imager. The information regarding the decision is used for both the exponent value for scaling the pixel voltage in (1) and for the next integration time CAR decision. The decision logic in the processing element always gives a positive value for the information latched from the memory when it is the first integration time being checked (T_{INT}/X^1). A plot of the control waveforms is shown in Fig. 4 for a single row of pixels. The first two integration times of the WDR algorithm are shown (the rest of the integration times have the same timing with only the row select changing per the WDR algorithm). The first column is the readout of the pixel voltage, first a Sample-Hold-Signal (SHS) is asserted with the amplifier in unity gain configuration signaling the Sample and Hold (S/H) circuitry to store the pixel voltage. The S/H circuitry consists of a column parallel offset compensated, input-independent switched capacitor amplifier [21]. All the columns of the row being read out are sampled at the same time and each column is then read out one at a time. A hard reset is followed through the Flush signal and then an AR is employed through the V_Reference signal. The AR is only asserted after the Unity Gain Amplification (UGA) signal is low whcih switches the polarity of the amplifier and puts it

in open loop. Finally a Sample-Hold-Reset (SHR) is asserted with the amplifier in unity gain configuration signaling the S/H circuitry to store the reset value. When the mantissa is finally read out the pixel signal voltage is subtracted from the reset voltage giving a correlated double sampling (CDS) value. This work uses a rolling shutter method and therefore this is not a true CDS because the reset value is that of the next frame. This CDS method still reduces offset FPN because the pixel's double sampling is still correlated to the same readout circuitry.

The second column is the control of the first row being checked for the WDR algorithm (row $\eta - N/2$, for $X = 2$), the third column is the second row being checked for the WDR algorithm (row $\eta - N/4$, for $X = 2$) and the fourth column not drawn is the third row being checked (row $\eta - N/8$, for $\eta - N/4$). For larger DR implementations, i.e. more SRAM cells implemented, the aforementioned sequence will continue until row $\eta - N/N$ is reached. The frame rate is not affected because the time to finish the WDR algorithm is much shorter than the time it takes for the current row to be read out through the S/H circuitry. The readout through the S/H happens in parallel to the WDR algorithm which includes storing the WDR information in the SRAM signaled by SRAM Row_Select and Write Enable (WE). In the waveform, notice that the same V_Reference is toggled between the AR (a gradually increasing pulse) to the pre-determined threshold V_th for WDR CM, allowing us to utilize the same partitioned pixel level amplifier with variable topology for both techniques when the UGA signal is low. When UGA is high the partitioned pixel amplifier is in unity gain sampling mode.

The Compare signal toggles the Demultiplexer E so the output of the amplifier in CM mode, checking the pixel crossed the threshold, can be stored in the processing element. The Load_CMP latches the amplifier output and the SRAM's output regarding the previous integration time in the processing element for a decision to be made regarding the current integration time. The new decision is stored in the SRAM through the WE buffer in parallel to performing the CAR if the decision was true. Notice the V_Reference always performs the increasing ramp for the CAR, but the amplifier won't receive the ramp if the decision was false because the processing element controls Multiplexer C which forces the input to the amplifier to be GND. With the proposed novel architecture in this paper, V_Reference is shared for all the columns in the pixel array removing the need to generate this signal for each column independently, ultimately increasing power consumption and die size. For the prototype reported here the V_Reference signal was generated off-chip through an external Texas Instruments 18bit low noise Digital to Analog Converter (TI DAC 9881).

IV. Imager Results

A test chip having a 128 × 128 sensor array has been fabricated in a mixed signal 0.18 μm CMOS technology. The SRAM memory has been implemented with three bit storage per pixel. Every time a CAR is initiated the pixel gets the full well capacity back, just now with a shorter integration time,

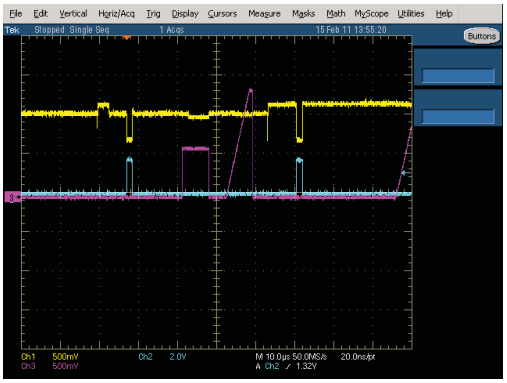


Fig. 5. Probed signals from the imager showing one pixel's voltage (yellow), V_Reference (purple) and the sampling of the pixel's voltage (blue). The pixel's voltage does not cross the threshold voltage (V_Refernce at V_th) and when the CAR is activated (V_Reference ramping up gradually) it does not reset the pixel's voltage.

giving a dynamic range of:

$$D(dB) = D_1(dB) + 20^* \log\left(\frac{T_{INT}}{T_{1INT}}\right). \quad (2)$$

Where $D(dB)$ is the total dynamic range in dB, $D_1(dB)$ is the dynamic is range of the imager without WDR expansion, i.e. the intrinsic DR of the N-well over P-Substrate photodiode, T_{INT} is the integration time for the lowest light intensity and T_{1INT} is the integration time for the highest light intensity. In our case of $X = 2$ and with a three bit expansion we get integration times of $T_{INT}/64$, $T_{INT}/32$, and $T_{INT}/16$, where T_{INT} is the number of row in the imager, i.e. 128. Therefore the dynamic range of the imager with a three bit expansion is:

$$D(dB) = D_1(dB) + 20^* \log\left(\frac{128}{16}\right) = 54 + 18 = 72dB. \quad (3)$$

For comparison, the size of the memory could be increased to store seven bits for each pixel, i.e. the highest light intensity now has an integration time of one row and this is the maximum achievable DR for a 128 row sensor with $X = 2$. The DR of CMOS image sensor in this case would be:

$$D(dB) = D_1(dB) + 20^* \log\left(\frac{128}{1}\right) = 54 + 42 = 96dB. \quad (4)$$

To validate the HALLI functionality the signals in the chip were probed for one pixel as shown in Fig. 5. The top line (yellow) is the pixel voltage under low illumination. The pixel voltage is reset to 1.1V and illumination causes the voltage to drop (reverse biased photodiode). The bottom line (blue) is the sample and hold signal, i.e. the pixel voltage is only valid when the sample and hold signal is high because the rest of the time the pixel voltage is internal to the pixel and cannot be probed. As shown in Fig. 5. For the first sample and hold, the pixel voltage after a certain integration time and illumination, reaches ~730mV. As per the WDR algorithm and timing signals displayed in Fig. 4. The V_Reference signal (purple) is driven to the threshold voltage (V_th) to check if the pixel will saturate at the end of the integration time. As the pixel voltage did not cross the threshold, when the V_Reference is changed to an increasing ramp signal for the CAR the pixel

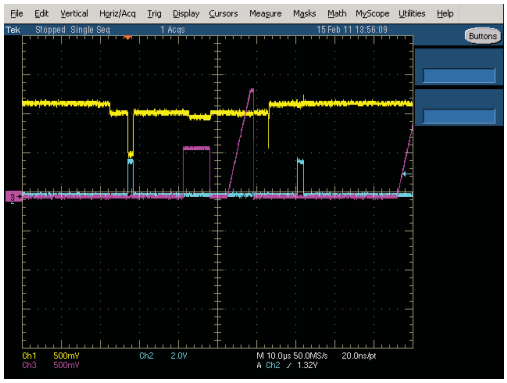
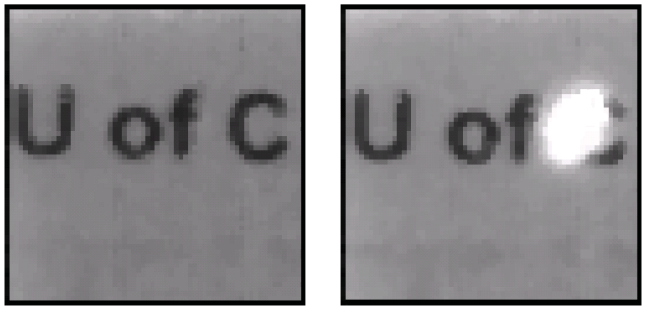


Fig. 6. Probed signals from the imager showing one pixel's voltage (yellow), V_Reference (purple) and the sampling of the pixel's voltage (blue). The pixel's voltage does cross the threshold voltage (V_Refernce at V_th) and when the CAR is activated (V_Reference ramping up gradually) it resets the pixel's voltage.



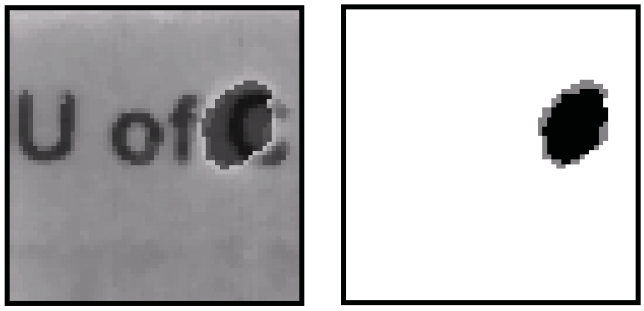
(a) (b)

Fig. 7. Picture taken with HALLI and WDR turned off. (a) Low light illumination and (b) same illumination but a bright laser was focused on the image saturating a portion of the image.

voltage does not reset, as explained in section III. This can be seen in the second sample and hold in Fig. 5. where the same pixel voltage is read out right after the CAR and it did not reset. Important to state that under normal rolling shutter imager operation the pixel voltage will be read out only at the end of the integration time and not as performed in Fig. 5. The two simultaneous sample and hold below was done only for imager validation purposes.

The same scenario described above for Fig. 5. applies below to Fig. 6. The only difference in Fig. 6. Is that a higher illumination level was used so that the pixel voltage crosses the threshold voltage, i.e. the pixel will saturate at the end of the integration time and information will be lost without the WDR implementation. The pixel voltage in Fig. 6. reaches ~400mV when it is first sampled and when the CAR is activated (as described in section III) the pixel voltage is reset to 1.1V (this can be seen with the second sample and hold). Now the pixel again has the full well capacity to keep on integrating with the shorter integration time per the WDR algorithm and information won't be lost.

An image taken from the HALLI with the WDR turned off under low light illumination is shown in Fig. 7(a). The same image is taken again with the HALLI and WDR turned off but with a bright laser focused on part of the image. The laser causes part of the image to saturate and information is lost



(a) (b)

Fig. 8. Picture taken with HALLI and WDR turned on. (a) MANTISSA is shown and (b) memory (EXP value). White represents no resets, grey represents one reset at T/2 and black represents two resets, i.e. at T/2 and T/4.

TABLE I
CHIP ATTRIBUTES

Parameter	Measurement
Array Size	128 × 128
Pixel Size	7 μm × 7 μm
Supply Voltage	1.8V
Fill Factor	30%
Conversion Gain	29 uv/e^-
Dark Current Density (worst case)	31 nA/cm^2
Pixel FPN (reset frame)	0.12%
Column FPN (reset frame)	0.06%
QE (at 610 nm)	31%
Readout Non-Linearity	0.6%
Full Well Capacity	35 ke^-
Operation rate	30 fps
Partitioned Amplifier Gain	66 dB
Variable Topology Amplifier Bandwidth	500 kHz
Variable Topology Amplifier Phase Margin	81°
Variable Topology Amplifier Static Power Consumption	108 uW
Dynamic Range without WDR	54 dB
Extended Dynamic Range	3 bits

when the WDR implementation is off, as shown in Fig. 7(b) with part of the image saturated. Again an image is taken with the HALLI and the bright laser but with the WDR turned on and the results are shown in Fig. 8. We can see details, as per the MANTISSA image, and we can recover the whole WDR value with the combined EXP image data, Fig. 8(b). Future work is aimed for presenting the whole WDR value in a limited display.

Table 1. Summarizes the HALLI's measured performance and figures of merit. Main features to point are the dynamic range of the imager without any WDR expansion is 54 dB, i.e. just well capacity. With the three bit expansion implemented in the HALLI we get an extended dynamic range of 72 dB (18 dB DR expansion) and by simply increasing the memory size to store 7 bits per pixel an extended dynamic range of 96 dB (42dB DR expansion) can be achieved. For comparison purposes we compare the extended DR due to the WDR algorithm with other CMOS imagers performing similar

multiple reset algorithms and we leave the intrinsic DR out of the comparison. S. W. Han *et al.* [22] have reported on a 42 dB DR expansion, P. M. Acosta-Serafini, *et al.* [23] reported on 60 dB DR expansion, A. Belenky, *et al*. reported on 24 dB expansion for 4 bit WDR algorithm and 48 dB DR expansion with 8 bit WDR algorithm.

The prototype chip fabricated uses an N-Well over P substrate pixel structure in a standard CMOS 0.18 μm process giving a measured dark current density in the worst pixel of 31 $\eta A/cm^2$. The authors would like to note that if the same design was fabricated on an imager process with a pinned-photodiode the dark current is expected to decrease. The current chip peripherals as mentioned section III include one S/H circuitry for the reset voltage and one for the integrated voltage (SHR and SHS shown in the timing diagram of Fig. 4 respectively) and allow only for a partial CDS to be employed (the reset voltage is that of the next frame). The authors would like to note that the peripherals could be extended with the existing HALLI architecture to support a digital CDS mechanism in which the reset noise is eliminated at the cost of extra space and power for memory to store the reset voltage of the same frame being sampled for read out. With the AR technique and the partial CDS the reset noise was measured at 8.9 e^-. The variable topology column parallel partitioned pixel amplifier consumes 108 μW static power consumption. The amplifier performs all the tasks required for high and low light level imaging, i.e. AR, ACS and WDR, thereby reducing the overall chip power in contrast to having dedicated blocks to perform each task separately. The prototype has 128 columns, therefore the total static power consumption of the amplifiers is 13.8 mA, approximately one third the power of an architecture having dedicated blocks to perform all the tasks which can become substantial when large pixel arrays are used.

V. Conclusion

A High and Low Light Imager (HALLI) developed in a CMOS process has been presented. The HALLI utilizes a single column parallel partitioned pixel amplifier with variable topology for the detection of both high and low light levels in the same frame. For high light level detection, a Wide Dynamic Range (WDR) algorithm is utilized. For low light level detection, two noise reduction techniques are employed; Active Reset (AR) and Active Column Sensor (ACS) readout technique. Due to the commonalities in the high and low light level readout techniques, and the fact that they occur in staggered instances of time, a single partitioned pixel amplifier which can be configured in various modes of operation is used. The advantages of using a single column parallel partitioned pixel amplifier are simplicity in the analog readout path, power reduction, reduced chip size, and lower power consumption then using individuals dedicated blocks for each technique. The CMOS imager was designed and fabricated in a mixed signal 0.18 μm CMOS technology.

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