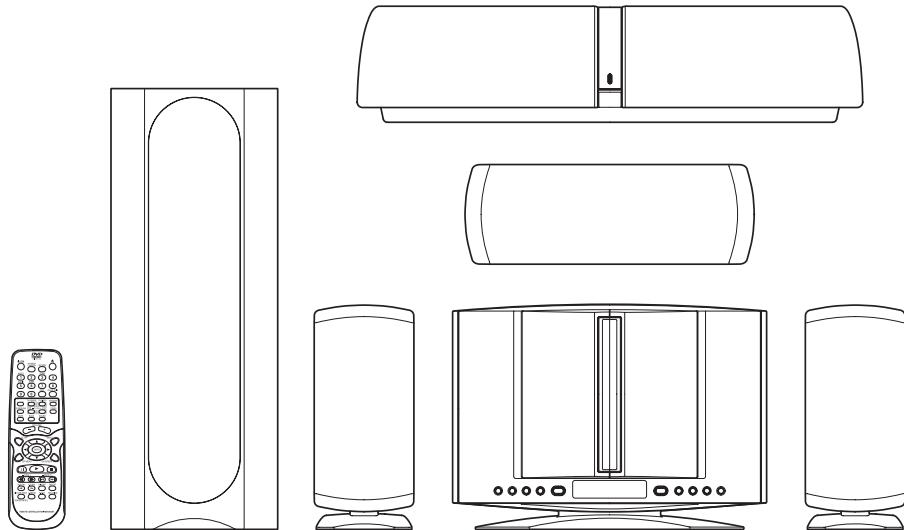


FILE NO.

Service Manual**DVD Home Theater
System****DWM-4500 (US)
DC-TS830WL (CA)****CONTENTS****PRODUCT CODE No.**
129 712 00 US
129 712 04 CA

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LASER BEAM SAFETY PRECAUTION

- Pick-up that emits a laser beam is used in this CD player section.

CAUTION :

USE OF CONTROLS OR ADJUSTMENTS
OR PERFORMANCE OF PROCEDURES
OTHER THAN THOSE SPECIFIED HEREIN
MAY RESULT IN HAZARDOUS RADIATION
EXPOSURE

LASER OUTPUT 0.6 mW Max. (CW)

WAVELENGTH 790 nm

DVD MECHANISM REPLACEMENT

1. Cautionary instructions in handling the assy (Safety instructions)

Optical pickup

The laser beam used in the pickup is classified as "class 2". Exposing your eyes or skin to the beam is harmful. Take care not to do so.

(Caution against static electricity and leakage voltage)

Ground securely the work tables, tools, fixtures, soldering irons (including those made of ceramic) and measuring instruments used in the production lines and inspection departments that handle loaders. The workers shall also be grounded.

(Cautionary instructions in handling)

Do not touch the object lens when handling a loader, or the lens will be stained, resulting in inadequate playability.

There is no power supply protection circuit provided for this product or adjustment/inspection device. Short-circuiting may lead to fire or damage.

Take care so as to protect from exposure to water, the entry of metallic pieces or dew condensation.

In particular, a strong magnet adjacent to the pickup will not only get inoperative but can damage the pickup if a small metallic piece, such as a screw or swarm, enters.

The loader edge can cause injury if inadvertently handled.

Do not touch a rotating disk, or injury may result.

This product is a precision device. Handle carefully.

A shock or dropping will cause misalignment or destruction. If it should occur, refer to clause 2.

This product is so designed as to endure an initial shock equivalent to a drop from a height of approx. 90 cm under the packed condition.

After the initial shock, the resistivity will still remain at a level of 50 to 60 G, but the mechanical robustness will weaken.

Do not place in a dusty location.

The entry and deposition of dirt into or on the pickup lens or moving section will cause malfunction or degradation.

(Connectors)

Do not connect or disconnect while power is on.

Connecting or disconnecting signal wires or the main power cord when the power is on may destruct the unit or fixture.

When connecting, push all the way in securely.

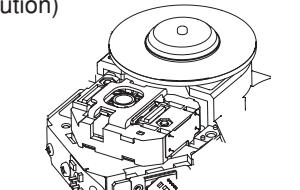
An insufficient insertion may cause a bad contact, leading to an erroneous operation.

Do not connect or disconnect roughly by an excessively strong force, or a broken wire or bad contact may result.

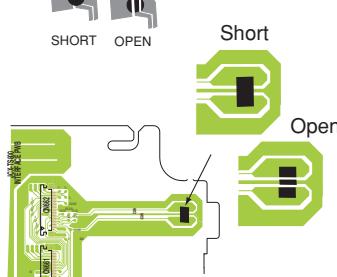
Semiconductors are connected. Do not touch connector terminals directly.

If the worker is grounded, there is nothing to worry about static electricity, but the rust on the connector terminal surface caused by the touch may result in bad contact.

(Caution)



Before disconnecting FFC cable from mechanism, make it "SHORT" as shown left.
After connecting FFC cable to mechanism, make it "OPEN" as shown left.



INTERFACE P.W.BOARD

Before disconnecting FFC cable from main p.w.b., make it "SHORT" as shown left.
After connecting FFC cable to main p.w.b., make it "OPEN" as shown left.

(Power source)

The power source need be good in quality (free from instantaneous interruptions or noises).

A low quality power source may well cause malfunction.

(Storage)

Do not place or store in a dusty place or a place where dew condensation is possible.

The entry and deposition of dirt or dust into or on the pickup lens or moving section will cause malfunction or degradation.

Also, dew condensation causes rust; the rust penetrate into the precision part of a pickup, causing malfunction, or degrading the optical quality of the internal lens and reflector, which also leads to malfunction.

SERVICE MODE

A. Market / Region SETUP

In the initial condition for this model, Market and Region information are undefined.

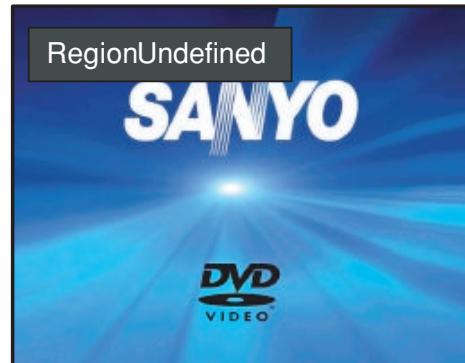
In the following cases, be sure to set up Market/Region.

1. When updating the system using CD-R
(Part code : 0PRADC9705--AC).

2. When replacing a DVD substrate.

While Market/Region information are undefined,
the message "Region Undefined" is displayed on the screen.

NOTE: Even if the condition is not under 1 or 2 above, if the message "Region Undefined" is displayed, be sure to set up Market/Region.

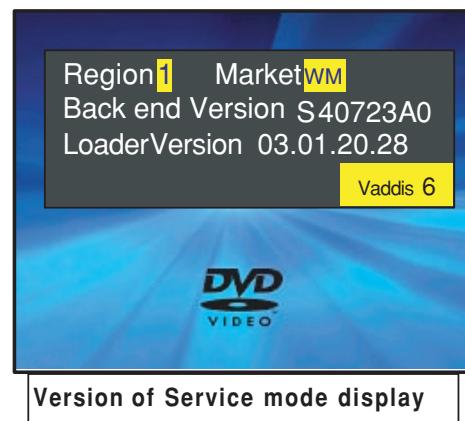


Undefined Market/Region display

B. How to enter Service Mode.

1. Using the buttons on the main unit

- 1-1. Display on "No Disc" by Function button.
1-2. Immediately (within one second) after pushing stop button both and power buttons simultaneously , push play button.



Version of Service mode display

C. Setup Procedures

1. Displaying SERVICE MODE screen

Display Service Mode screen following the instructions "How to enter Service Mode" above.

2. Displaying Internal Setup screen

Push PRESET+/NEXT button within three seconds after operating the Service Mode display.

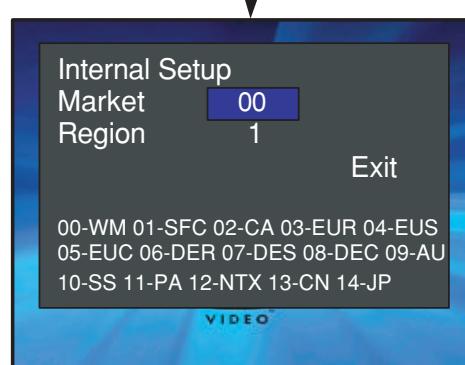
On the Internal Setup screen shown on the right, set up Market and Region.

- 3.1. While a highlighted indicator is displayed on the right side of the Market denotation, push numeric buttons on the remote controller.

When you push wrong number , push CLEAR button.
(The indicator reset to "00")

Be sure to input by double figures.

Market code of WM model is "00", and CA model is "02".



Screen of Internal Setup

- 3.2. Specify the code of the model in accordance with the Market/Region Setup Table above.

- 3.3 Once the desired code is displayed, push ▼ button to move the highlighted indicator to the Region input area.



Market Setting

SERVICE MODE

4. Setting REGION code

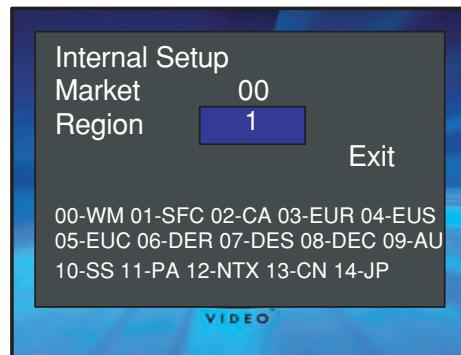
4.1 While a highlighted indicator is displayed on the right side of the Region denotation, push ENT, ▶ and ◀ each button on the remote controller. With each push the indicator will advance as shown below.

1 <-> 2 <-> 3 <-> 4 <-> 5 <-> 6

The region coder of US and CA is 1.

4.2 Set up the region coder currently displayed on the set.

4.3 Once the desired number is displayed, push ▼ button to move the highlighted indicator to Exit area.



Region Setting

5. Saving settings

5.1 Make sure that the Market and Region settings are properly set.

(If any of the settings are incorrect, you can make a change by moving the indicator using ▲ button, and following procedures 3 and 4 above.)

5.2 After ensuring that the settings are all correct, push ENT button while the indicator is on Exit area.

The settings are now saved.

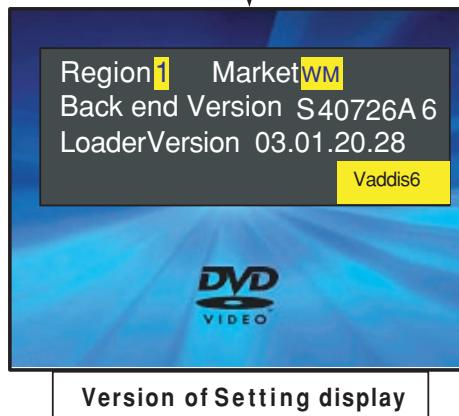
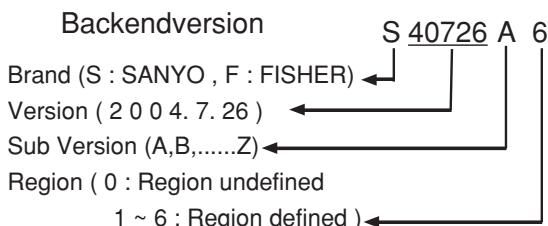


Save of Setting Data

6. Finishing settings

6.1 After a few seconds, the Internal Setup screen disappears, and then the Service Mode screen is displayed again for three seconds as shown on the right.

You should check the settings.



Version of Setting display

6.2 Power OFF.

SERVICE MODE

D. IMPORTANT NOTE

1. Once the "Market/Region" settings are written into EEPROM (IC810) on the DVD substrate, they cannot be reset.
(However, updating the system using CD-R enables you to make new settings.)
2. While the Internal Setup screen is displayed, pushing the Power button enables you to terminate the operations without making any settings.

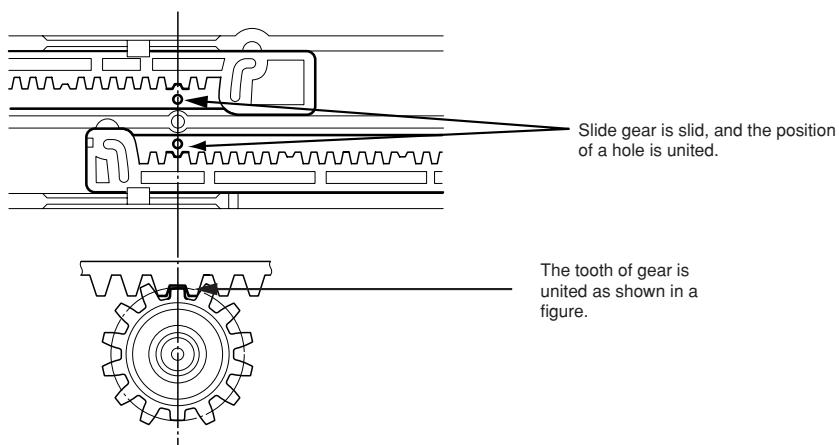
HOW TO LOAD SOFTWARE FOR MPEG P.W.BOARD

1. Power on, then open tray.
2. It take on CD-ROM for UPDATE software to the tray, and tray close.
3. TV screen display "Reading" and FL display "UPDATING"
4. For the time being, tray open and FL display "GOOD-BYE".
(caution) The update is not completed though the tray opens.
5. When software loading finished, "GOOD-BY" on a FL display disappears.
6. Next, set up market code and region code by "SERVICE MODE"
CD-ROM part code is "0PRADC9687--A".

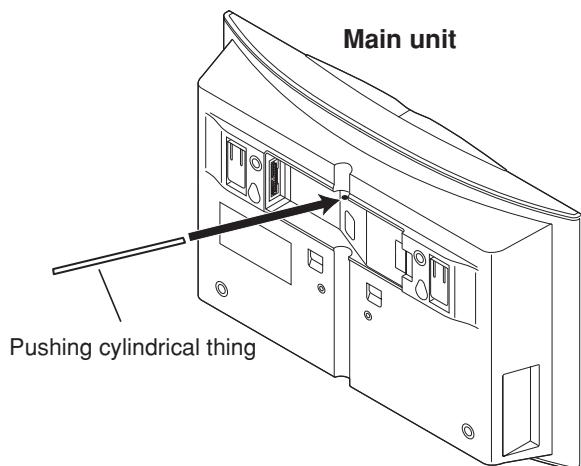
CAUTIONS FOR PWB OR IC ASSY EXCHANGE

After an MAIN board(614 332 3860) or IC ASSY(410 531 3201) exchange should carry out loading of the software by the newest CD-R, and should check operation.

How to attach gear rack

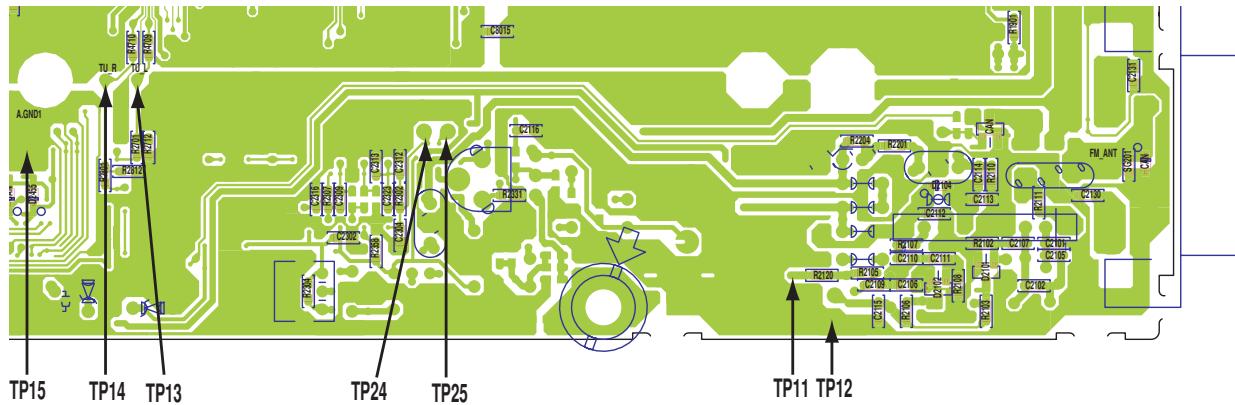
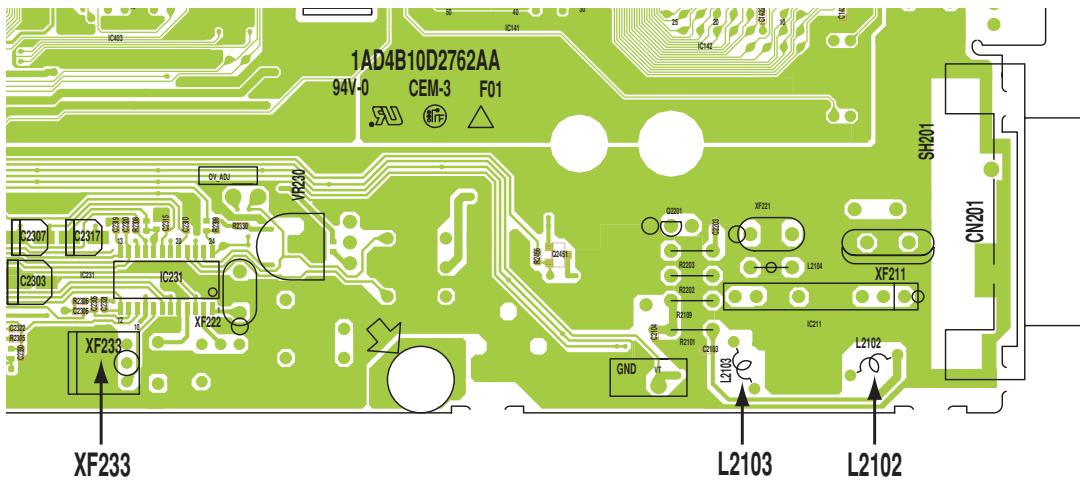


How to take out the disc.



TUNER ADJUSTMENT

- Use a plastic screw driver for adjustments.
- Speaker impedance : 8 ohms
- MODE : ST (Stereo)
- TUNING FM : 87.5 - 108MHz

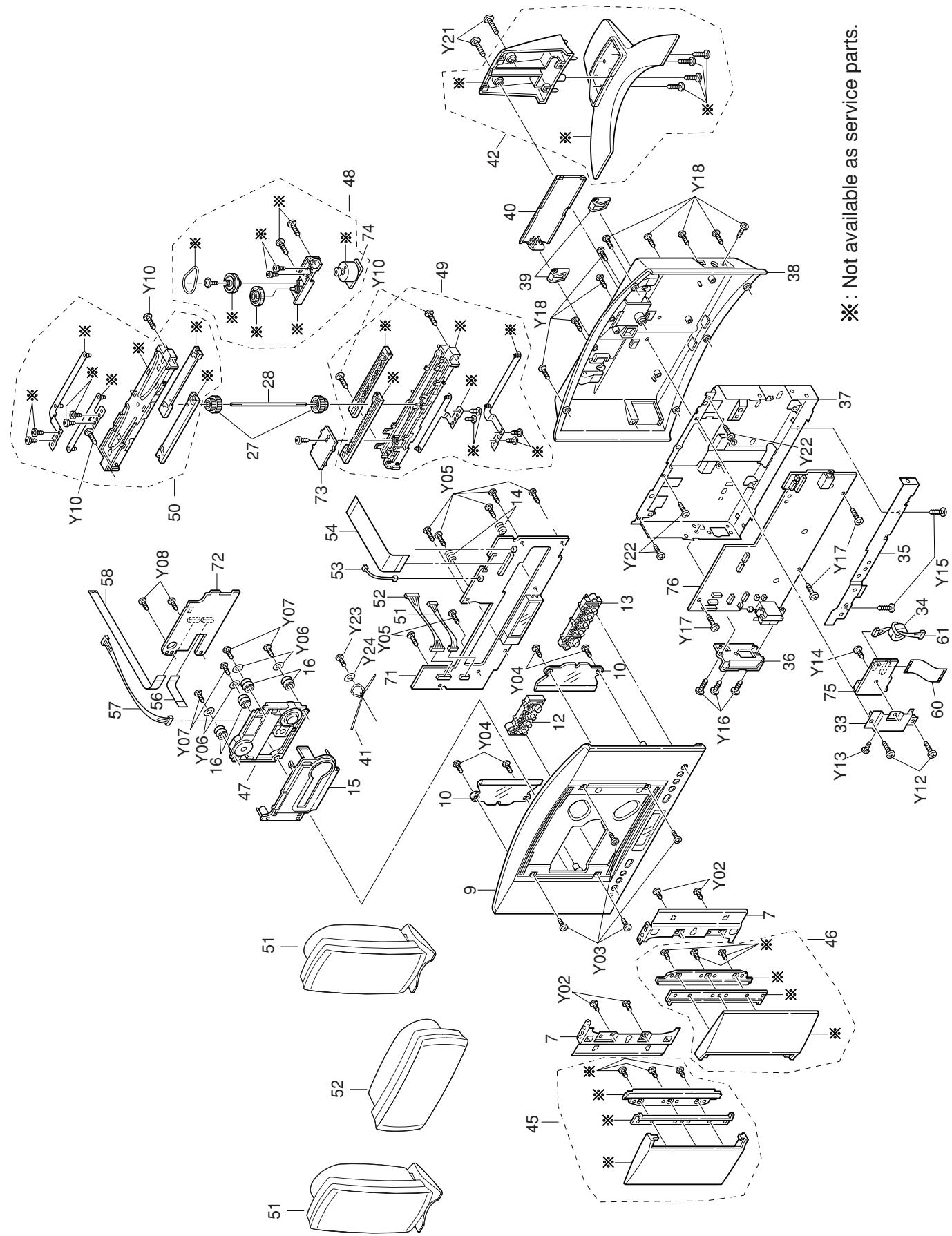


Antenna : 75Ω unbalanced direct, Modulation : 1 kHz
 Dev. : ±22.5kHz(MONO), ±22.5kHz(STEREO), ±6.75kHz(PILOT)
 RF Level : dBuV EMF
 Output Level : about 100mV at TP13, TP14, TP15

1. FM

Step	Adjusting Circuit	Connection		SG Frequency	Adjustment	Remark
		Input	Output			
1	IF Adjustment	FM Ant SG=66dB μ V	IC231 3-22Pin TP24,25	98.0MHz	XF233	0.0±0.05V
2	Cover	---	TP11 (H) TP12 (E)	87.5MHz	L2103	1.1±0.1V
				108.0MHz		< 9.0V
3	Tracking	FM Ant SG=8dB μ V	TP13 (L) TP14 (R) TP15 (E)	90.0MHz	L2102	Max.
				106.1MHz		

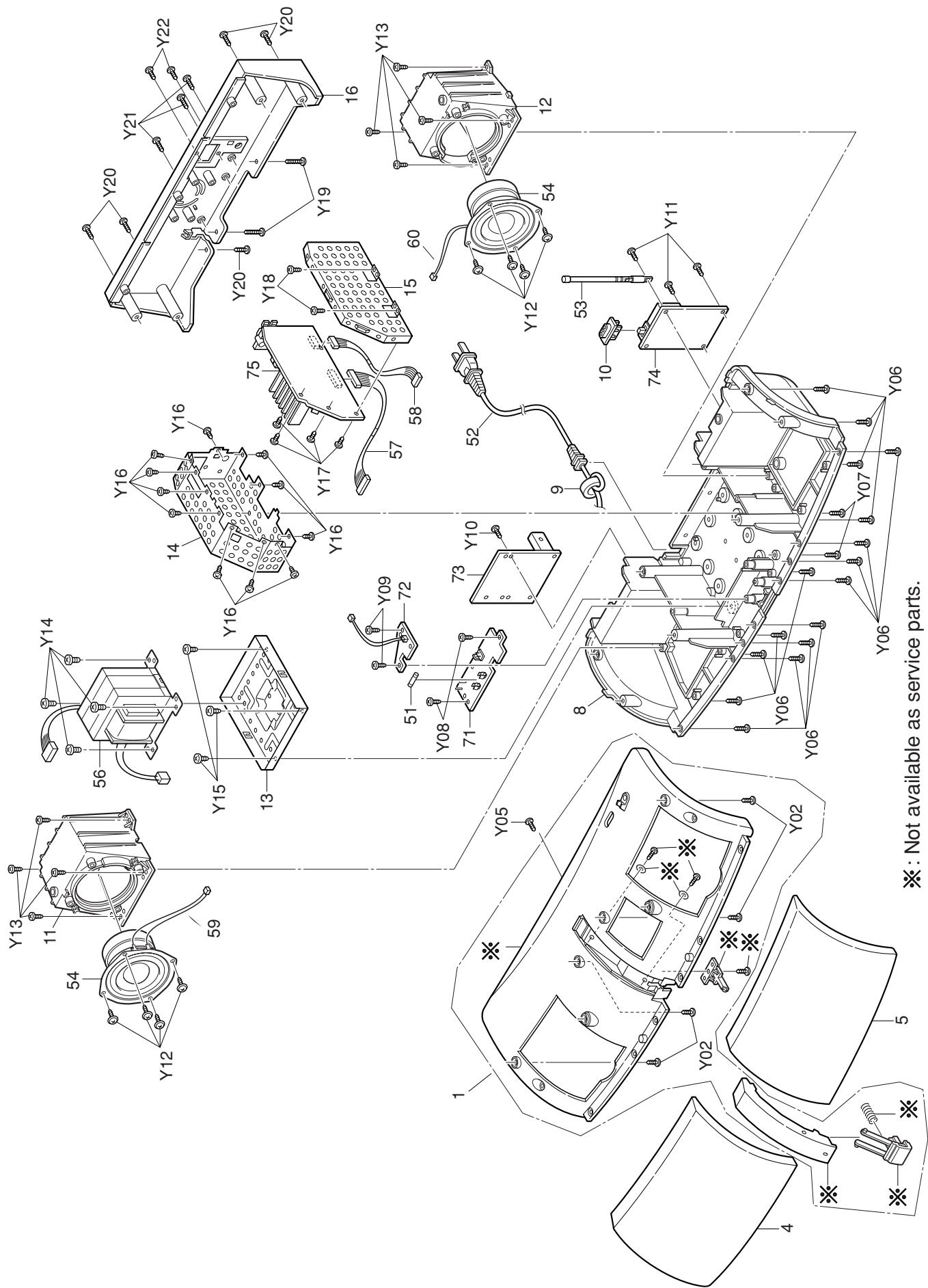
EXPLODED VIEW (CABINET & CHASSIS MAIN UNIT)



PARTS LIST

REF.NO.	PART NO.	DESCRIPTION
SG115	△ 645 055 3202	SURGE-ABSORBER,SURG_X
SG116	△ 645 055 3202	SURGE-ABSORBER,SURG_X
SG117	△ 645 055 3202	SURGE-ABSORBER,SURG_X
SG120	△ 645 055 3202	SURGE-ABSORBER,SURG_X
SG130	△ 645 055 3202	SURGE-ABSORBER,SURG_X
SG160	△ 645 055 3202	SURGE-ABSORBER,SURG_X
SG161	△ 645 055 3202	SURGE-ABSORBER,SURG_X
SG165	△ 645 055 3202	SURGE-ABSORBER,SURG_X
SG201	645 055 3202	SURGE-ABSORBER
SG408	△ 645 055 3202	SURGE-ABSORBER,SURG_X
SG409	△ 645 055 3202	SURGE-ABSORBER,SURG_X
SG418	△ 645 055 3202	SURGE-ABSORBER,SURG_X
SG428	△ 645 055 3202	SURGE-ABSORBER,SURG_X
SH201	614 325 5796	SHIELD,FM ANT
VR230	645 003 5586	VR,SEMI,22K N
X1100	645 045 8293	OSC,CRYSTAL 27.000MHZ
X2451	645 023 4965	OSC,CRYSTAL 7.2MHZ
XF211	645 026 2975	FILTER,BP 108MHZ
or	614 252 1045	FILTER,LC
or	645 059 0047	FILTER,BP
XF221	645 010 7665	CERAMIC FILTER 10.70MHZ
or	645 054 1223	CERAMIC FILTER 10.70MHZ
or	614 231 0199	FILTER
or	614 030 5074	I.F FILTER
XF222	645 010 7665	CERAMIC FILTER 10.70MHZ
or	645 054 1223	CERAMIC FILTER 10.70MHZ
or	614 231 0199	FILTER
or	614 030 5074	I.F FILTER
XF233	645 039 9923	TRANS,IF 10.7MHZ
or	645 040 9981	TRANS,IF 10.7MHZ

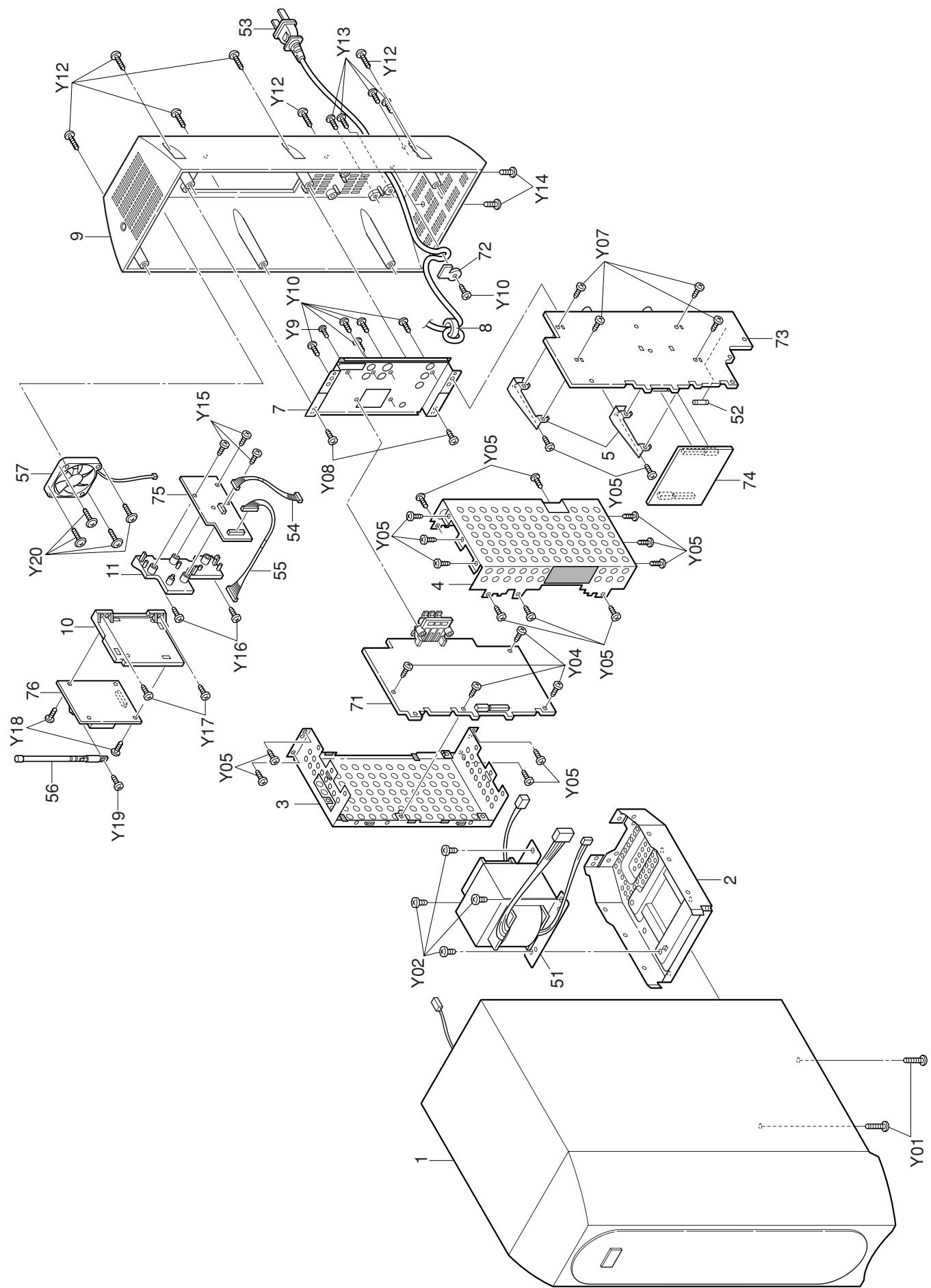
EXPLODED VIEW (REAR SPEAKER)



PARTS LIST

REF.NO.	PART NO.	DESCRIPTION
or	405 014 4509	TR 2SC2412K-R
or	405 011 1006	TR 2SC1623-L6
Q3411	405 146 2107	TR KTC3875-Y
or	405 146 2206	TR KTC3875-GR
or	405 014 4509	TR 2SC2412K-R
or	405 011 1006	TR 2SC1623-L6
R3413	△ 402 095 2202	RESISTOR 6.2 J- 2W
R3513	△ 402 095 2202	RESISTOR 6.2 J- 2W
RY340	△ 614 224 4531	RELAY
RY341	△ 614 224 4531	RELAY
S3410	645 067 1982	SWITCH,SLIDE 1P-2T
SCR32	411 191 4201	SCR S-TPG BRZ+FLG 3X12
SCR33	411 191 4201	SCR S-TPG BRZ+FLG 3X12
SCR34	411 187 2808	SCR S-TPG BIN 2.3X8
SCR35	411 187 2808	SCR S-TPG BIN 2.3X8
SG330	645 055 3202	SURGE-ABSORBER
SG341	645 055 3202	SURGE-ABSORBER
SG342	645 055 3202	SURGE-ABSORBER
SG351	645 055 3202	SURGE-ABSORBER
SG352	645 055 3202	SURGE-ABSORBER
SVR34	645 006 5347	VR,SEMI,47K N
SVR35	645 006 5347	VR,SEMI,47K N

EXPLODED VIEW (SUBWOOFER SPEAKER)

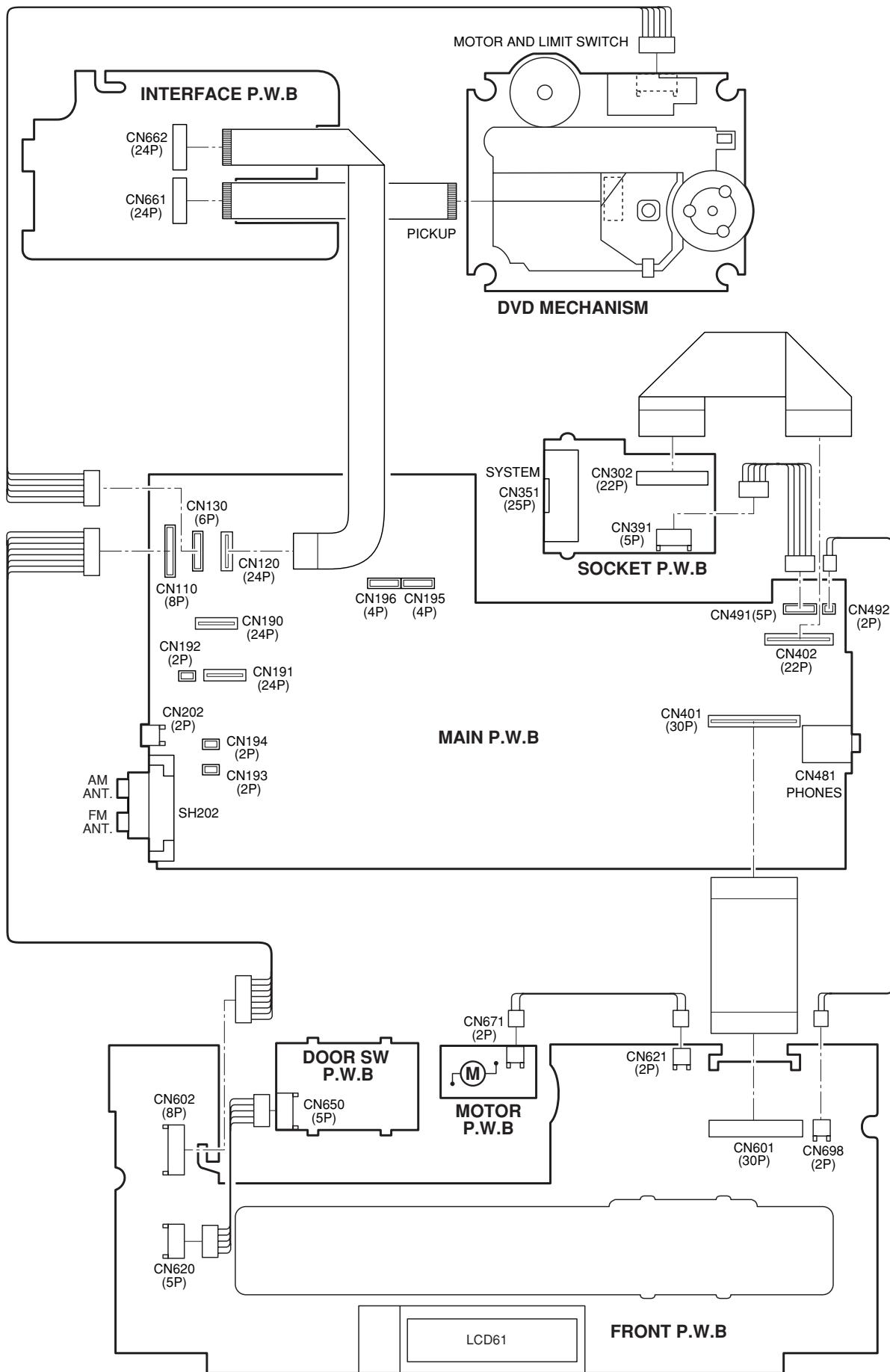


PARTS LIST

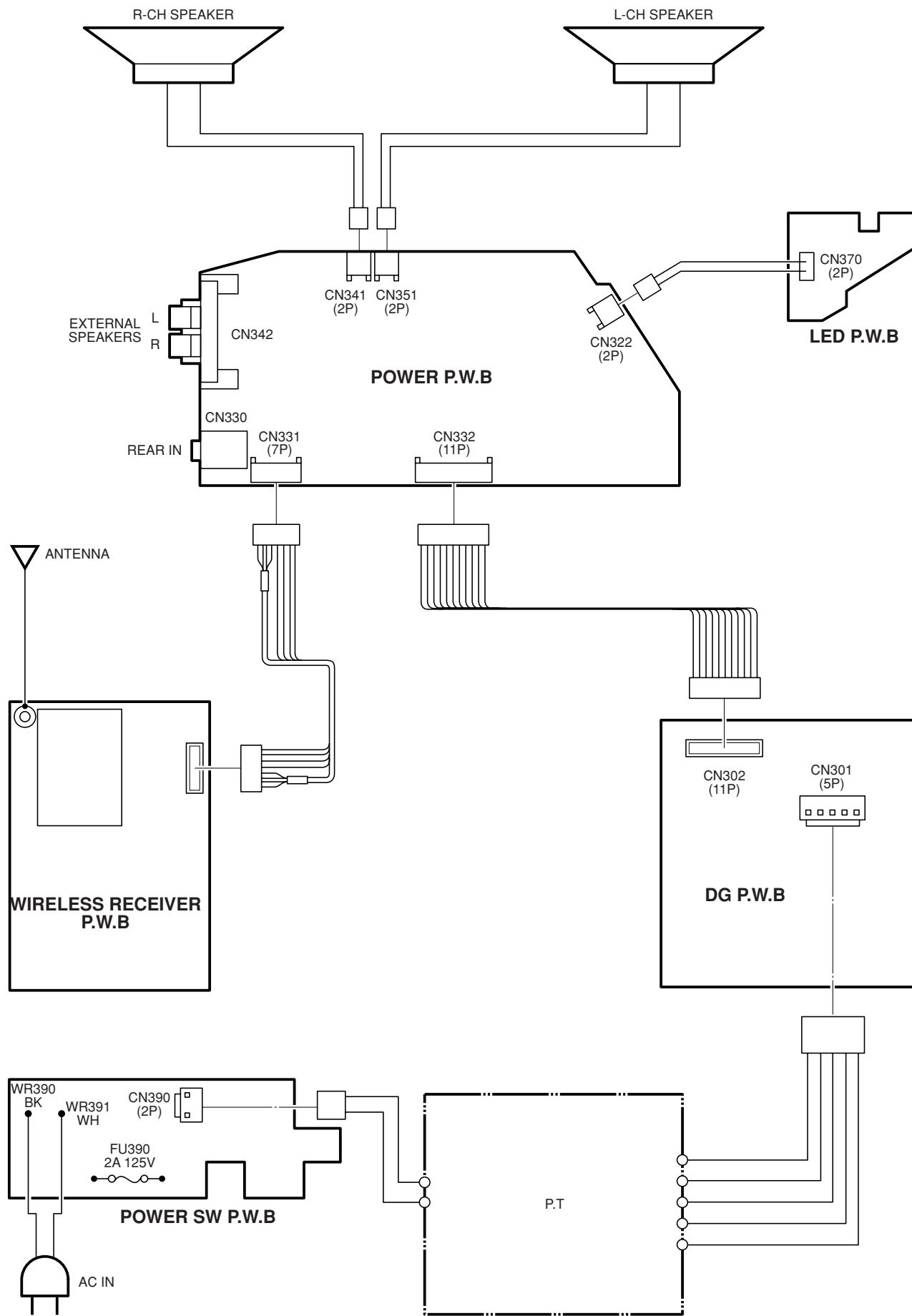
REF.NO.	PART NO.	DESCRIPTION
L3001	645 075 2223	FILTER,LP
L3002	645 075 2223	FILTER,LP
L3101	645 034 7887	INDUCTOR,1000 OHM
or	645 020 1813	INDUCTOR,1000 OHM
or	645 045 7869	IMPEDANCE,1000 OHM P
L3102	645 034 7887	INDUCTOR,1000 OHM
or	645 020 1813	INDUCTOR,1000 OHM
or	645 045 7869	IMPEDANCE,1000 OHM P
S3000	645 075 2254	SWITCH,SLIDE 2P-4T
X3000	645 059 1525	OSC,CERAMIC 4.19MHZ

NOTE _____

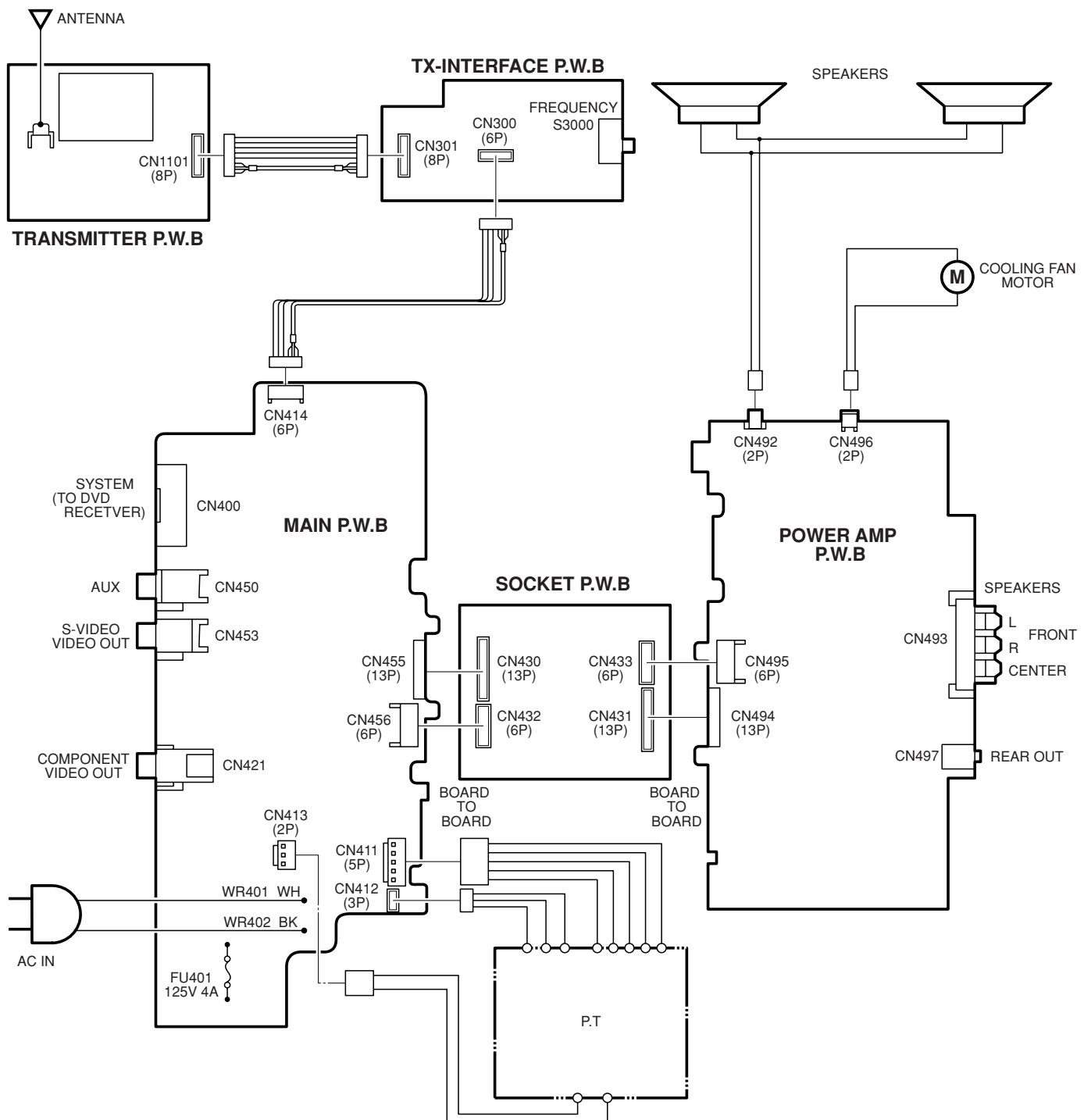
WIRING CONNECTION(MAIN UNIT)



WIRING CONNECTION(REAER SPAEKER)

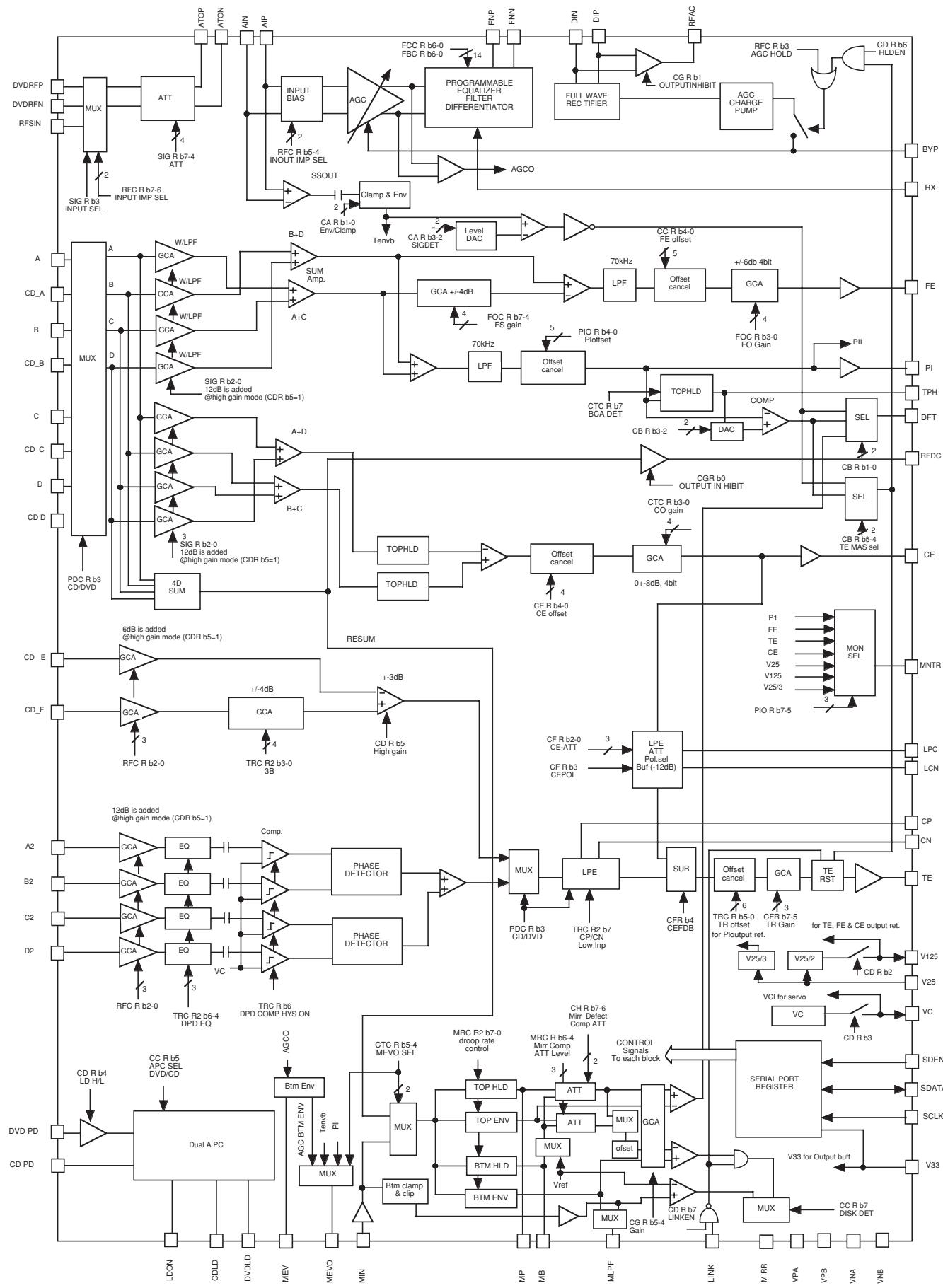


WIRING CONNECTION(SUBWOOFER SPAEKER)



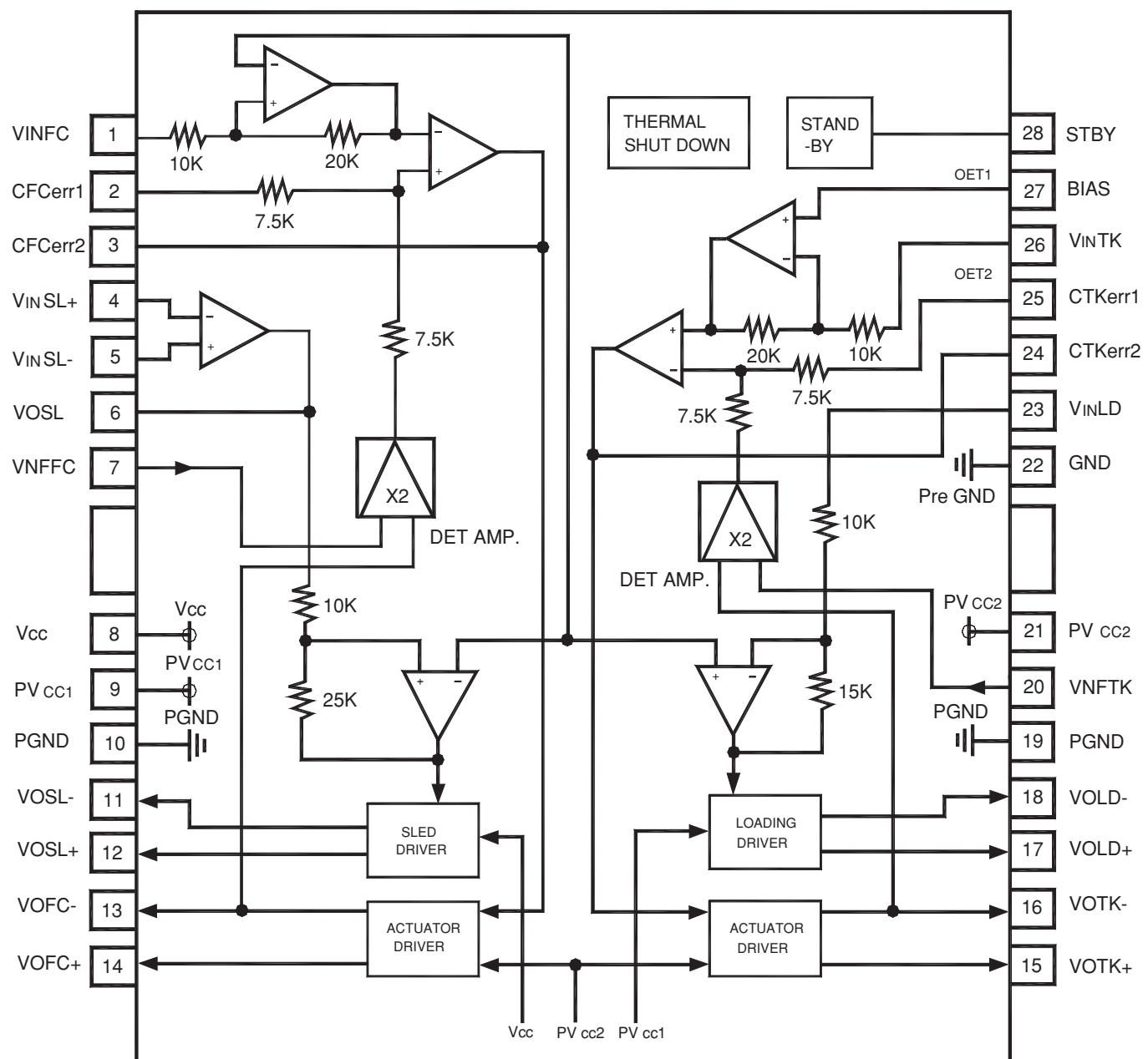
IC BLOCK DIAGRAM & DESCRIPTION

IC120 ZR36707TQC-N(READ CHANNEL)



IC BLOCK DIAGRAM & DESCRIPTION

IC103 BA5954FP(MOTOR DRIVE)



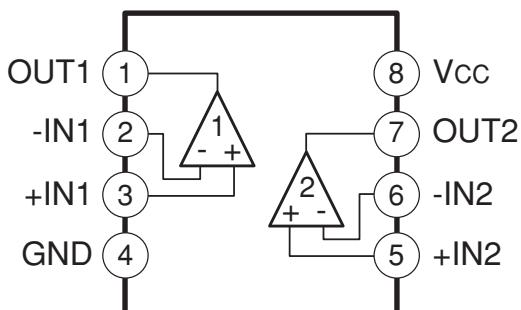
IC BLOCK DIAGRAM & DESCRIPTION

IC103 BA5954FP(MOTOR DRIVE)

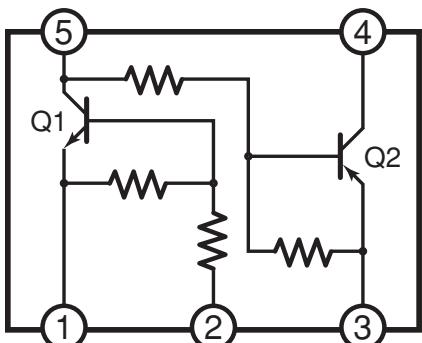
Pin No.	Pin name	Function
1.	VINFC	Focus drive input
2.	CFC err1	For connection of capacitor for the error amp filter
3.	CFC err2	For connection of capacitor for the error amp filter
4.	VINSL +	Op-amp input (+) for the sled driver
5.	VINSL -	Op-amp input (-) for the sled driver
6.	VOSL	Op-amp output for the sled driver
7.	VNFFC	Focus driver feedback pin
8.	Vcc	Vcc
9.	PV cc1	Power Vcc for sled driver block
10.	PGND	Ground for Sled Driver block
11.	VOSL -	Sled driver output (-)
12.	VOSL +	Sled driver output (+)
13.	VOFC -	Focus driver output (-)
14.	VOFC +	Focus driver output (+)
15.	VOTK +	Tracking driver output (+)
16.	VOTK -	Tracking driver output (-)
17.	VOLD +	Loading driver output (+)
18.	VOLD -	Loading driver output (-)
19.	PGND	Ground for Actuator driver block
20.	VNFTK	Tracking driver feedback pin
21.	PV cc2	Power Vcc for Actuator driver block
22.	GND	Ground
23.	VINTK	Loading driver input
24.	CTKerr2	For connection of capacitor for the error amp filter
25.	CTKerr1	For connection of capacitor for the error amp filter
26.	VINTK	Tracking driver input
27.	BLAS	Bias input
28.	STBY	Stand - By control

IC BLOCK DIAGRAM & DESCRIPTION

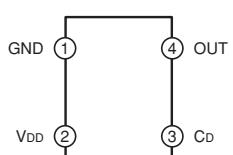
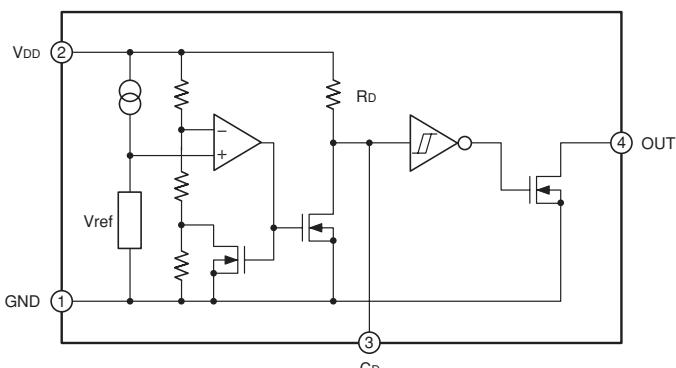
IC132 BA10358F(Dual OP. AMP.)



IC161,IC406 KRX101U(Switching and Drive)



IC171 PST3627U

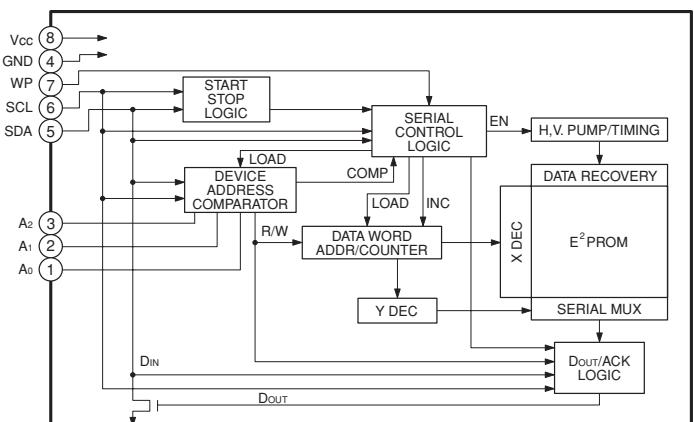


PIN No.	PIN NAME	FUNCTIONS
1	GND	GND Pin
2	Vdd	Vdd Pin / Voltage Detect Pin
3	Cd	Capacitor Connect Pin with Delay
4	OUT	Reset Signal Output Pin

IC141, IC142 M12L1616A-7TG(SDRAM)

VDD	1	Vss	50
DQ0	2	DQ15	49
DQ1	3	DQ14	48
VSSQ	4	VSSQ	47
DQ2	5	DQ13	46
DQ3	6	DQ12	45
VDDQ	7	VDDQ	44
DQ4	8	DQ11	43
DQ5	9	DQ10	42
VSSQ	10	VSSQ	41
DQ6	11	DQ9	40
DQ7	12	DQ8	39
VDDQ	13	VDDQ	38
LDQM	14	NC	37
WE#	15	UDQM	36
CAS#	16	CLK	35
PAS#	17	CKE	34
CS#	18	NC	33
A11	19	A9	32
A10	20	A8	31
A0	21	A7	30
A1	22	A6	29
A2	23	A5	28
A3	24	A4	27
VDD	25	Vss	26

IC172,IC602 AT24C02N(EEPROM)



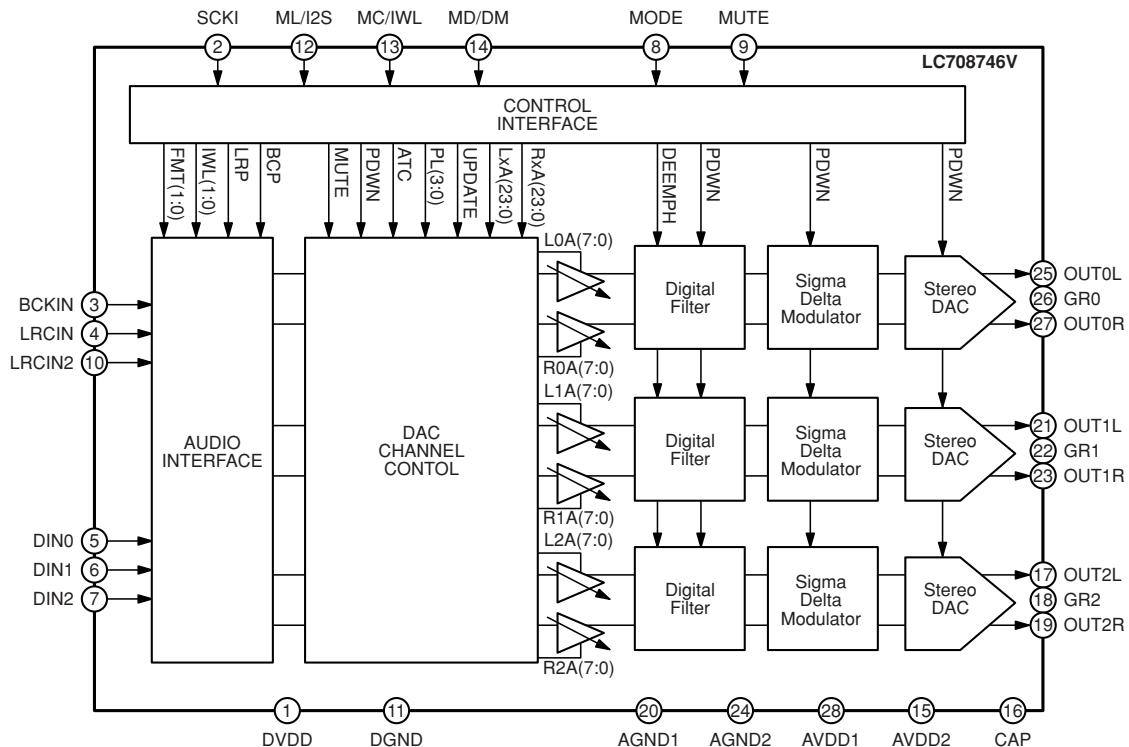
IC BLOCK DIAGRAM & DESCRIPTION

IC14, IC1421 M12L1616A-7TG(SDRAM)

Symbol	Type	Description
CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
CKE	Input	Clock Enable: CKE activates(HIGH) and deactivates(LOW) the CLK signal. If CKE goes low synchronously with clock(set-up and hold time same as other inputs), the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. When both banks are in the idle state, deactivating the clock controls the entry to the Power Down and Self Refresh modes. CKE is synchronous except after the device enters Power Down and Self Refresh modes, where CKE becomes asynchronous until exiting the same mode. The input buffers, including CLK, are disabled during Power Down and Self Refresh modes, providing low standby power.
A11	Input	Bank Select: A11(BS) defines to which bank the BankActivate, Read, Write, or BankPrecharge command is being applied.
AC-A10	Input	Address Inputs: A0-A10 are sampled during the BankActivate command (row address A0-A10 and Read/Write command (column address A0-A7 with A10 defining Auto Precharge) to select one location out of the 256K available in the respective bank. During a Precharge command, A10 is sampled to determine if both banks are to be precharged (A10-HIGT). The address inputs also provide the op-code during a Mode Register Set command.
CS#	Input	Chip Select: CS# enables (sampled LOW) and disables (sampled HIGH) the command decoder. All commands are masked when CS# is sampled HIGH. CS# provides for external bank selection on systems with multiple banks. It is considered part of the command code.
RAS#	Input	Row Address Strobe: The RAS# signal defines the operation commands in conjunction with the CAS# and WE# signals and is latched at the positive edges of CLK. When RAS# and CS# are asserted "LOW" and CAS# is asserted "HIGH," either the BankActivate command or the Precharge command is selected by the WE# signal. When the WE# is asserted "HIGH," the BankActivate command is selected and the bank designated by BS is turned on to the active state. When the WE# is asserted "LOW," the Precharge command is selected and the bank designated by BS is switched to the idle state after the precharge operation.
CAS#	Input	Column Address Strobe: The CAS# signal defines the operation commands in conjunction with the RAS# and WE# signals and is latched at the positive edges of CLK. When RAS# is held "HIGH" and CS# is asserted "LOW," the column access is started by asserting CAS#"LOW." Then, the Read or Write command is selected by asserting WE# "LOW" or "HIGH."
WE#	Input	Write Enable: The WE# signal defines the operation commands in conjunction with the RAS# and CAS# signals and is latched at the positive edges of CLK. The WE# input is used to select the BankActivate or Precharge command and Read or Write command.
LDQM, UDQM	Input	Data Input/Output Mask: LDQM and HDQM are byte specific, nonpersistent I/O buffer controls. The I/O buffers are placed in a high-z state when DQM is sampled HIGH. Input data is masked when DQM is sampled HIGH during a write cycle. Output data is masked (two-clock latency) when DQM is sampled HIGH during a read cycle. UDQM masks DQ15-DQ8, and LDQM masks DQ7-DQ0.
DQC-DQ15	Input / Output	Data I/O: The DQ0-15 input and output data are synchronized with the positive edges of CLK. The I/Os are byte-maskable during Reads and Writes.
NC	-	No Connect: These pins should be left unconnected.
VDDQ	Supply	DQ Power: Provide isolated power to DQs for improved noise immunity.(3.3V+/-0.3V)
Vssq	Supply	DQ Ground: Provide isolated ground to DQs for improved noise immunity.(0V)
VDD	Supply	Power Supply: +3.3V+/-0.3V
Vss	Supply	Ground

IC BLOCK DIAGRAM & DESCRIPTION

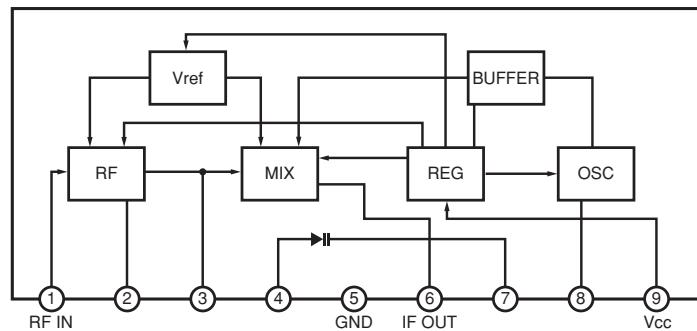
IC160 LC708746V(6ch DAC)



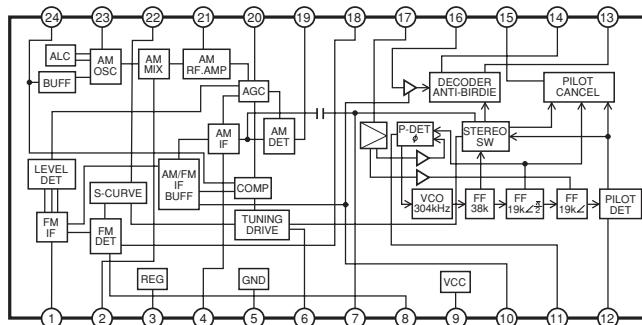
Pin No.	Name	Type	Function	
1	DVDD	Supply	Digital power source	
2	SCKI	Digital input	System clock input	
3	BCKIN	Digital input	Audio data bit clock input	
4	LRCIN	Digital input	Sampling rate clock (LRCK) input	
5	DIN0	Digital input	Channel 0 Serial audio data input	
6	DIN1	Digital input	Channel 1 Serial audio data input	
7	DIN2	Digital input	Channel 2 Serial audio data input	
8	MODE	Digital input Internal pull-up	Control mode select Low= Software mode High= Hardware mode	
9	MUTE	Digital bidirectional	Mute control (PCM mode) Input Low; Not mute High; Mute Z; Auto mute	Output (Auto mute active) Low; Mute off High; Mute on
10	LRCIN2	Digital input Internal pull-down	192kHz/96kHz Mode active 2nd LRCIN input	
11	DGND	Supply	Digital GND	
12	ML/I2S	Digital input Internal pull-up	Software mode; 3way serial control latch lag Hardware mode; Input format selector	
13	MC/IWL	Digital input Internal pull-up	Software mode; 3way serial control clock input Hardware mode; Input word length select	
14	MD/DM	Digital input	Software mode; 3way serial control data input Hardware mode; Deepnphasis select	
15	AVDD2	Supply	Analogue power source	
16	CAP	Analogue output	Analogue power VREF de-coupling	
17	OUT2L	Analogue output	Lch 2 Output	
18	GR2	Analogue input	Ch 2 GND	
19	OUT2R	Analogue output	Rch 2 Output	
20	AGND1	Supply	Analogue GND	
21	OUT1L	Analogue output	Lch 1 Output	
22	GR1	Analogue input	Ch 1 GND	
23	OUT1R	Analogue output	Rch 1 Output	
24	AGND2	Supply	Analogue GND	
25	OUT0L	Analogue output	Lch 0 Output	
26	GR0	Analogue input	Ch 0 GND	
27	OUT0R	Analogue output	Rch 0 Output	
28	AVDD1	Supply	Analogue power source	

IC BLOCK DIAGRAM & DESCRIPTION

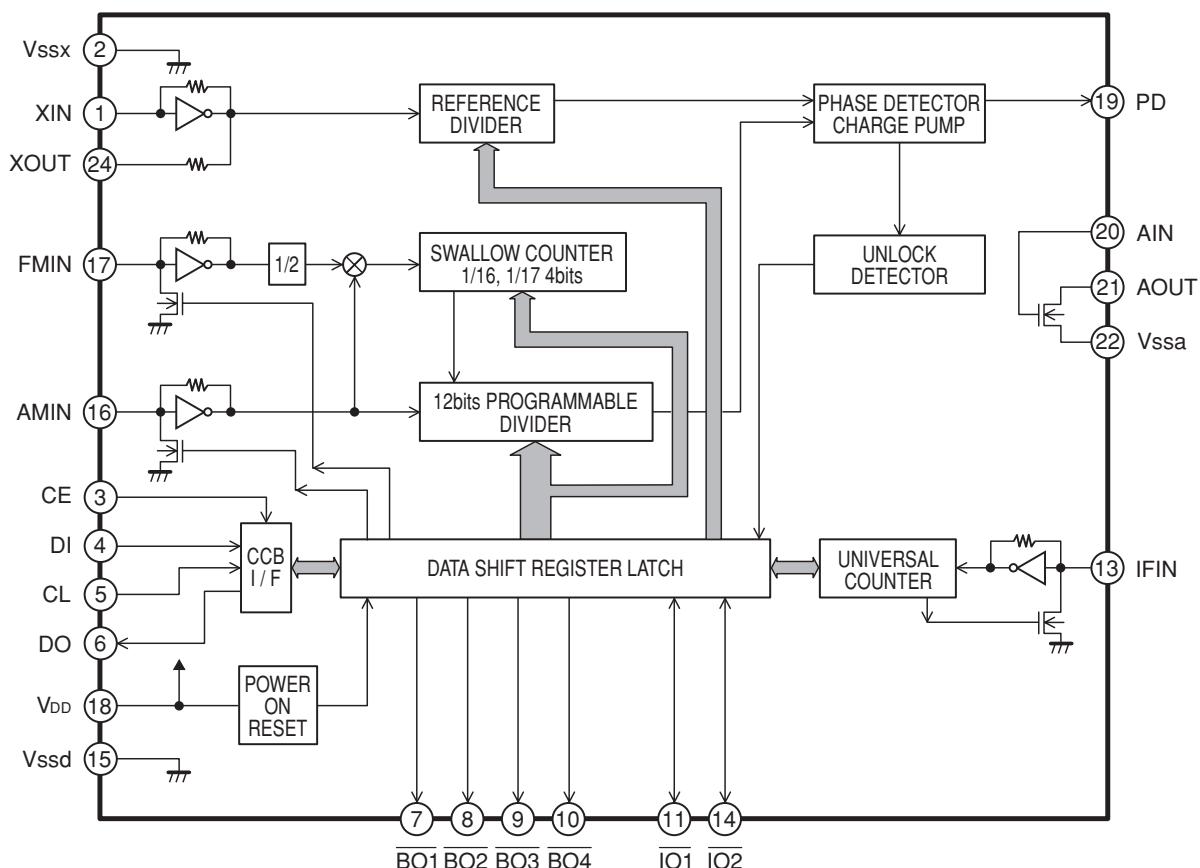
IC211 LA1186N(Diode for RM AMP,MX,OSC & AFC)



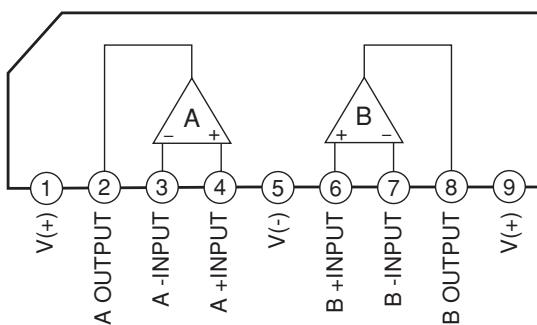
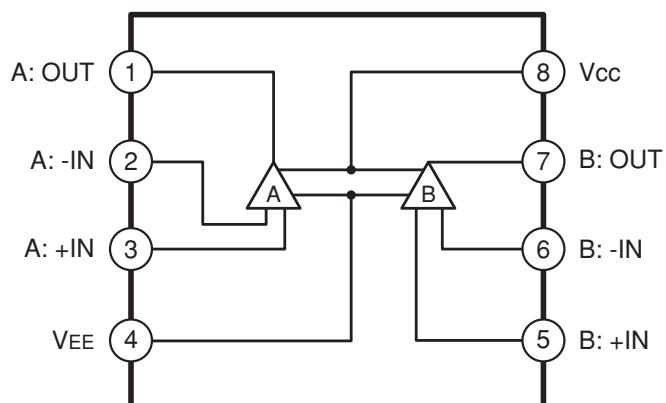
IC231 LA1844ML(AM/FM-ZF/MPX)



IC241 LC72121M-D(PLL)

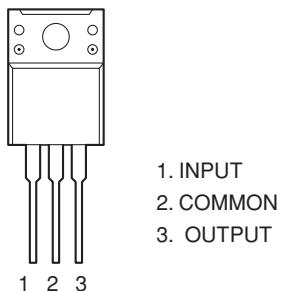


IC301 NJM4560M(OP. AMP.)

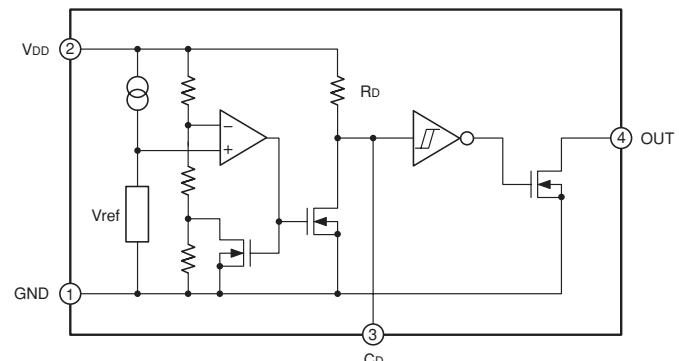


IC BLOCK DIAGRAM & DESCRIPTION

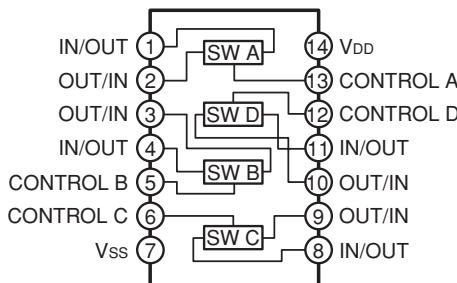
IC310 KIA7810API(Regulator)



IC321, IC491, IC603 PST3645U(System reset)

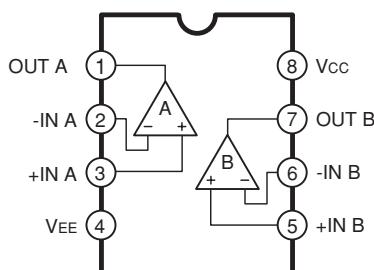


IC330 CD4066BCM(Switch)

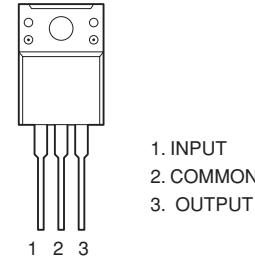


PIN No.	PIN NAME	FUNCTIONS	INTERNAL EQUIVALENT CIRCUIT
1	GND	GND Pin	Refer to BLOCK DIAGRAM
2	V _{DD}	V _{DD} Pin / Voltage Detect Pin	
3	C _d	Capacitor Connect Pin with Delay	
4	OUT	Reset Signal Output Pin	

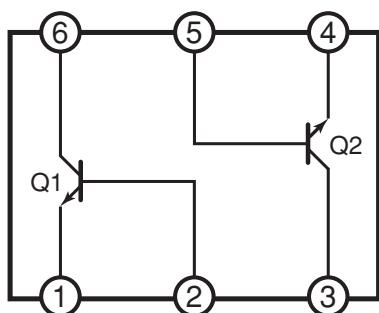
IC331, IC402, IC460 KIA4558F(OP. AMP.)



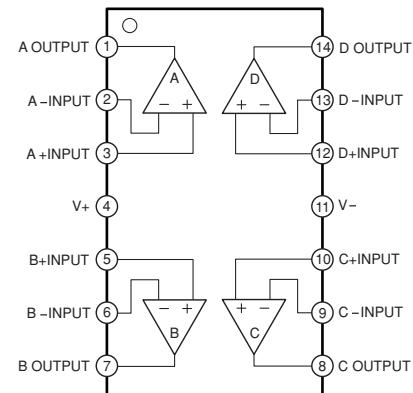
IC401, 402, IC461 KIA4558F(Regulator)



IC333 KTC801U(Switching)

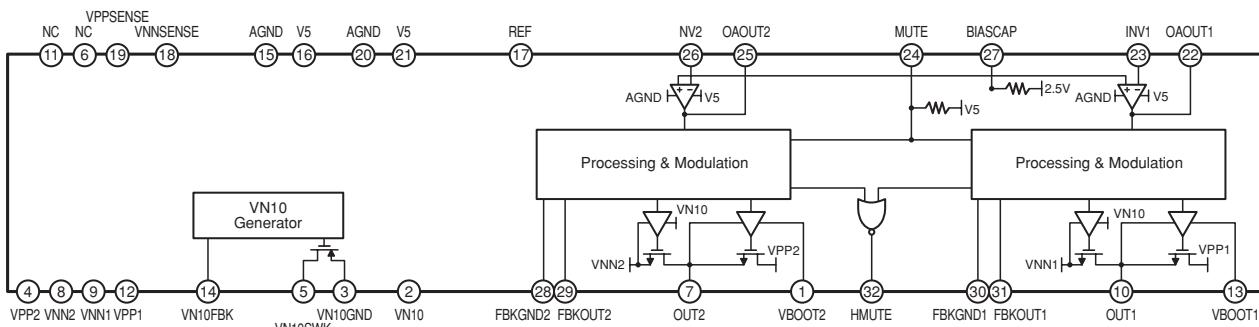


IC403, IC405 NJM2058V(OP. AMP.)



IC BLOCK DIAGRAM & DESCRIPTION

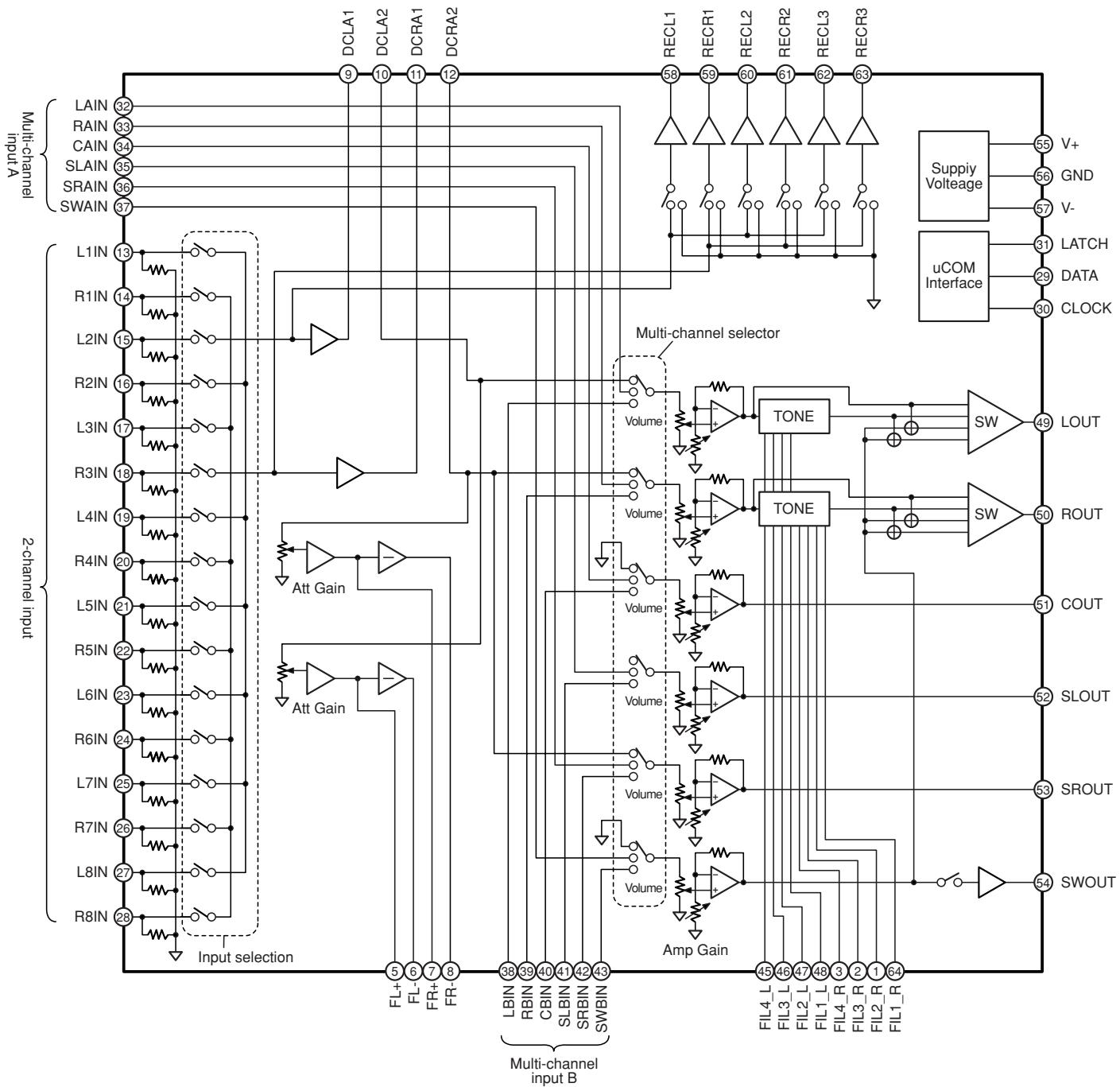
IC340, IC470, IC480 TA2022(Digital Audio Power AMP.)



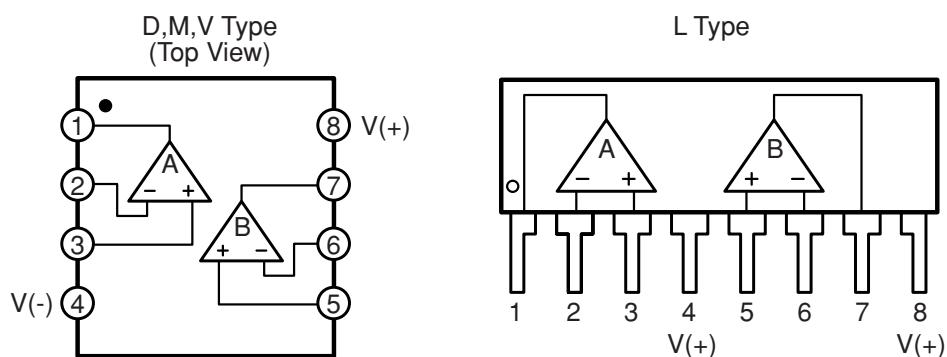
Components	Description
R _I	Inverting input resistance to provide AC gain in conjunction with R _F . This input is biased at the BIASCAP voltage (approximately 2.5VDC).
R _F	Feedback resistor to set AC gain in conjunction with R _I . Please refer to the Amplifier Gain paragraph, in the Application Information section.
C _I	Ac Input coupling capacitor which, in conjunction with R _I , form a high pass filter at $f_c = 1/(2\pi R_I C_I)$.
R _{FBA}	Feedback divider resistor connected to V ₅ . This resistor is normally set at 1kΩ .
R _{FBB}	Feedback divider resistor connected to AGND. This value of this resistor depends on the supply voltage setting and helps set the TA2022 gain in conjunction with R _I , R _F , R _{FBA} , and R _{FBC} . Please see the Modulator Feedback Design paragraphs in the Application Information Section.
R _{FBC}	Feedback resistor connected from either the OUT1(OUT2) to FBKOUT1(FBKOUT2) or speaker ground to FBKGND1(FBKND2). The value of this resistor depends on the supply voltage setting and helps set the TA2022 gain in conjunction with R _I , R _F , R _{FBA} , and R _{FBB} . It should be noted that the resistor from OUT1(OUT2) to FBKOUT1(FBKOUT2) must have a power rating of greater than Poiss = $V_{PP}^2/(2R_{FBC})$. Please see the Modulator Feedback Design paragraphs in the Application Information Section.
C _{FB}	Feedback delay capacitor that both lowers the idle switching frequency and filters very high frequency noise from the feedback signal, which improves amplifier performance. The value of C _{FB} should be offset between channel 1 and channel 2 so that the idle switching difference is greater than 40kHz. Please refer to the Application / Test Circuit.
R _{OFA}	Potentiometer used to manually trim the DC offset on the output of the TA2022.
R _{OFB}	Resistor that limits the manual DC offset trim range and allows for more precise adjustment.
R _{REF}	Bias resistor located close to pin 17 and ground at pin 20.
C _A	BIASCAP decoupling capacitor. Should be located close to pin 27 and grounded at pin 20.
D _B	Bootstrap diode. This diode charges up the bootstrap capacitors when the output is low(at VNN) to drive the high side gate circuitry. Schottky or fast recovery diode rated at least 200mA, 90V, 50nS is recommended for the bootstrap circuitry. In addition, the bootstrap diode must be able to sustain the entire V _{PP} -V _{NN} voltage. Thus, for most applications, a 90V(or greater) diode should be used.
C _B	High frequency bootstrap capacitor, which filters the high side gate drive supply. This capacitor must be located as close to pin 13(VBOOT1) or pin 1n (VBOOT2) for reliable operation. The other side of C _B should be connected directly to the OUT1(pin 10) or OUT2(pin 7). Please refer to the Application/Test Circuit.
C _{BAUX}	Bulk bootstrap capacitor that supplements C _A during "clipping" events, which result in a reduction in the average switching frequency.
R _B	Bootstrap resistor that limits C _{BAUX} charging current during TA2022 power up (bootstrap supply charging).
C _{SW}	VN10 generator filter capacitors. The high frequency capacitor (0.1μF) must be located close to pin 2 (VN10) to maximize device performance. The value of the bulk capacitor should be sized appropriately such that the VN10 voltage does not overshoot with respect to VNN during TA2022 turn on. Tripath recommends using a value of 1000μF for the bulk capacitor.
L _{SW}	VN10 generator filter inductor. This inductor sized appropriately so that L _{SW} does not saturate. If the recommended inductor value of 100μH is not used, the VN10 may overshoot with respect to VNN during TA2022 turn on.
D _{SW}	Flywheel diode for the internal VN10 buck converter. This diode also prevents VN10SW from going more than one diode drop negative with respect to VNN. This Diode can be a Fast Recovery, Switching or Schottky, but must be rated at least 200mA, 30V, 50nS.
C _{SWFB}	VN10 generator feedback capacitor. This capacitor, in conjunction with R _{SWFB} , filters the VN10 feedback signal such that the loop is unconditionally stable.
R _{SWFB}	VN10 generator feedback resistor. This resistor sets the nominal VN10 voltage. With R _{SWFB} equal to 1kΩ , the internally VN10 voltage will typically be 11V above VNN.
C _S	Supply decoupling for the power supply pins. For optimum performance, these components should be located close to the TA2022 and returned to their respective ground as shown in the Application/Test Circuit.
R _{VNNSENSE}	Overvoltage and undervoltage sense resistor for the negative supply (VNN). Please refer to the Electrical Characteristics Section for the trip points as well as the hysteresis band. Also, please refer to the Over / Under-voltage Protection section in the Application Information for a detailed discussion of the internal circuit operation and external component selection.
R _{VPPSENSE}	Overvoltage and undervoltage sense resistor for the positive supply (VPP). Please refer to the Electrical Characteristics Section for the trip points as well as the hysteresis band. Also, please refer to the Over / Under-voltage Protection section in the Application Information for a detailed discussion of the internal circuit operation and external component selection.
C _{HBR}	Supply decoupling for the high current Half-bridge supply pins. These components must be located as close to the device as possible to minimize supply overshoot and maximize device reliability. These capacitors should have good high frequency performance including low ESR and low ESL. In addition, the capacitor voltage rating must be twice the maximum V _{PP} voltage.
C _Z	Zobel capacitor, which in conjunction with R _Z , terminates the output filter at high frequencies. Use a high quality film capacitor capable of sustaining the ripple current caused by the switching outputs.
R _Z	Zobel resistor, which in conjunction with C _Z , terminates the output filter at high frequencies. The combination of R _Z and C _Z minimizes peaking of the output filter under both on load conditions or with real world loads, including loudspeakers which usually exhibit a rising impedance with increasing frequency. The recommended power rating is 2 watts.
D _O	Fast Recovery diodes that minimize overshoots and undershoots of the outputs with respect to power ground during switching transitions as well as output shorts to ground. For maximum effectiveness, these diodes must be located close to the output pins and returned to their respective V _{PP} and VNN. Also, they should be rated with a maximum Forward Voltage of 1V at 10A. Please see Application/Test Circuit for V _{PP} and VNN return pins.
L _O	Output inductor, which in conjunction with C _O , demodulates (filters) the switching waveform into an audio signal. Forms a second order filter with a cutoff frequency of $f_C = 1/(2\pi\sqrt{L_O C_O})$ and a quality factor of $Q = R_L C_O / \sqrt{L_O C_O}$. These inductors must be rated at least 10A with high linearity. Please see Output Filter Design section for details.
C _O	Output capacitor, which, in conjunction with L _O , demodulates (filters) the switching waveform into an audio signal. Forms a second order low-pass filter with a cutoff frequency of $f_C = 1/(2\pi\sqrt{L_O C_O})$ and a quality factor of $Q = R_L C_O / \sqrt{L_O C_O}$. Use a high quality film capacitor capable of sustaining the ripple current caused by the switching outputs. Electrolytic capacitors should not be used.

IC BLOCK DIAGRAM & DESCRIPTION

IC401 NJW1153FG1(6ch Electric Volume)

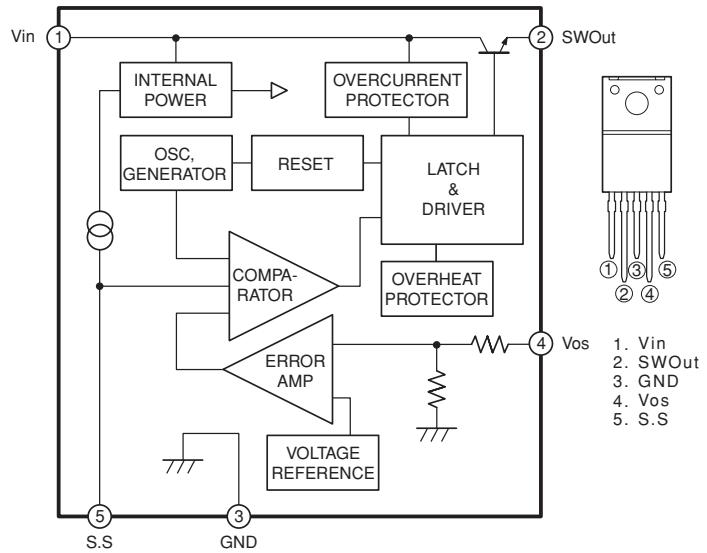


IC404 NJM4556AL(OP. AMP.)

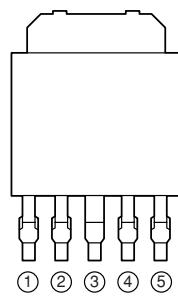


IC BLOCK DIAGRAM & DESCRIPTION

IC490 SI-8050RD(Regulator)

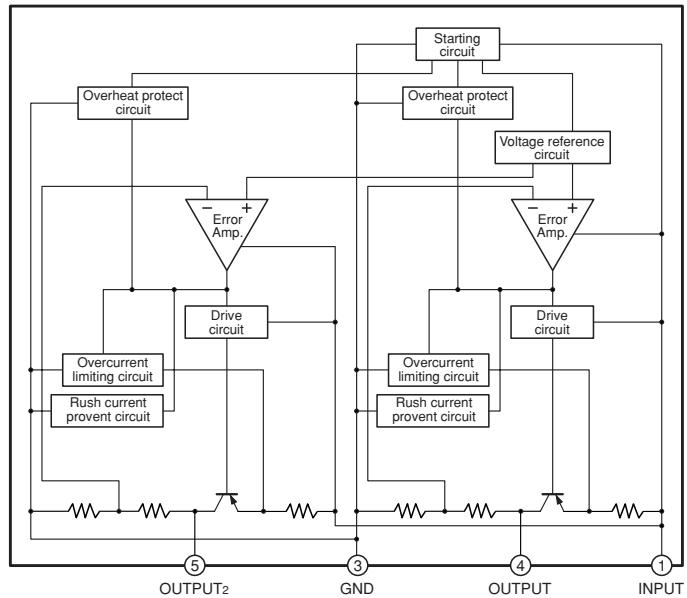


IC492, IC494 PQ050DZ01Z(Regulator)



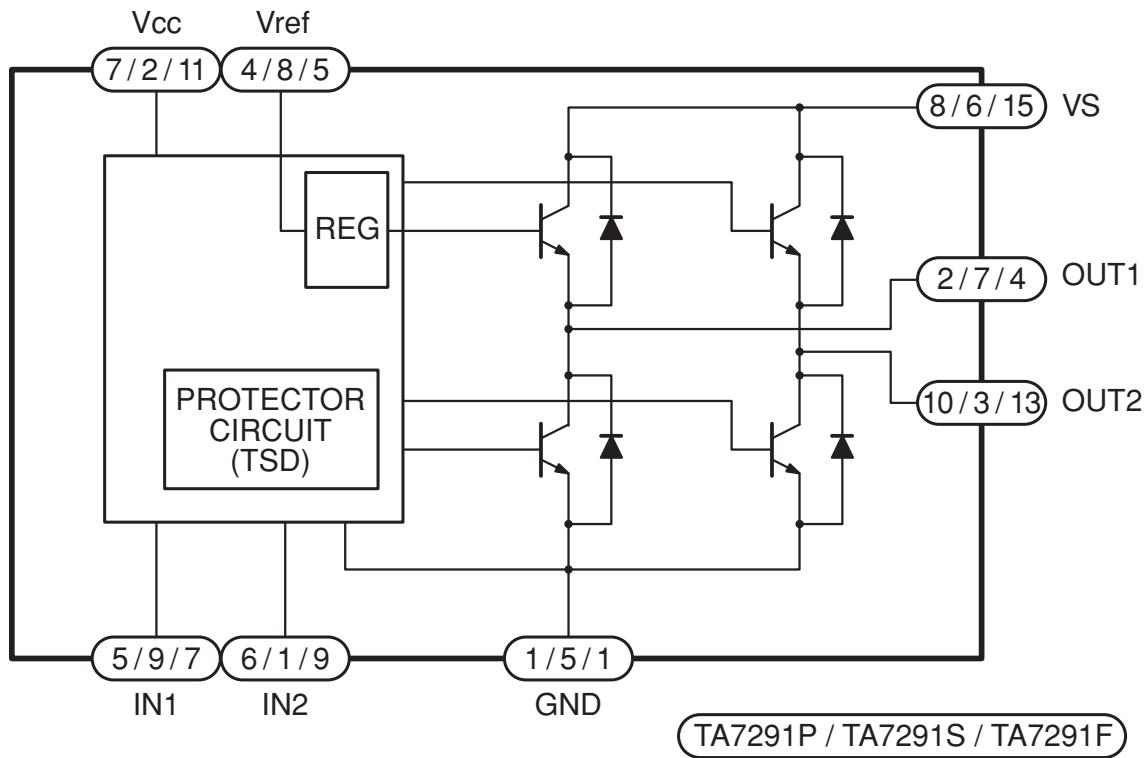
Pin No.	Symbols	Description
1	Vin	DC INPUT
2	Vc	ON/OFF CONTROL
3	Vo	DC OUTPUT
4	NC	
5	GND	

IC493 UPC37M31TJ-AZ(Regulator)



IC BLOCK DIAGRAM & DESCRIPTION

IC604 TA7291S(Driver)



PIN FUNCTION

PIN No.			SYMBOL	FUNCTIONAL DESCRIPTION
P	S	F		
7	2	11	Vcc	Supply voltage terminal for Logic
8	6	15	Vs	Supply voltage terminal for Motor driver
4	8	5	Vref	Supply voltage terminal for control
1	5	1	GND	GND terminal
5	9	7	IN1	Input terminal
6	1	9	IN2	Input terminal
2	7	4	OUT1	Output terminal
10	3	13	OUT2	Output terminal

P Type : PIN③, ⑨ : NC

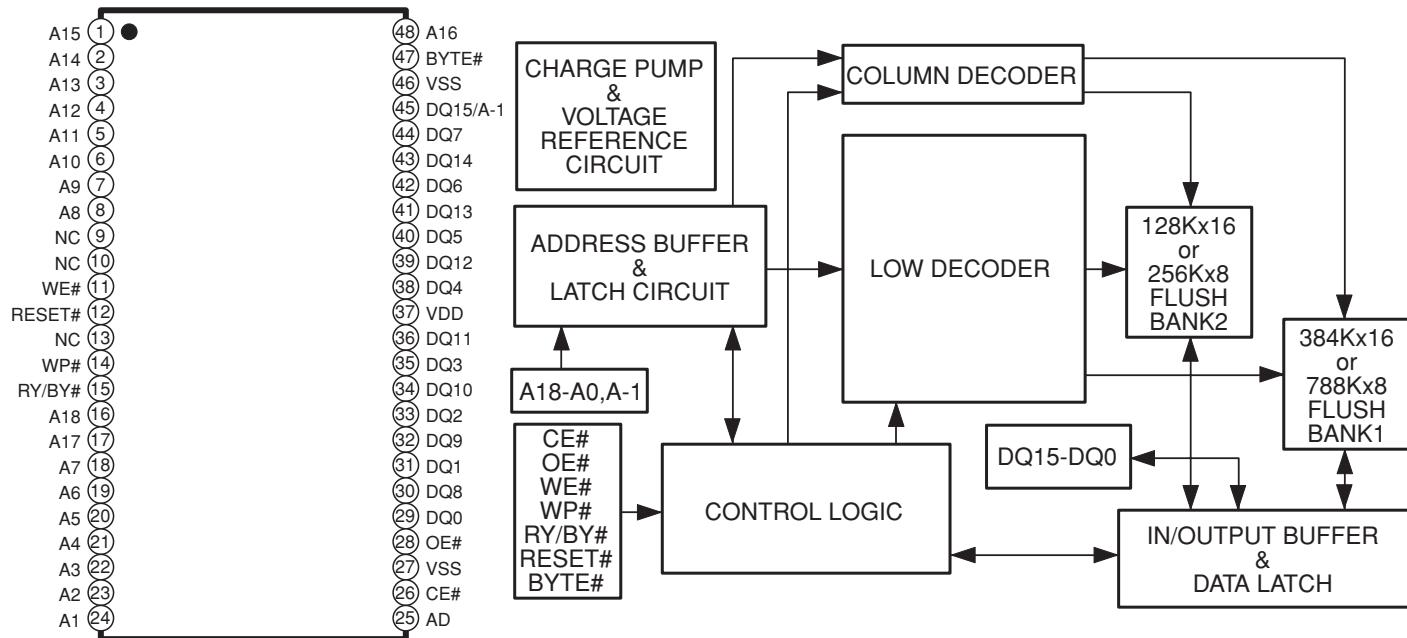
S Type : PIN④ : NC

F Type : PIN②, ③, ⑥, ⑧, ⑩, ⑫, ⑭, and ⑯ : NC

For F Type, We recommend FIN to be connected to the GND.

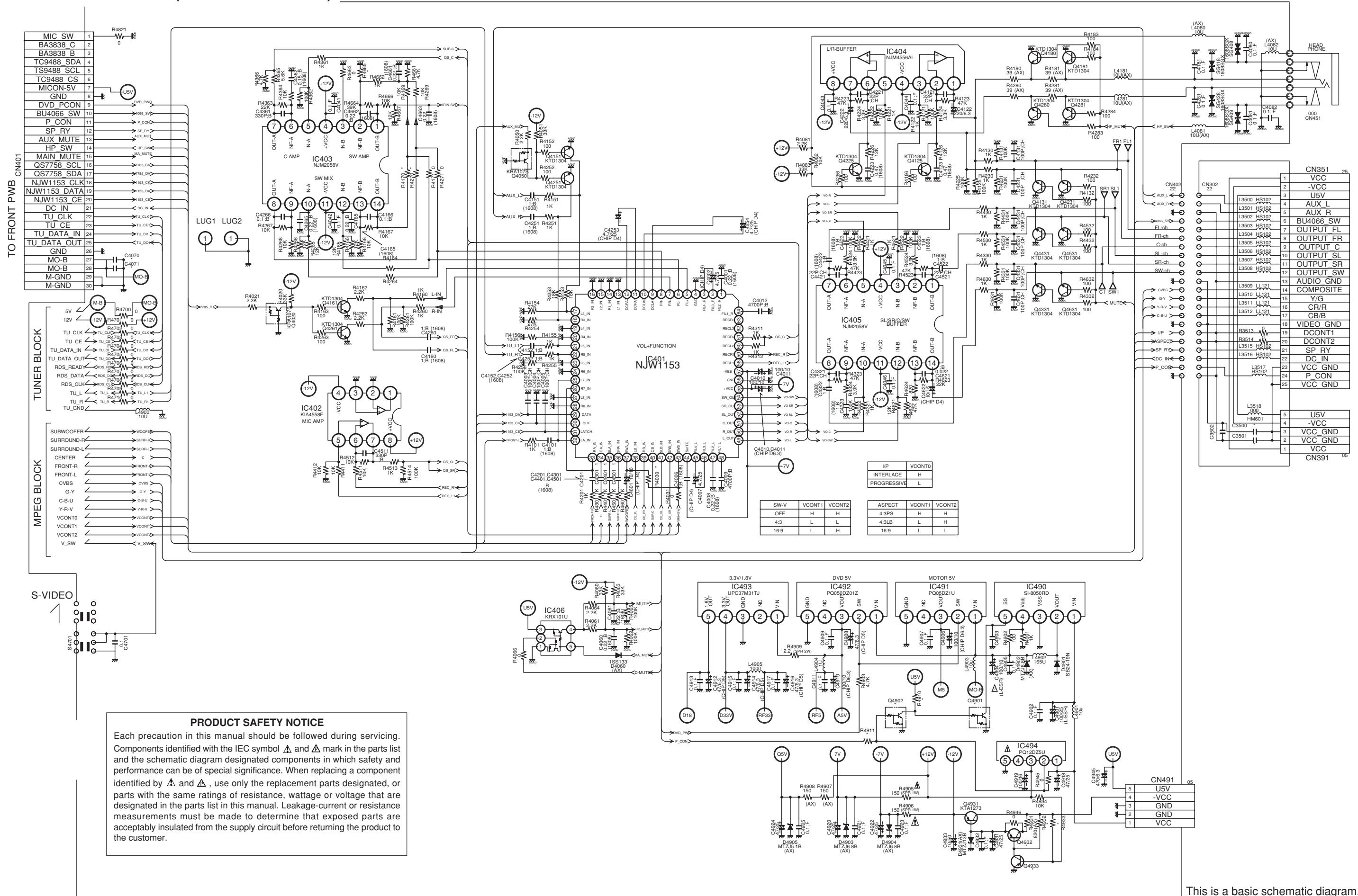
IC BLOCK DIAGRAM & DESCRIPTION

IC810 SST39VF800A(Flash)

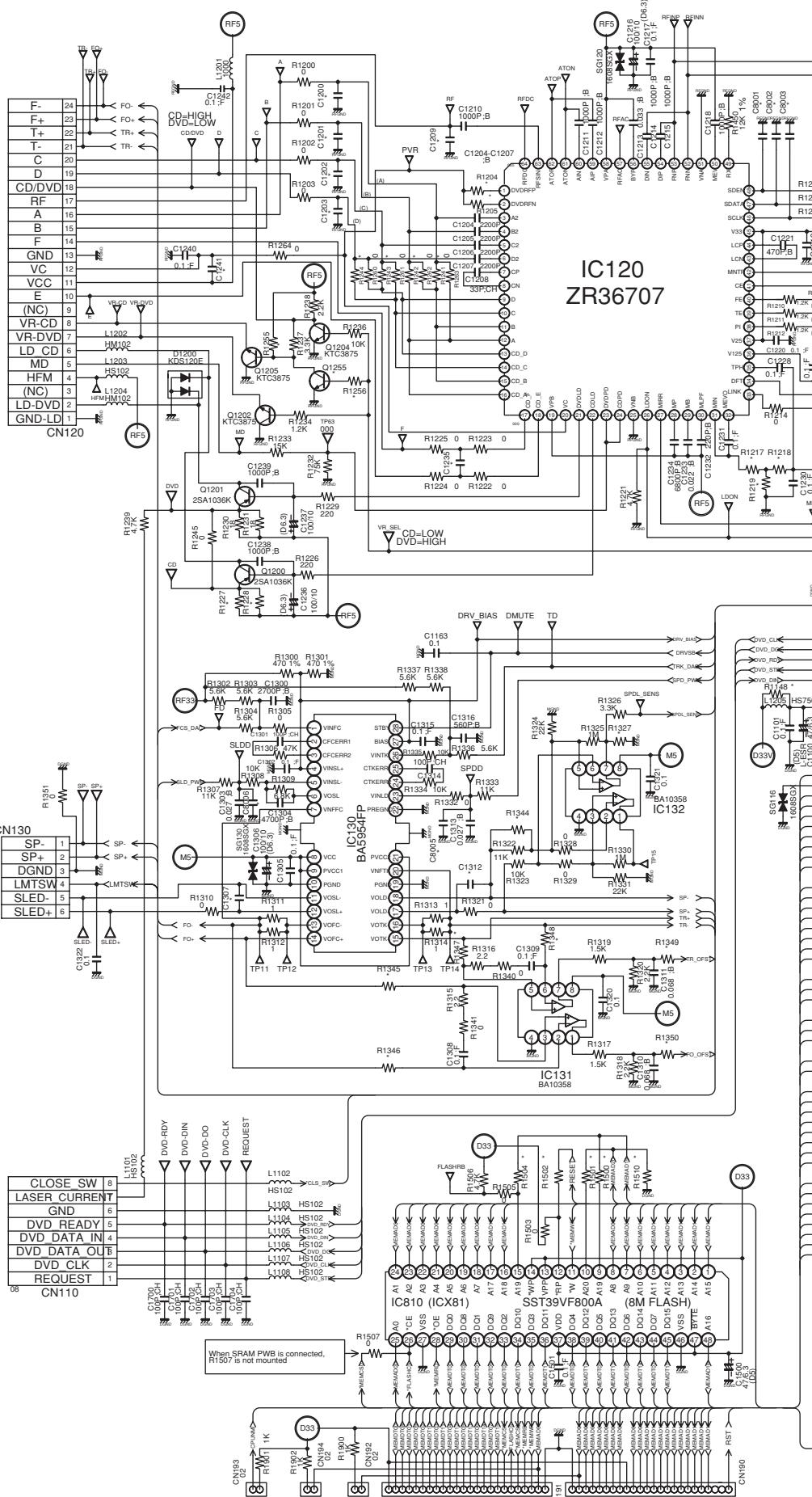


Symbols	Pin Name	Functions
A18,A17	Bank Selective Address	Selects bank 1 when "L" and bank 2.
A16-A0,A-1	Flush Bank Address	Supply address for flush bank.
A18-A15	Flush Bank Block Address	Select flush bank for erase.
A18-A10	Flush Bank Sector Sddress	Select flush bank sector for erase.
DQ15-DQ0	Data Input/Output	To output data during read cycle and receive input data during write cycles. Data is internally latched during a writecycle. The output are high impedance when OE#,CE# is "H".
CE#	Chip Enable	To activate the flush bank when CE# is "L".
OE#	Output Enable	To activate the data output buffer .
WE#	Write Enable	To control the write, erase and program.
BYTE#	Bait Pin	Bait mode when "L" and word mode when "H".
RY/BY#	Ladey/Beje Output	Output "L" when write and except "H".
WP#	Write Protect	To activate hardware write protect when "L".
RESET#	Reset	To activate hardware reset when "L".
VDD	Power Supply	2.7V~3.6V supply.
VSS	Ground	

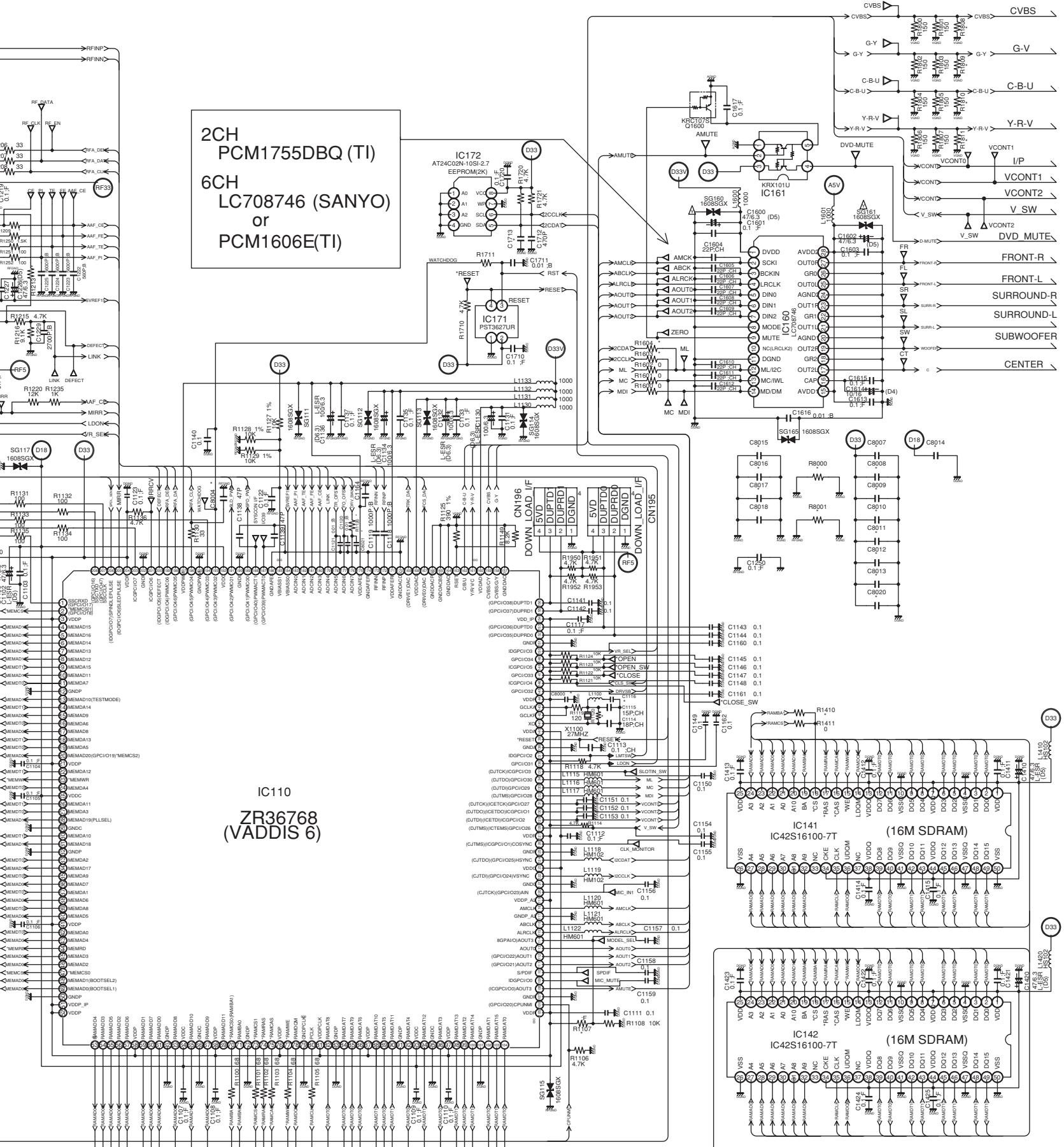
SCHEMATIC DIAGRAM (MAIN UNIT PREAMP)



SCHEMATIC DIAGRAM (MAIN UNIT DVD)

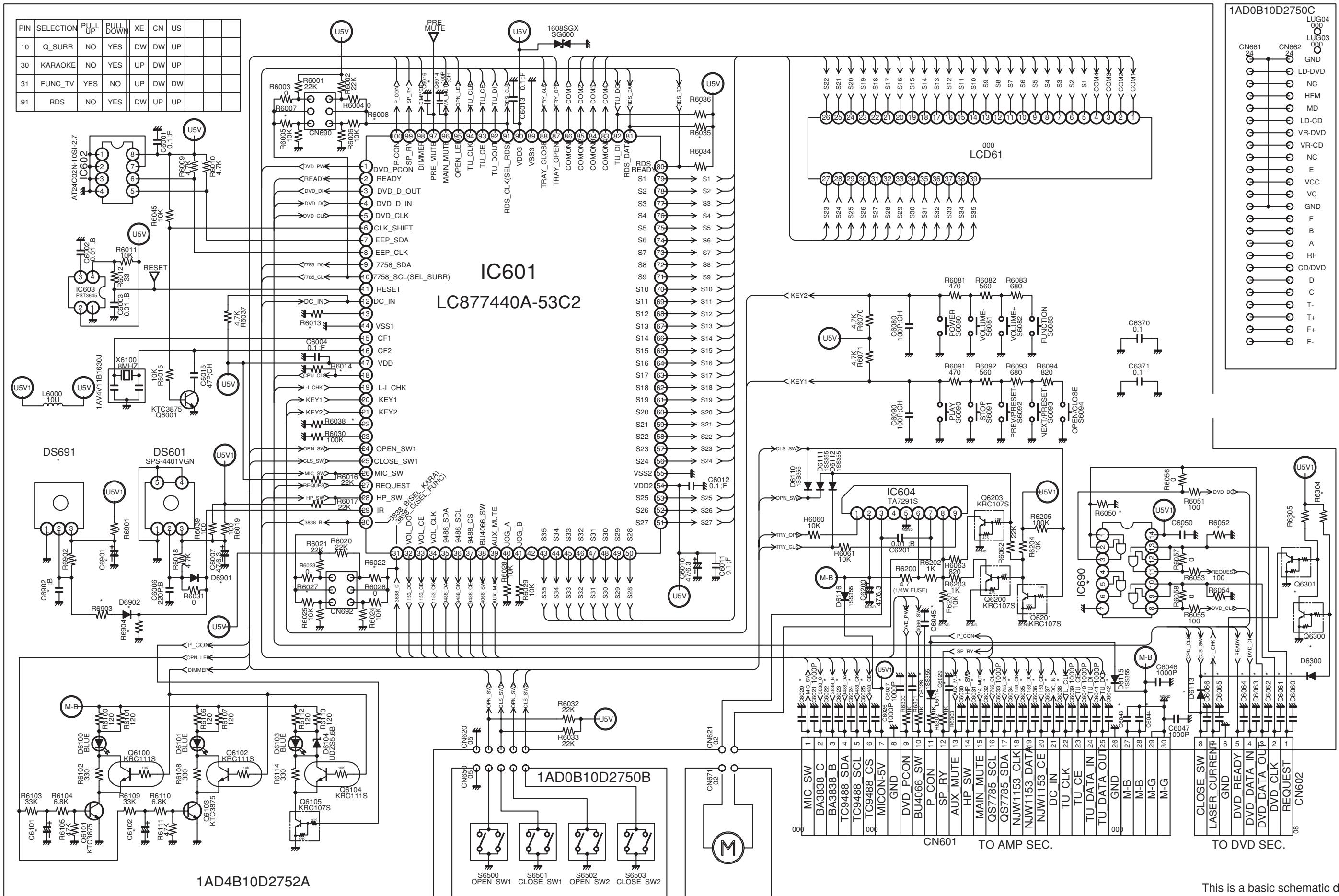


**2CH
PCM1755DBQ (TI)
6CH
LC708746 (SANYO)
or
PCM1606E(TI)**

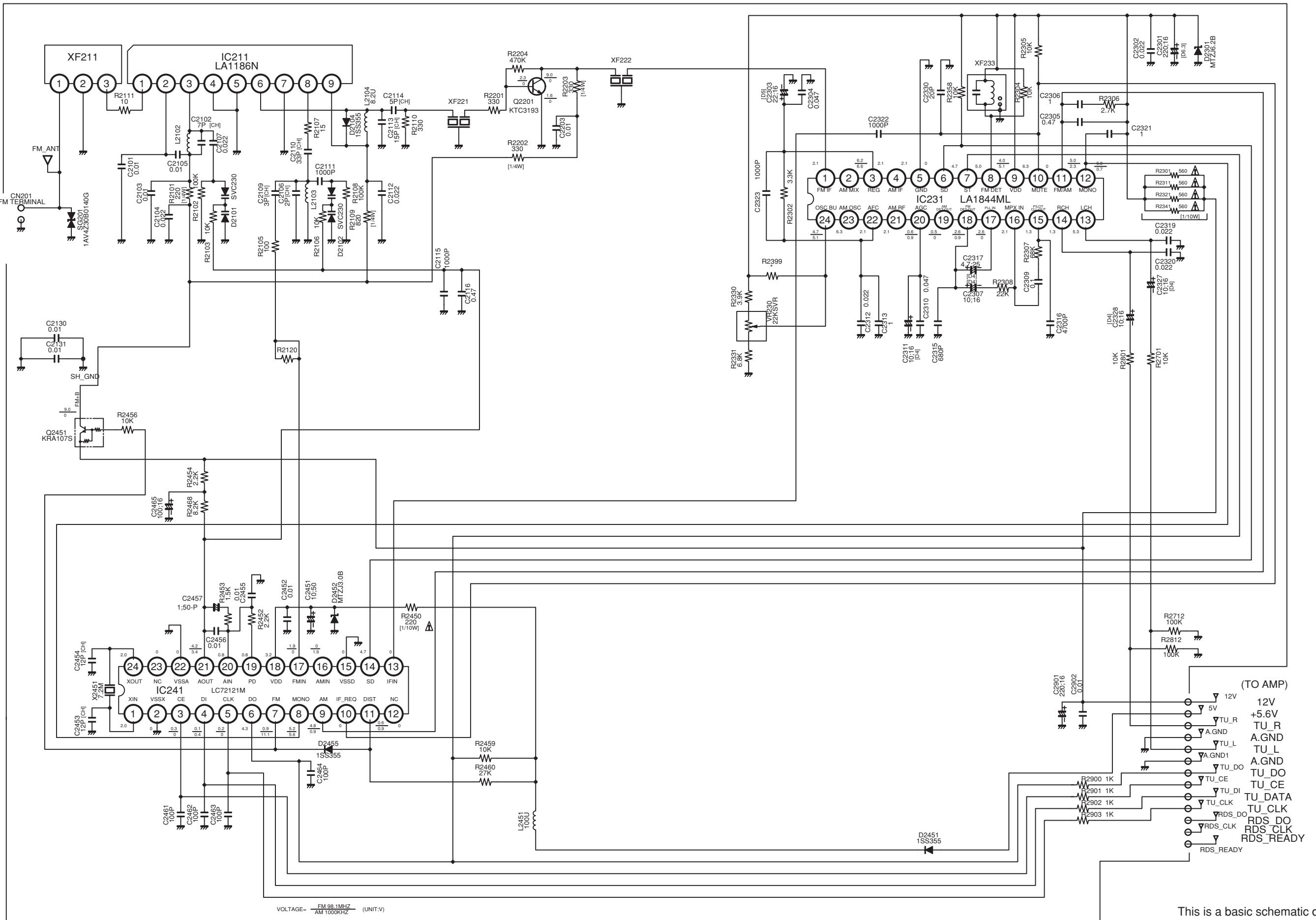


This is a basic schematic diagram.

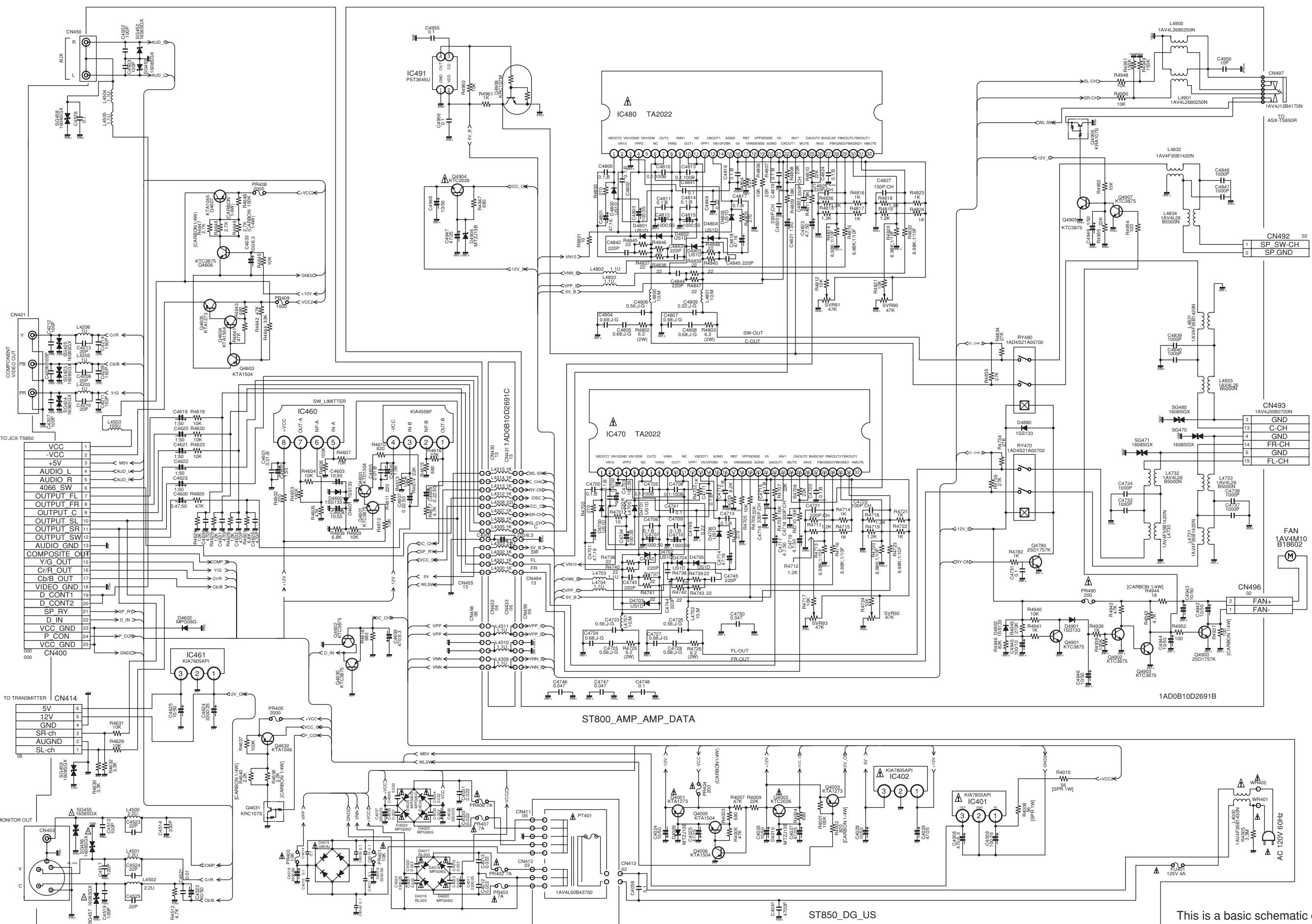
SCHEMATIC DIAGRAM (MAIN UNIT FRONT)



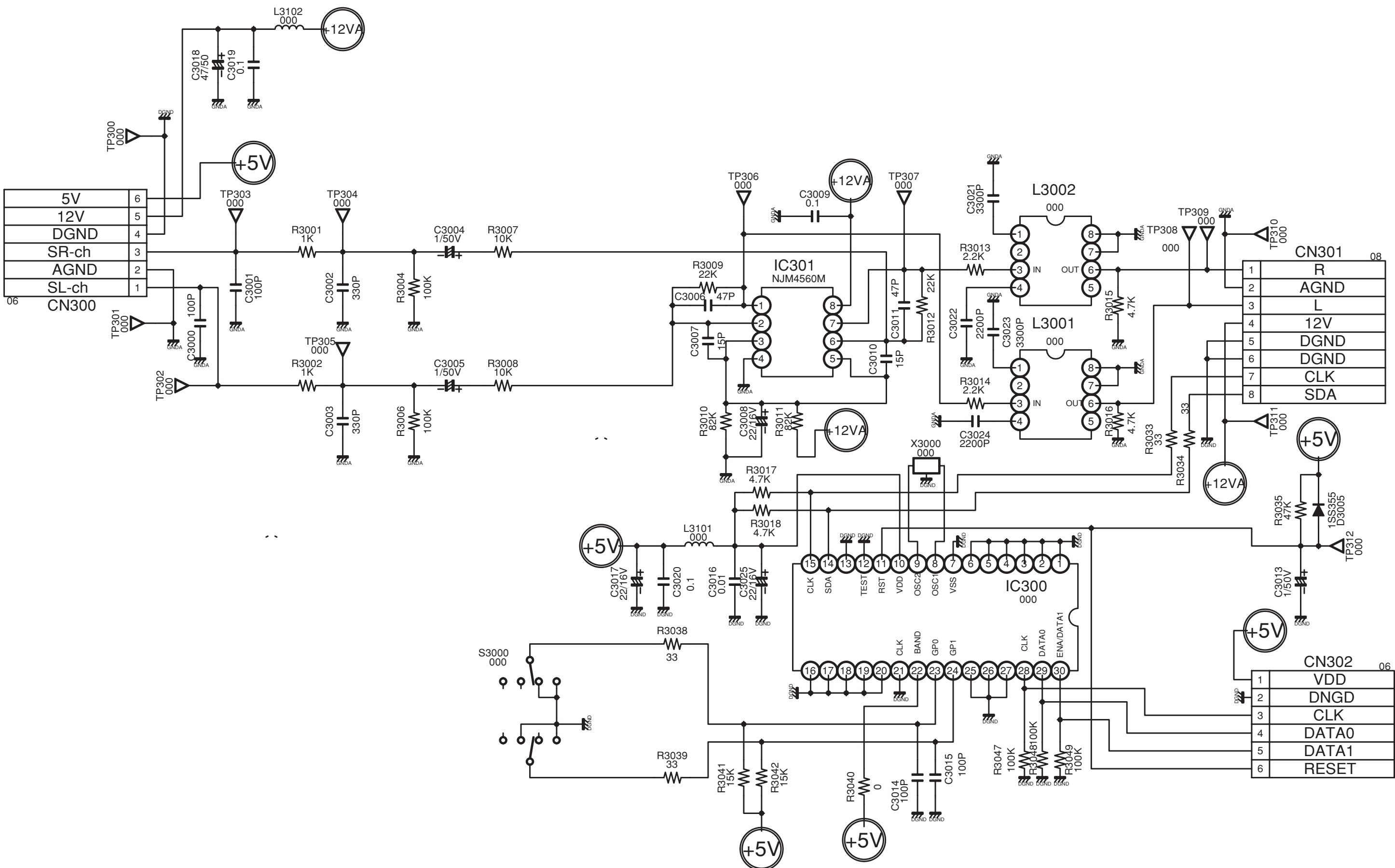
SCHEMATIC DIAGRAM (MAIN UNIT TUNER)



SCHEMATIC DIAGRAM (SUBWOOFER SPEAKER MAIN)

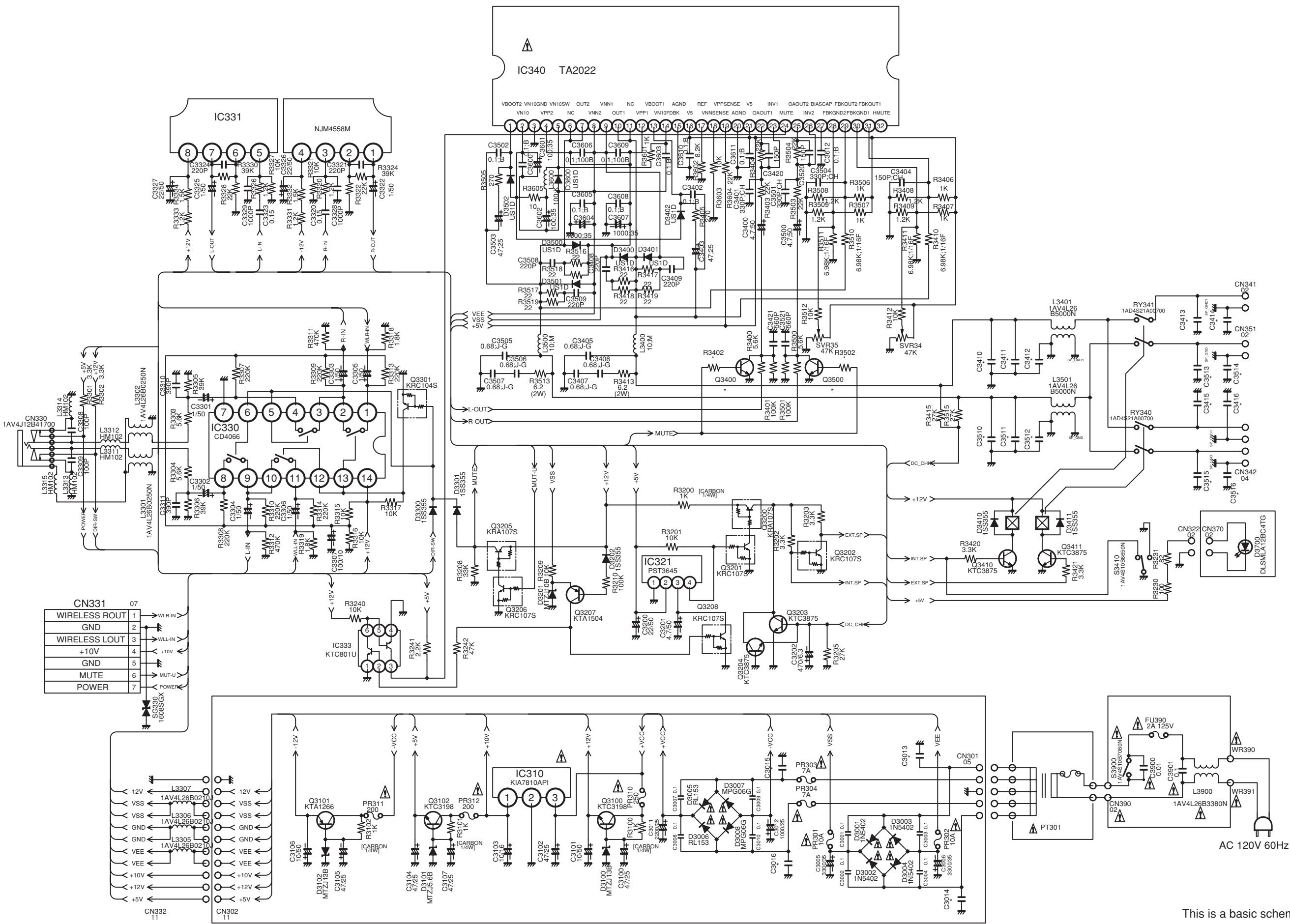


SCHEMATIC DIAGRAM (SUBWOOFER SPEAKER TX-IF)

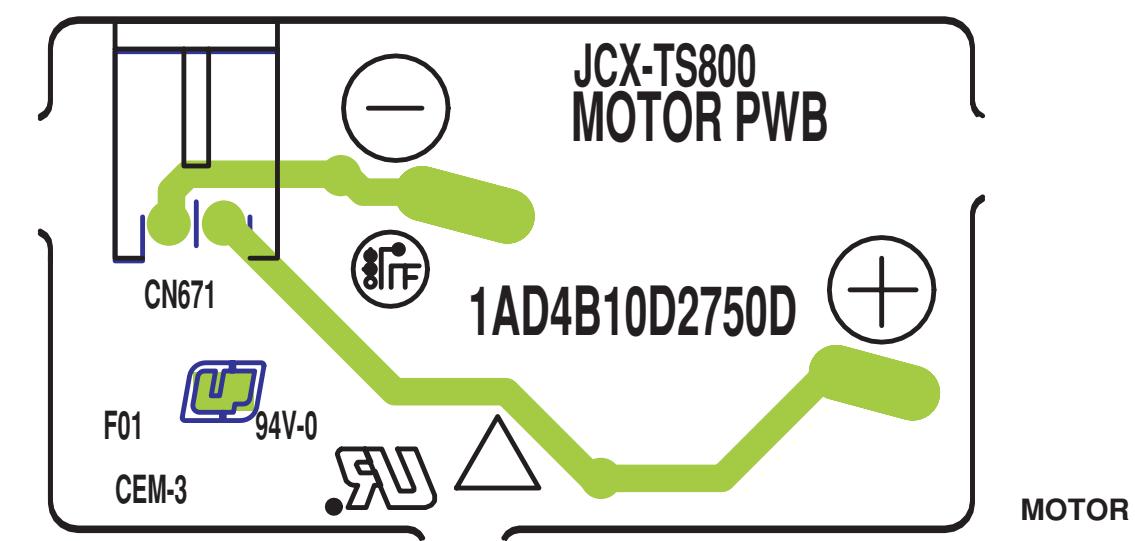
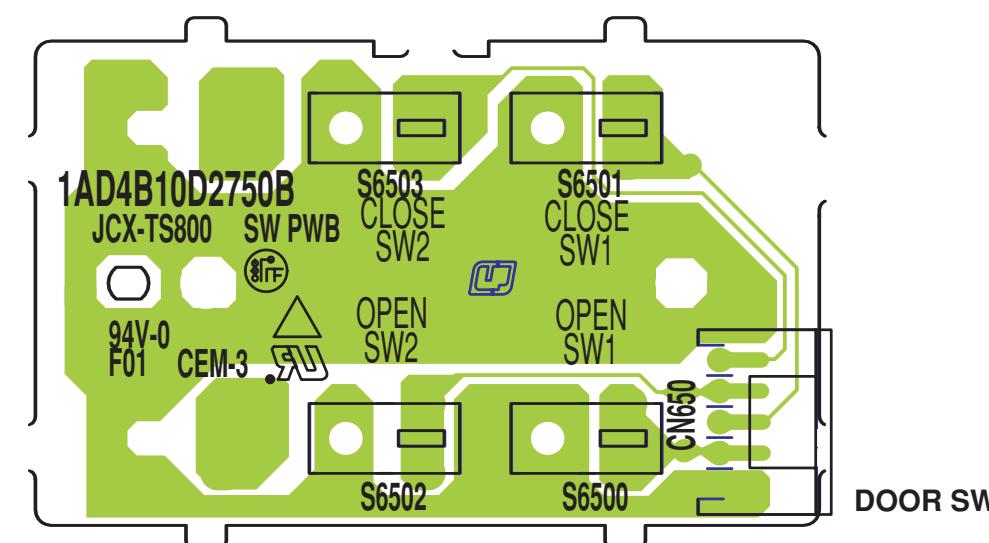
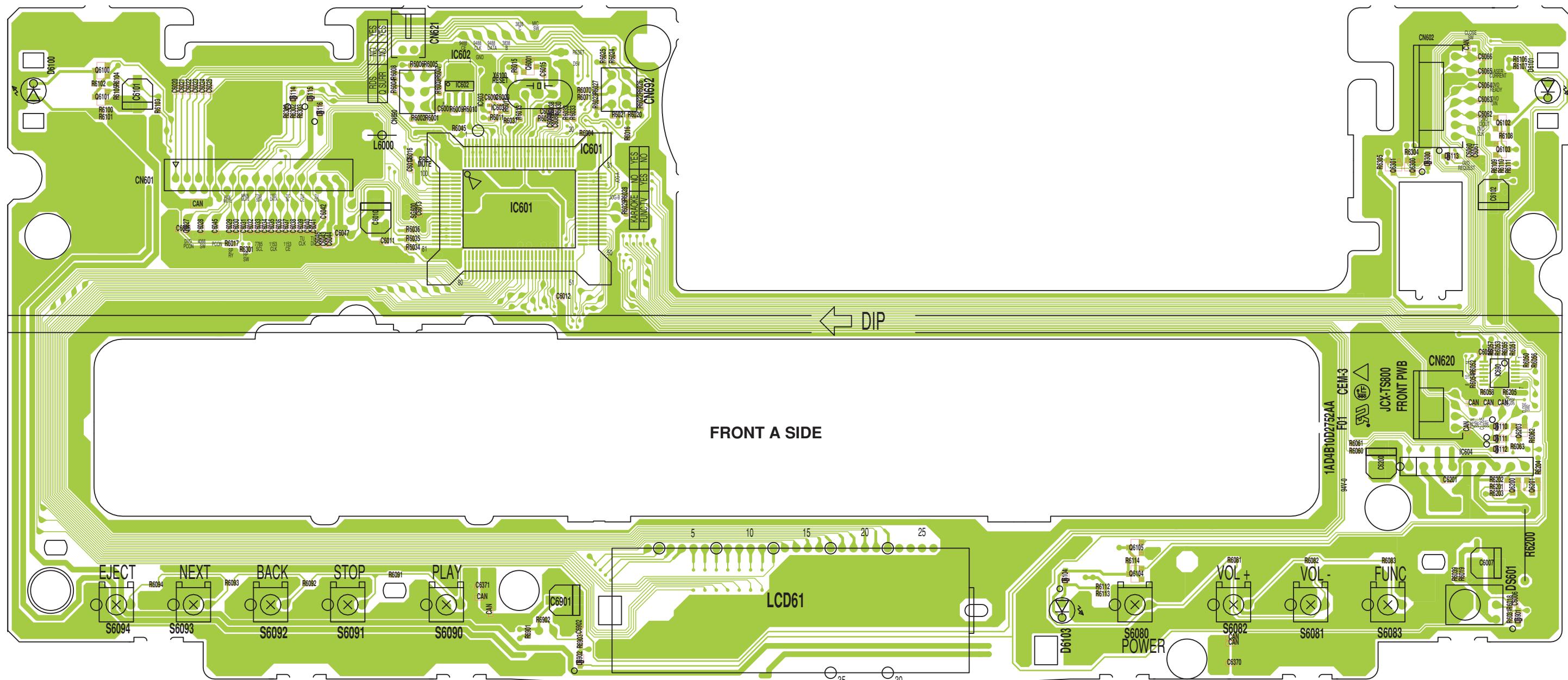


This is a basic schematic diagram.

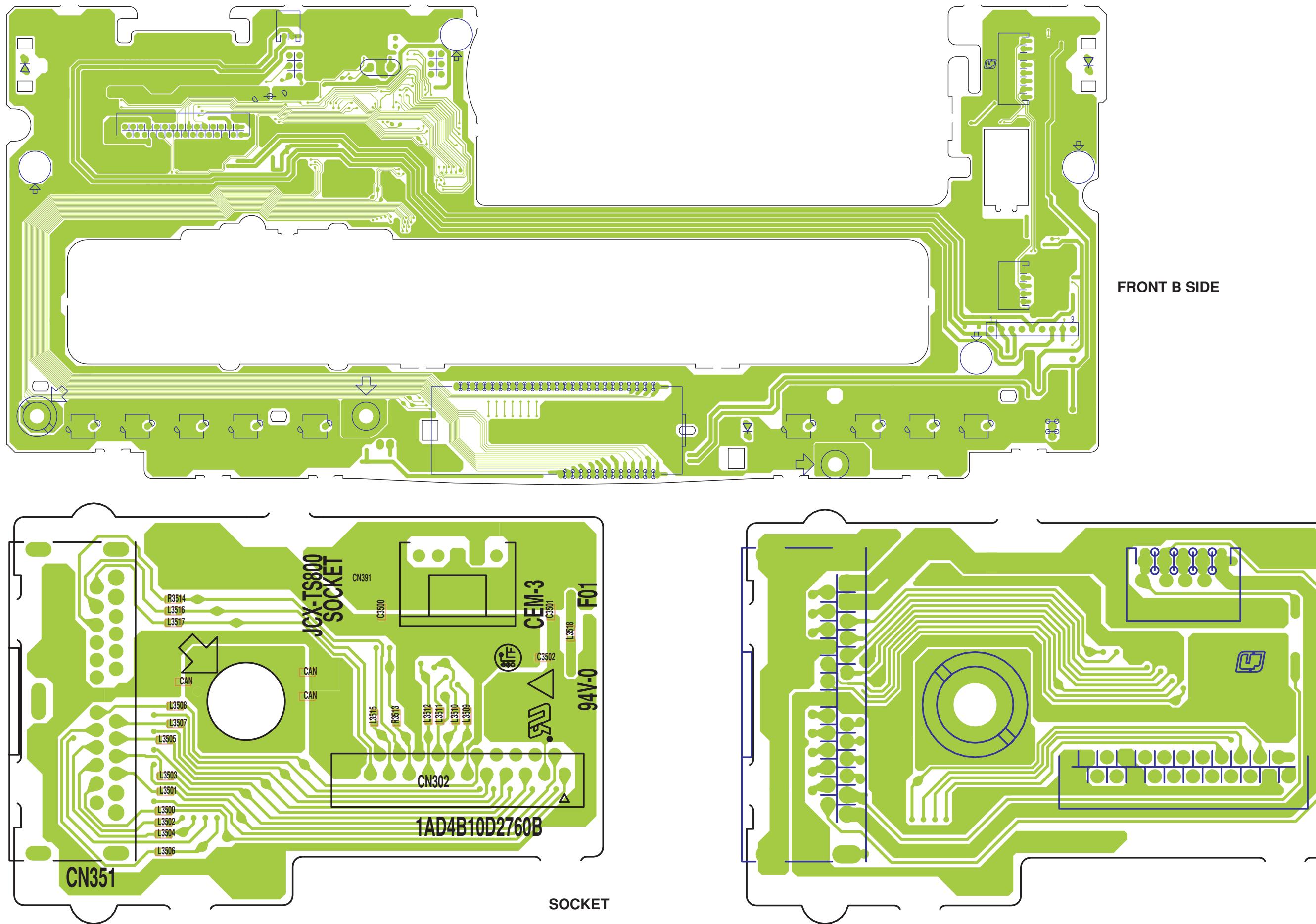
SCHEMATIC DIAGRAM (REAR SPEAKER MAIN AMP)



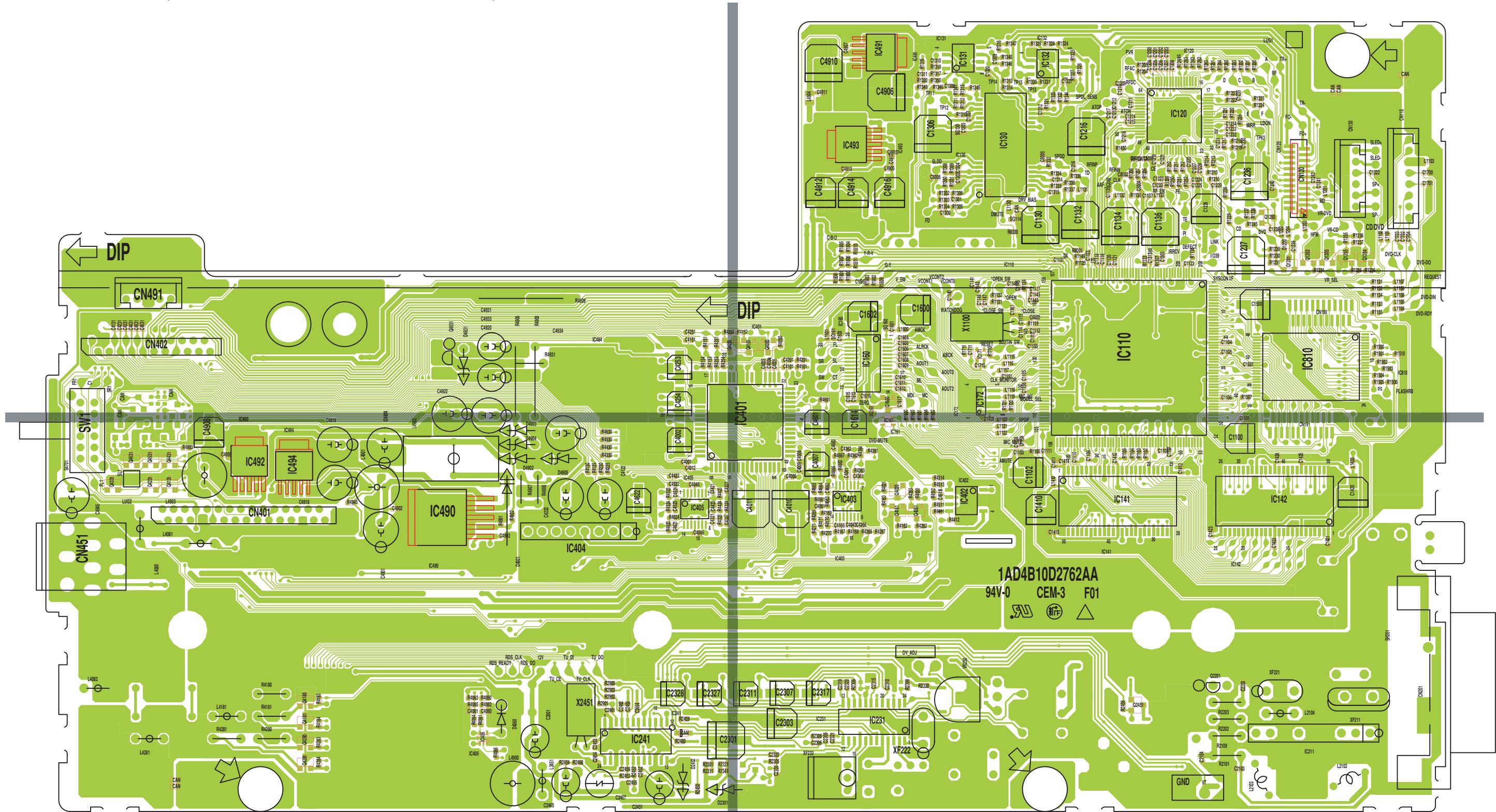
WIRING DIAGRAM (MAIN UNIT FRONT A SIDE , DOOR SW and MOTOR)



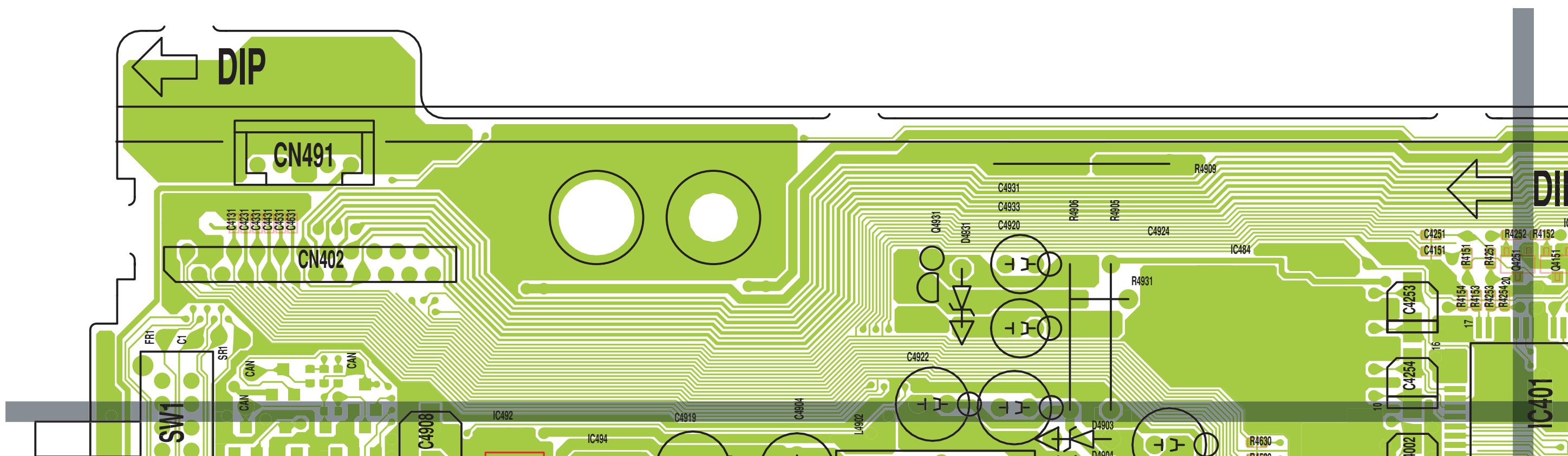
WIRING DIAGRAM (MAIN UNIT FRONT B SIDE and SOCKET)



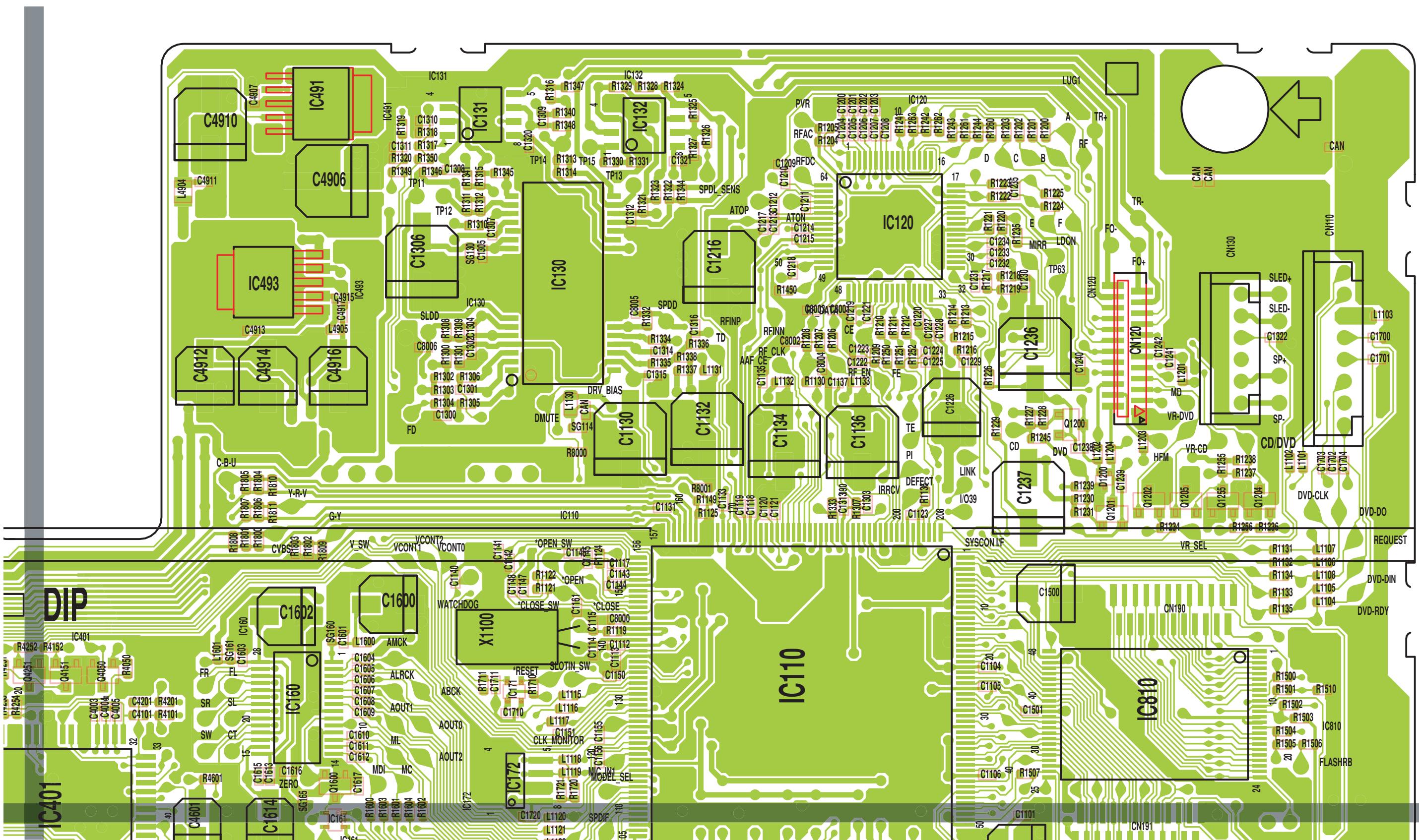
WIRING DIAGRAM (MAIN UNIT DVD/PREAMP/TUNER A SIDE)



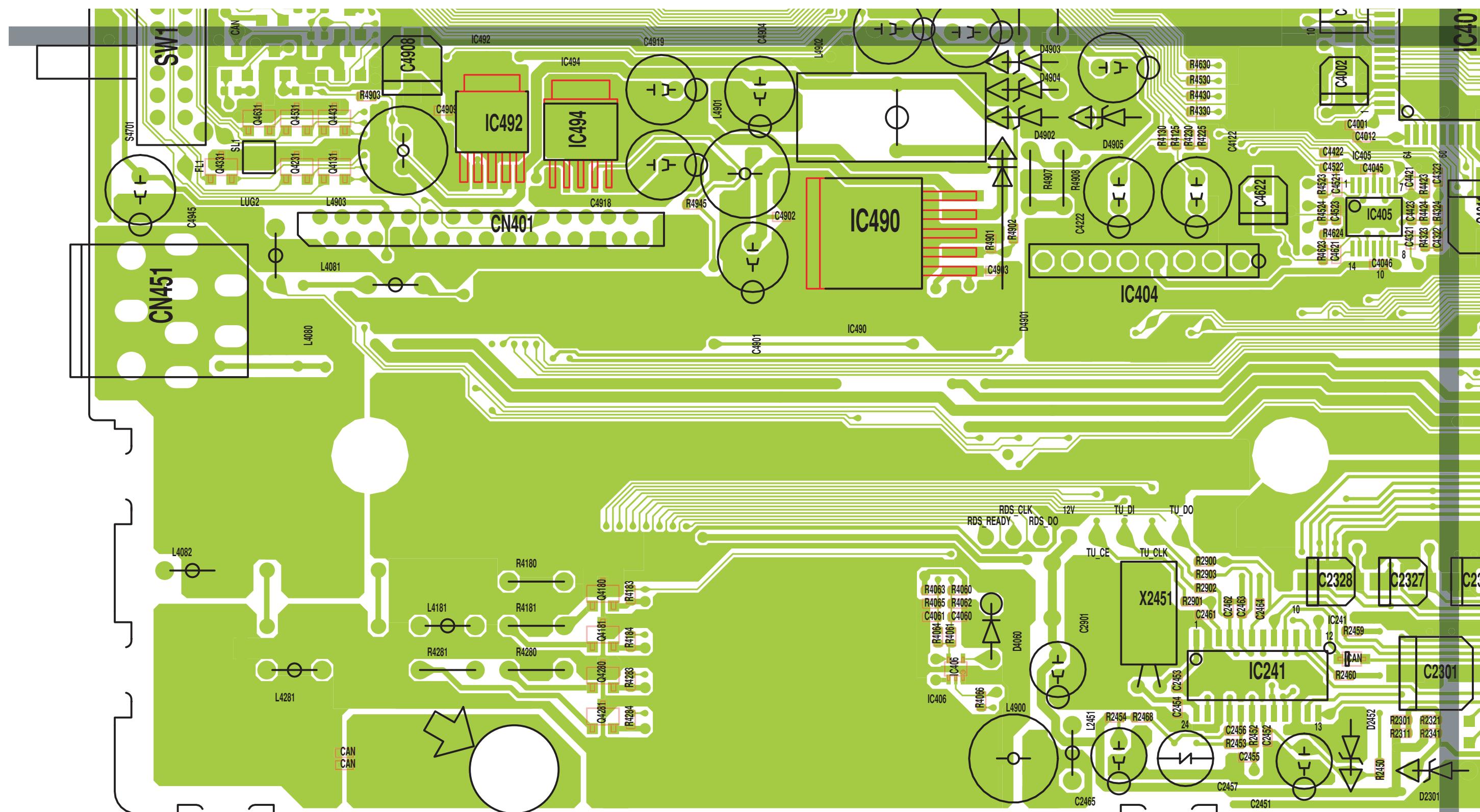
WIRING DIAGRAM (MAIN UNIT DVD/PREAMP/TUNER A SIDE)



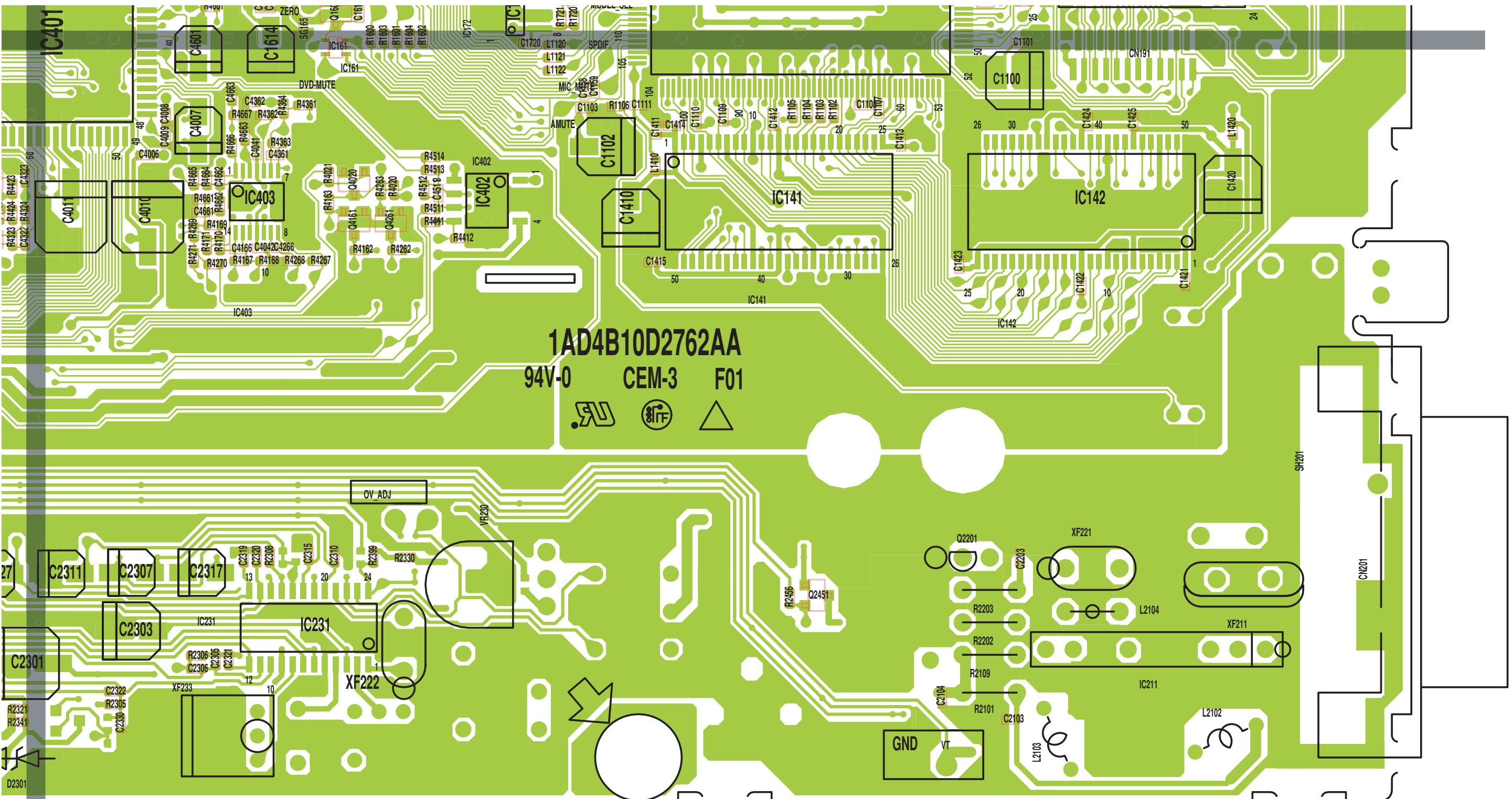
WIRING DIAGRAM (MAIN UNIT DVD/PREAMP/TUNER A SIDE)



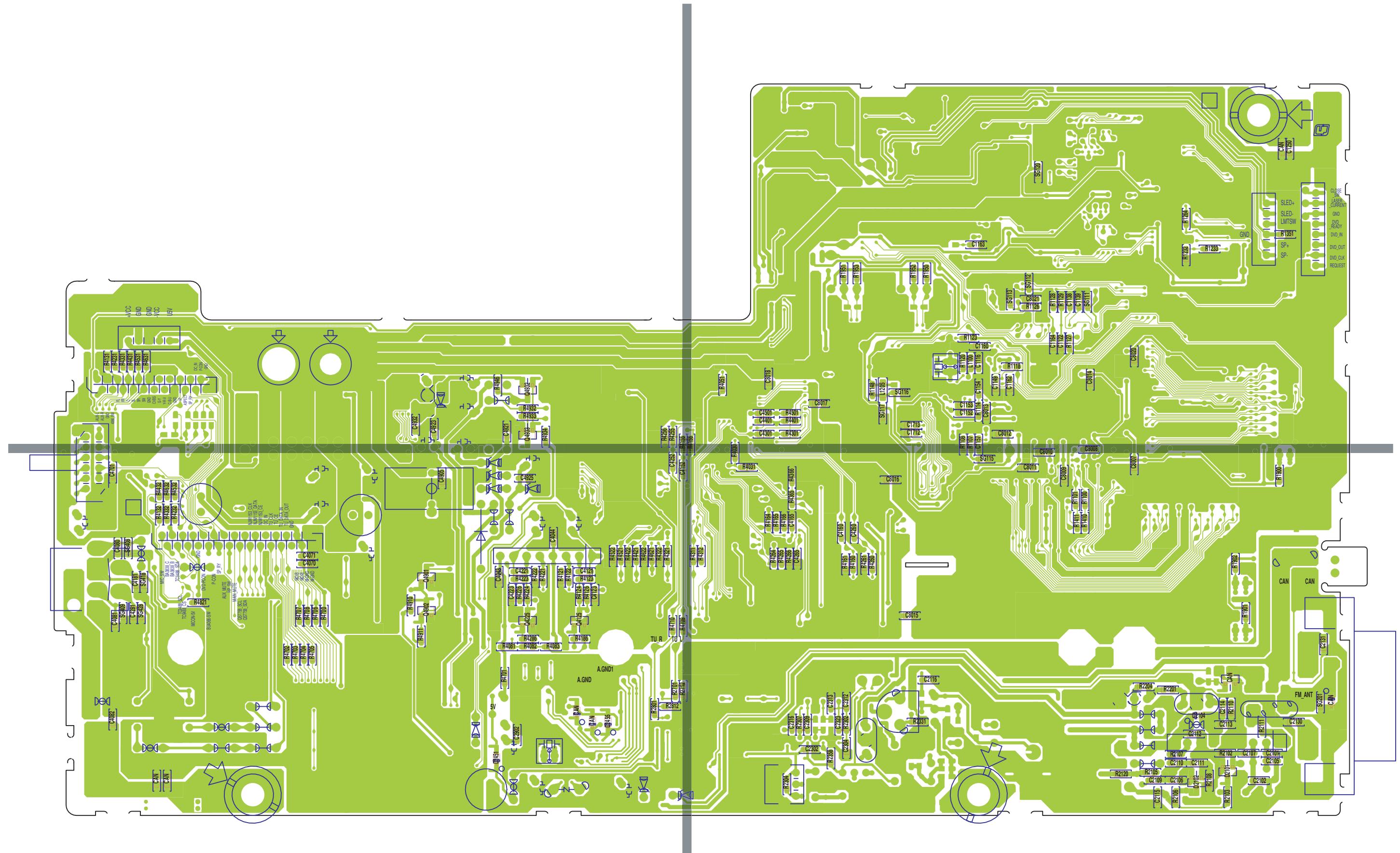
WIRING DIAGRAM (MAIN UNIT DVD/PREAMP/TUNER A SIDE)



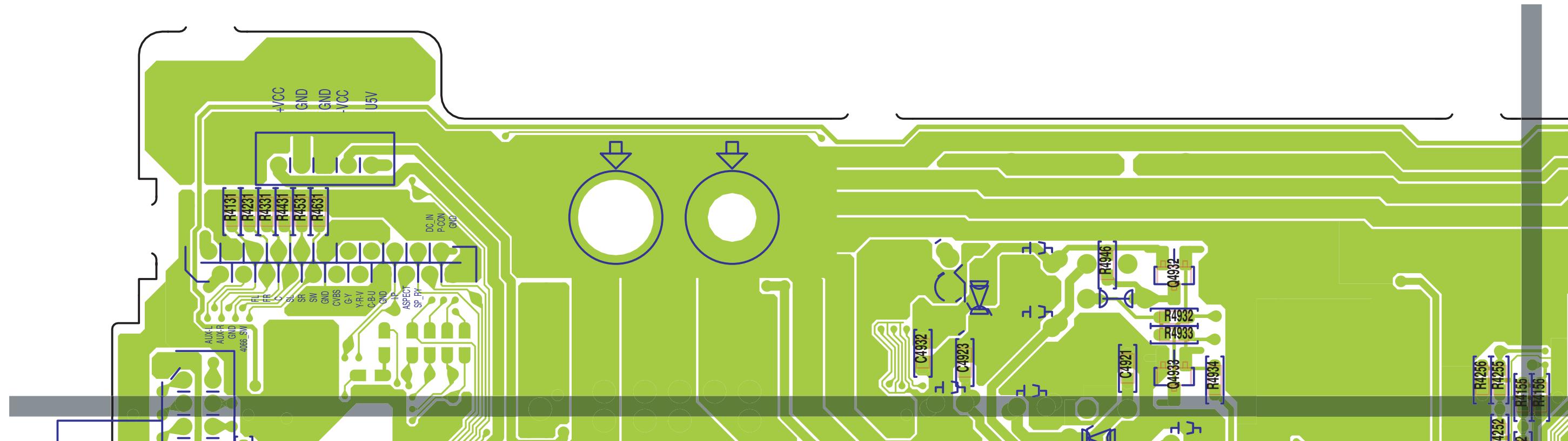
WIRING DIAGRAM (MAIN UNIT DVD/PREAMP/TUNER A SIDE)



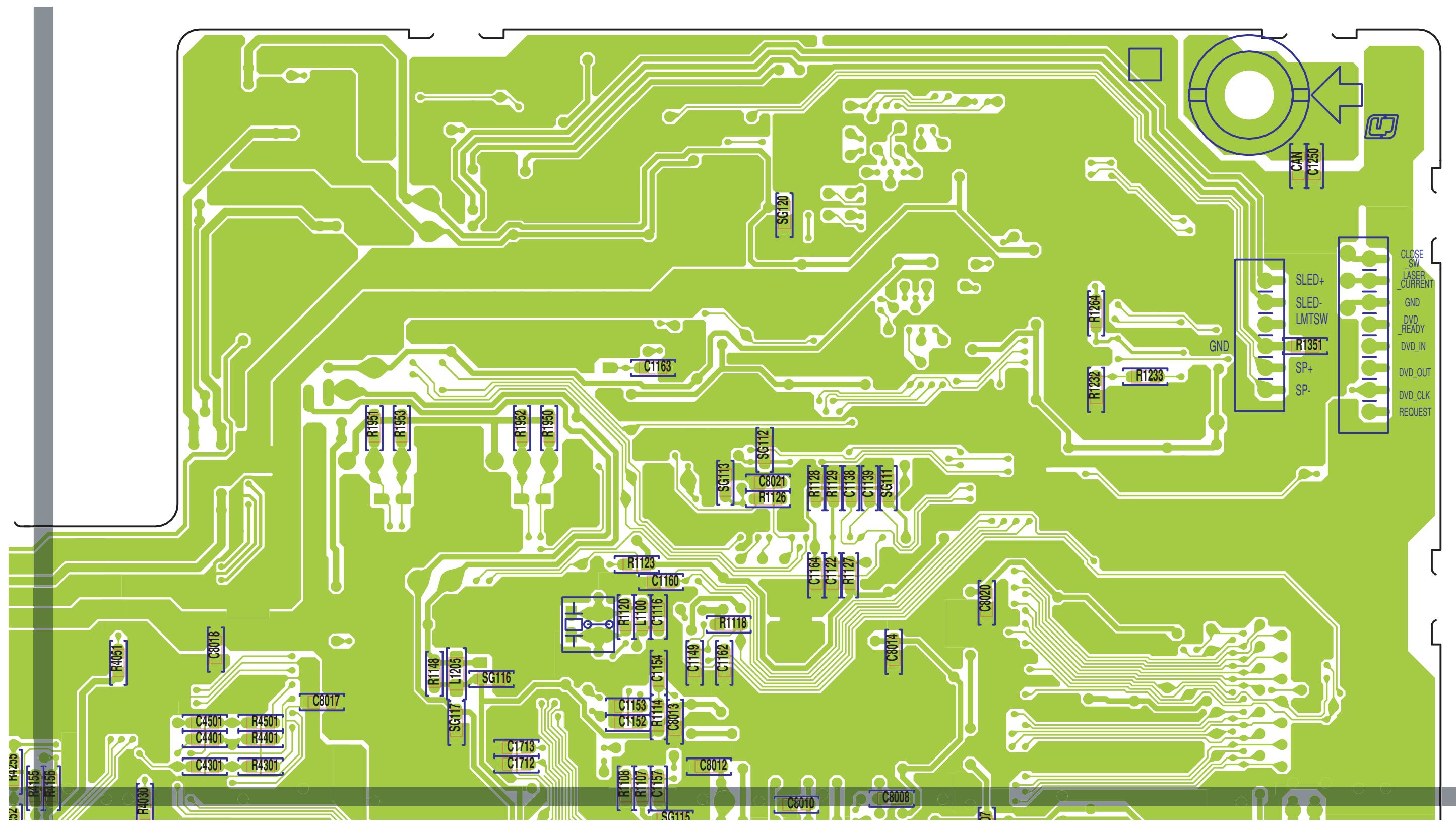
WIRING DIAGRAM (MAIN UNIT DVD/PREAMP/TUNER B SIDE)



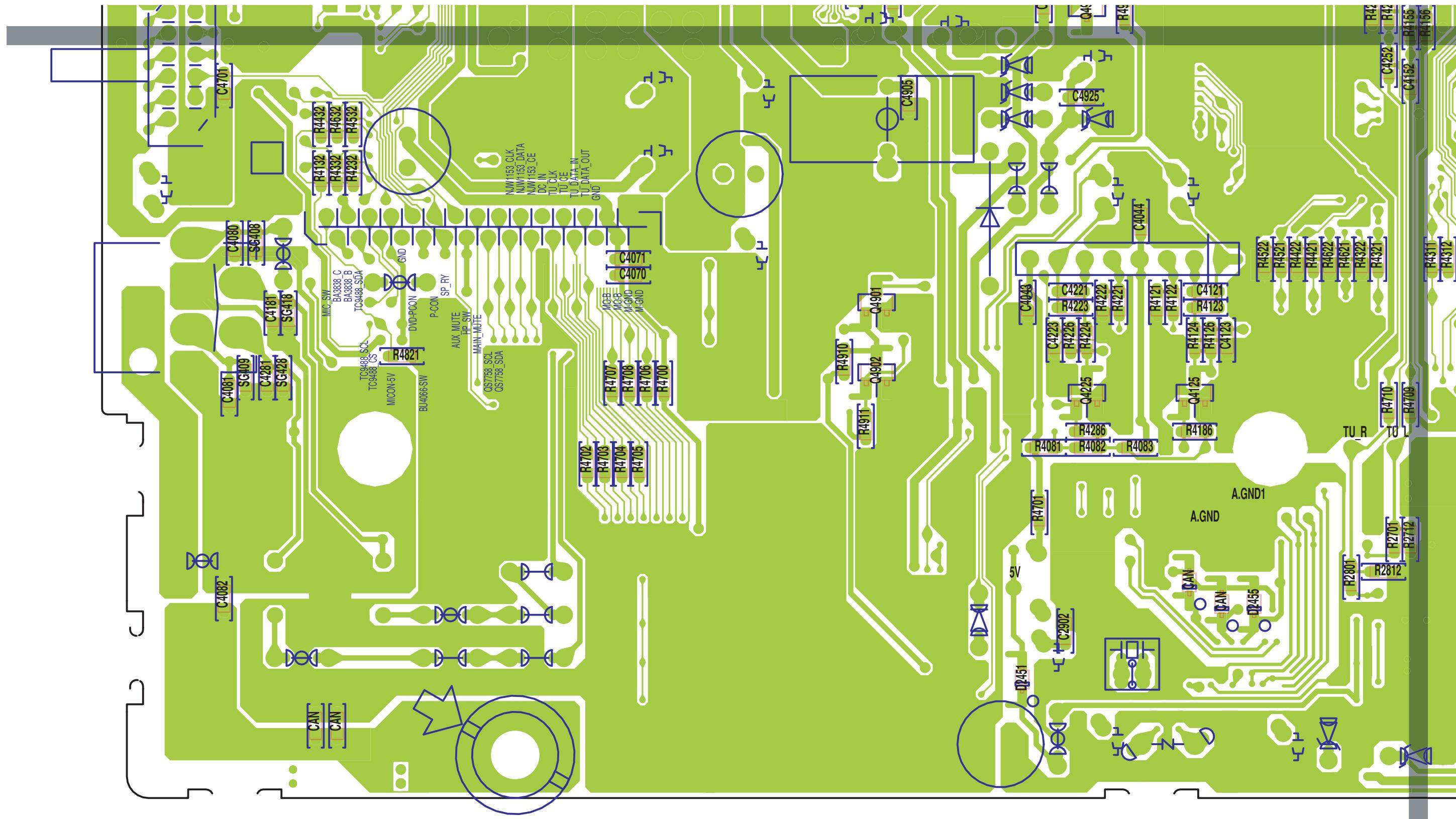
WIRING DIAGRAM (MAIN UNIT DVD/PREAMP/TUNER B SIDE)



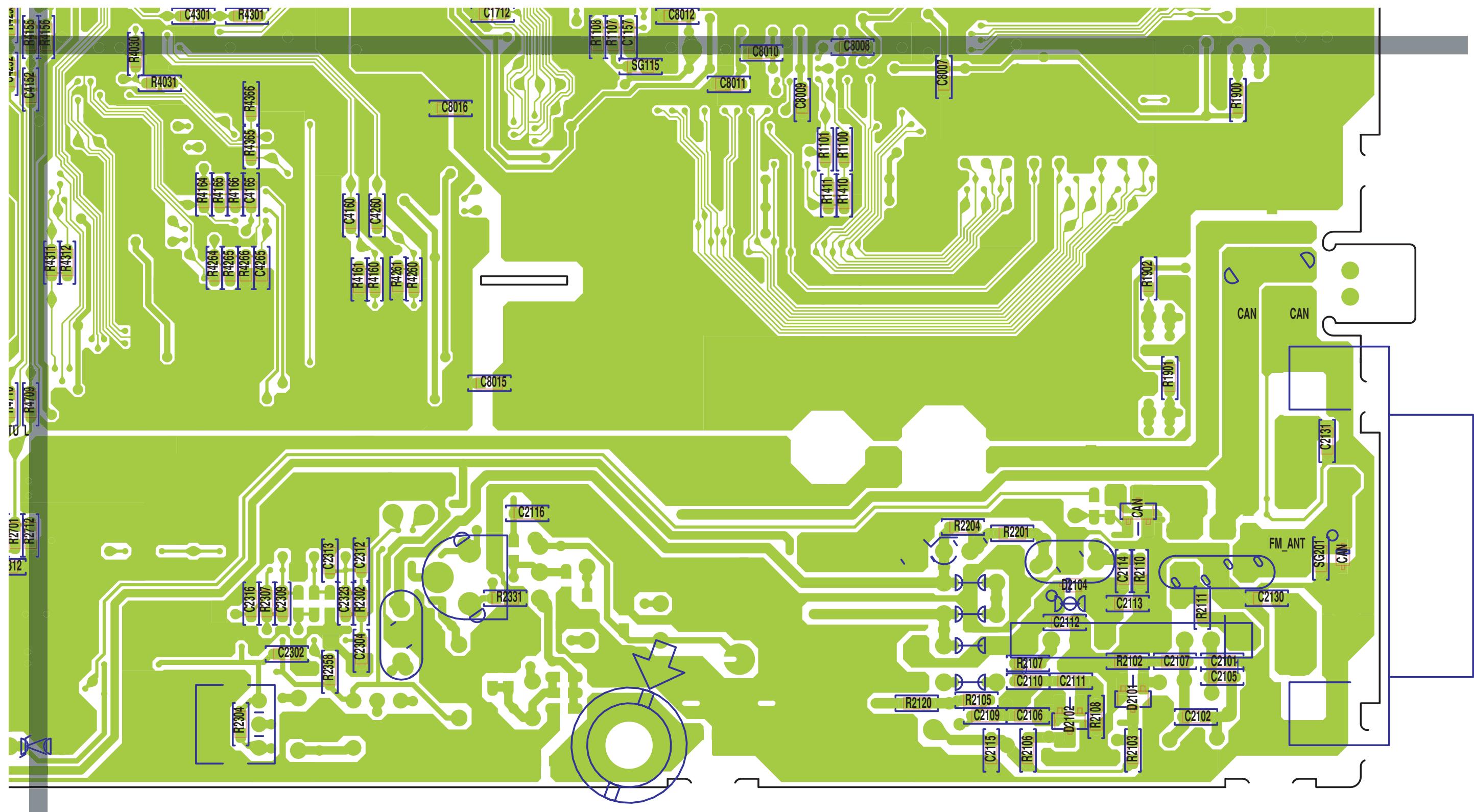
WIRING DIAGRAM (MAIN UNIT DVD/PREAMP/TUNER B SIDE)



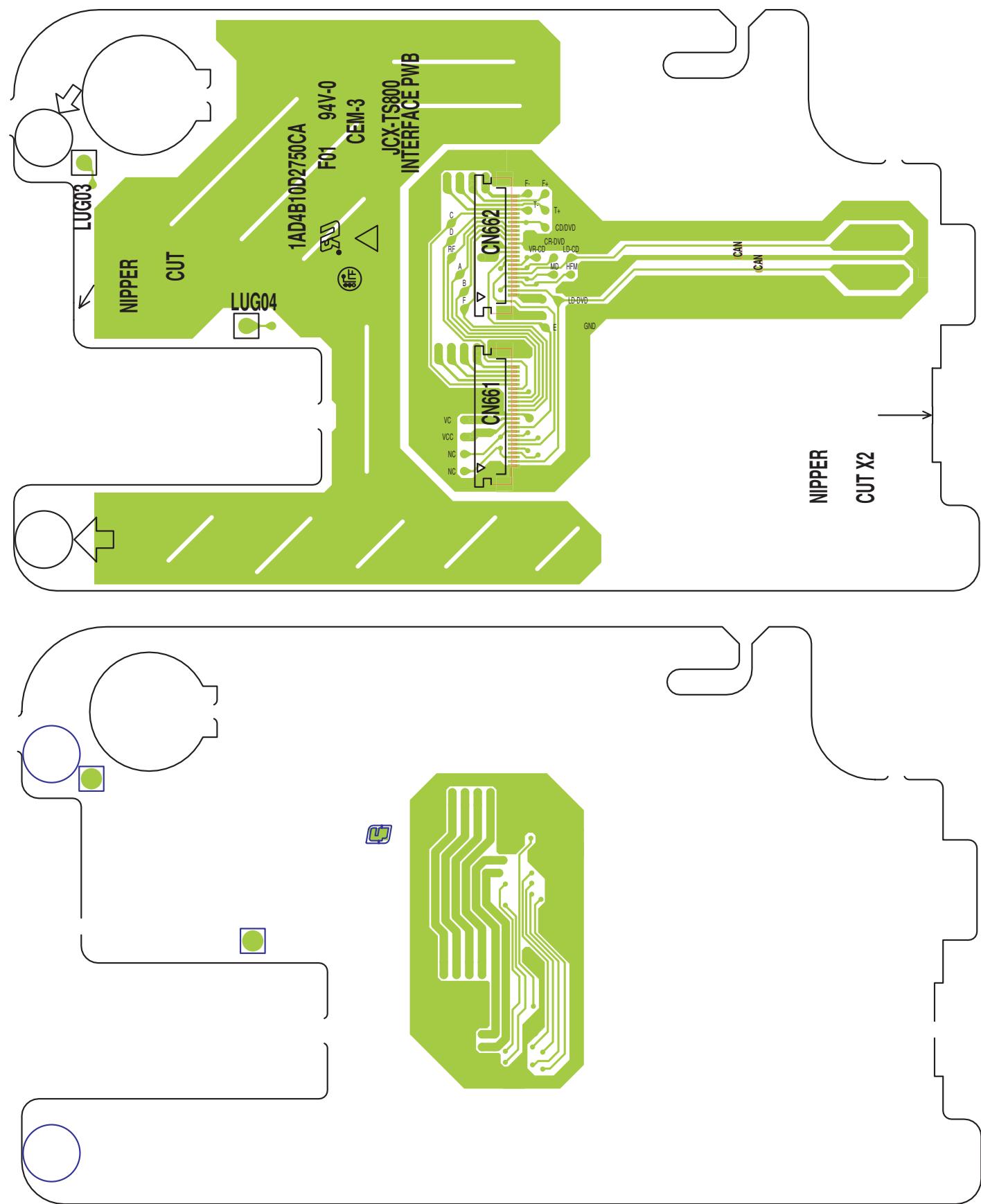
WIRING DIAGRAM (MAIN UNIT DVD/PREAMP/TUNER B SIDE)



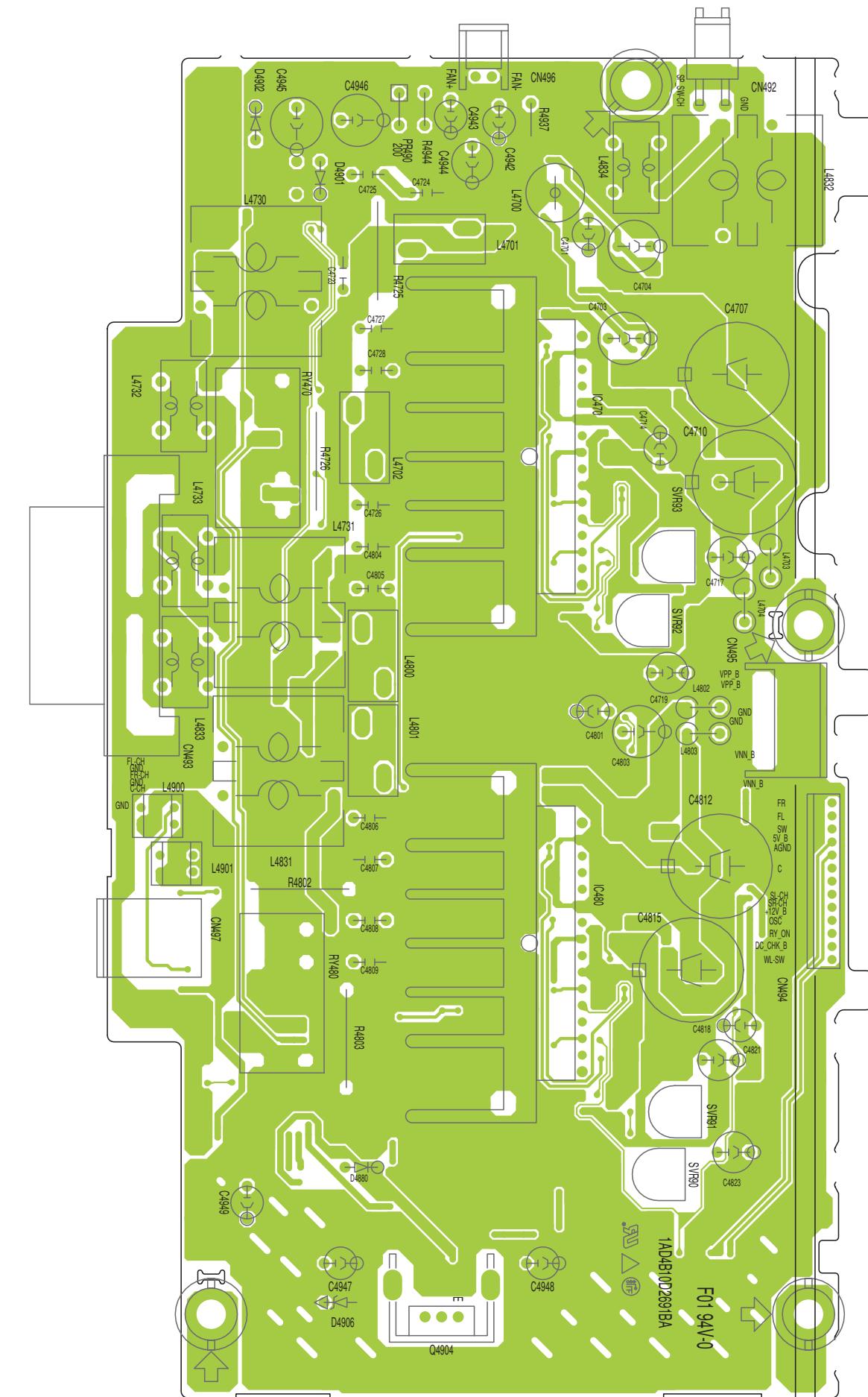
WIRING DIAGRAM (MAIN UNIT DVD/PREAMP/TUNER B SIDE)



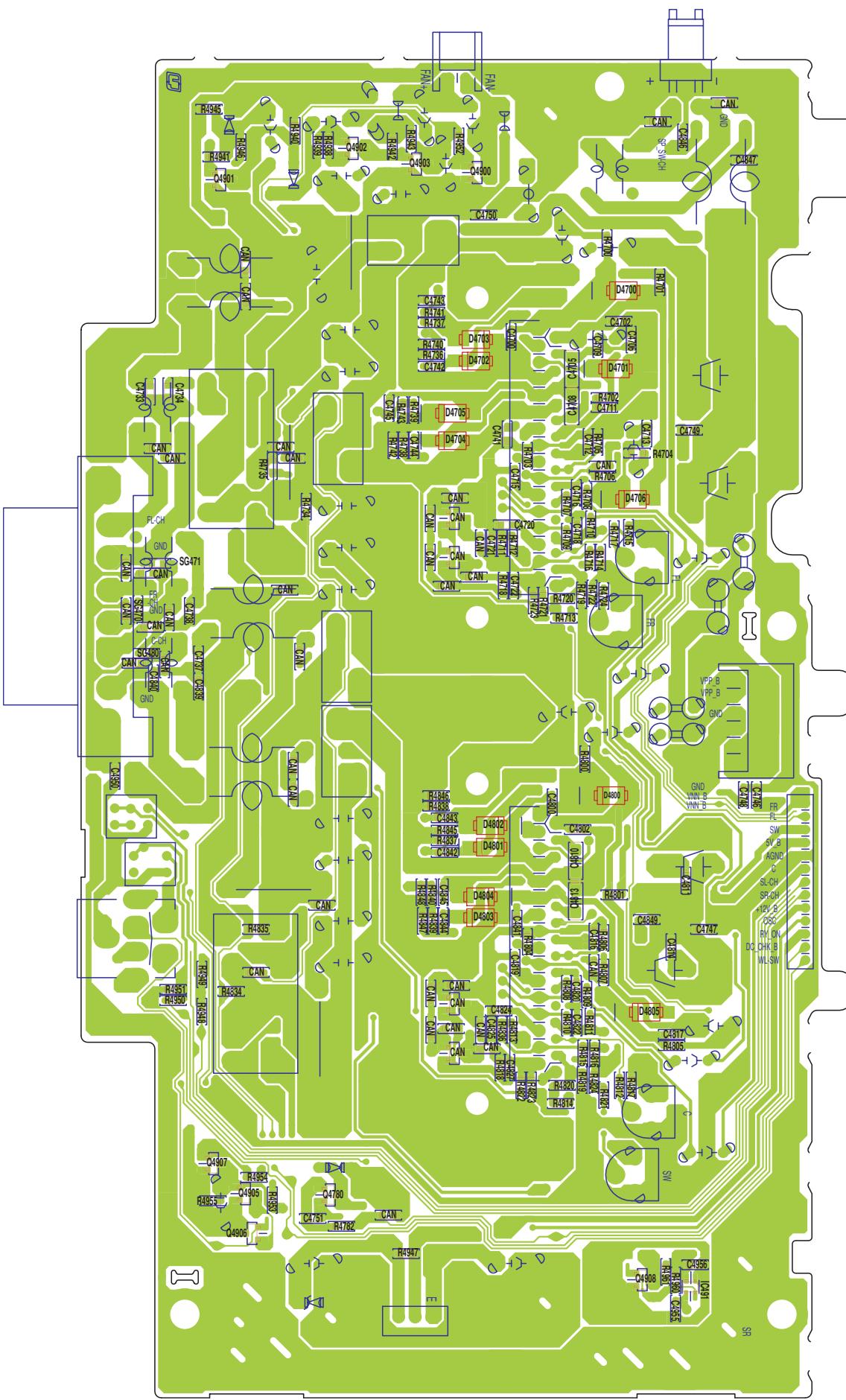
WIRING DIAGRAM (MAIN UNIT INTERFACE)



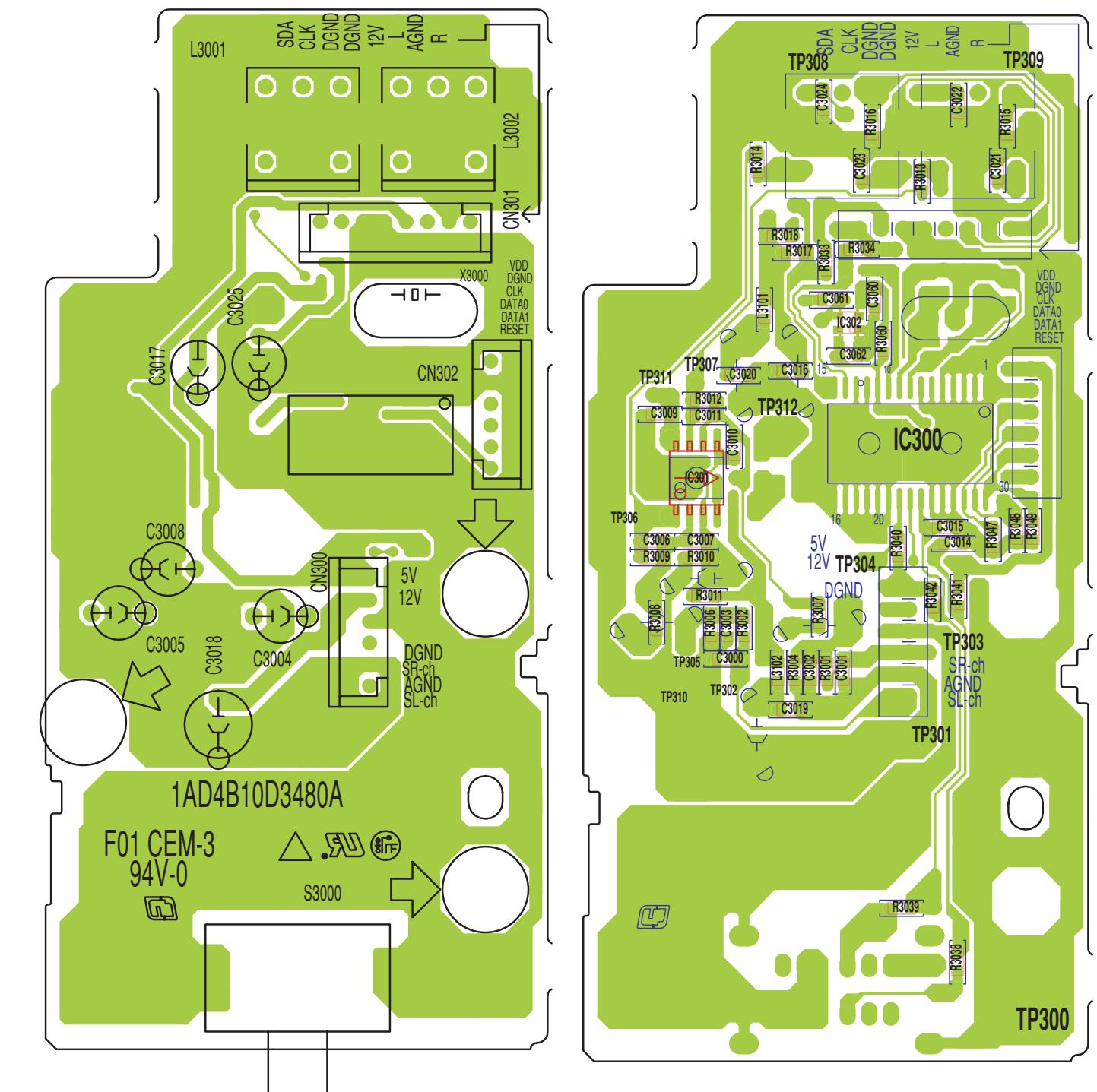
WIRING DIAGRAM (SUBWOOFER SPEAKER POWER A SIDE)



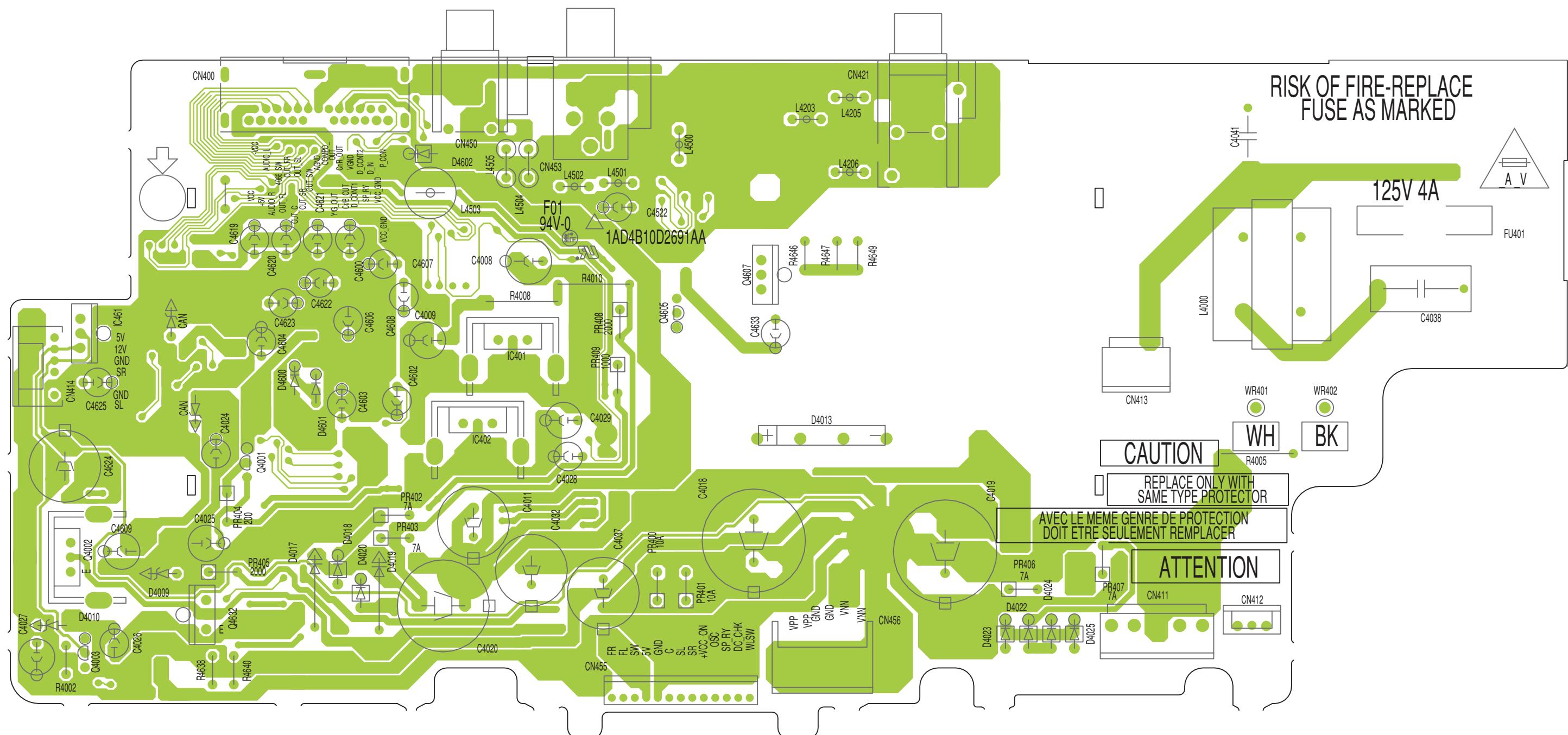
WIRING DIAGRAM (SUBWOOFER SPEAKER POWER B SIDE)



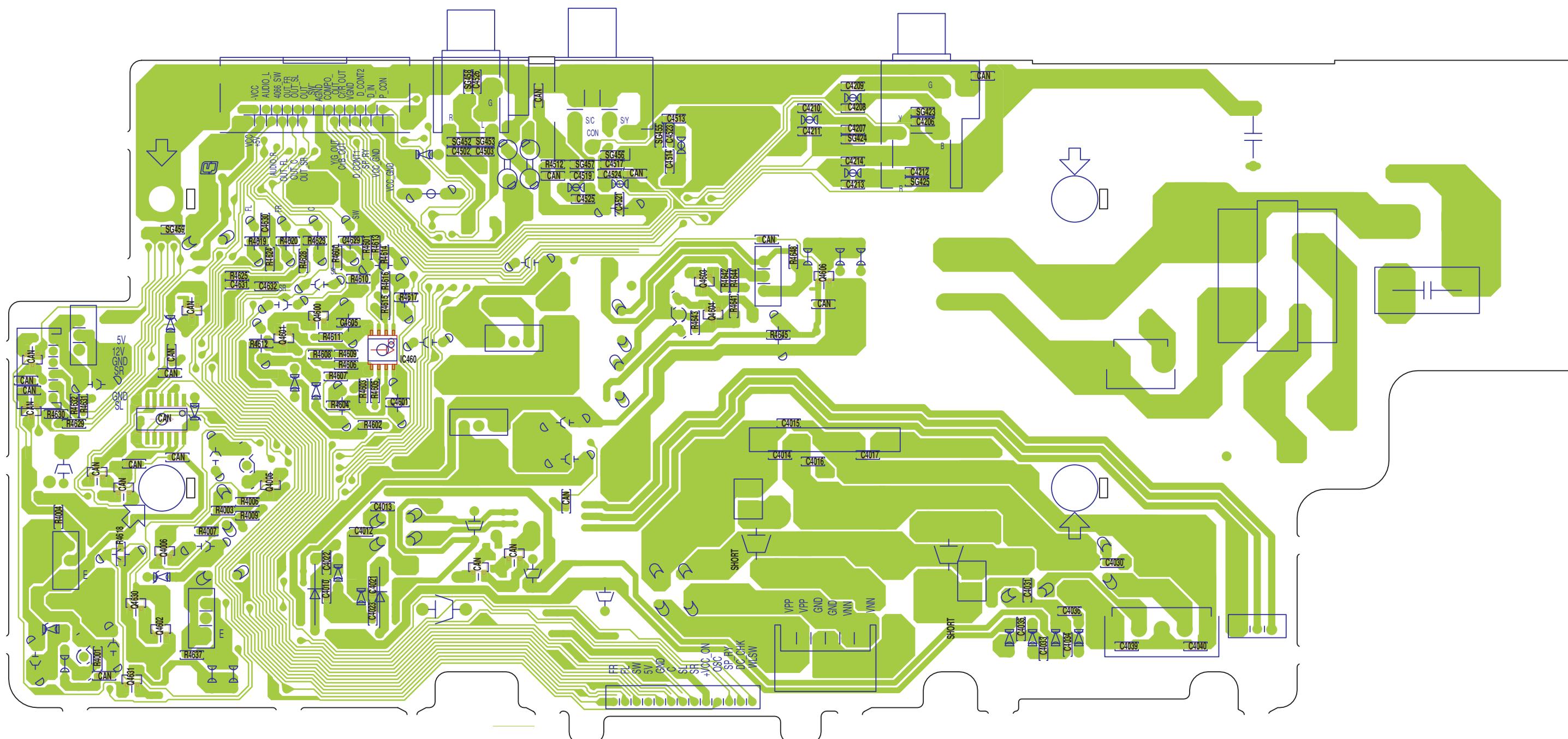
WIRING DIAGRAM (SUBWOOFER SPEAKER TX-INTERFACE)



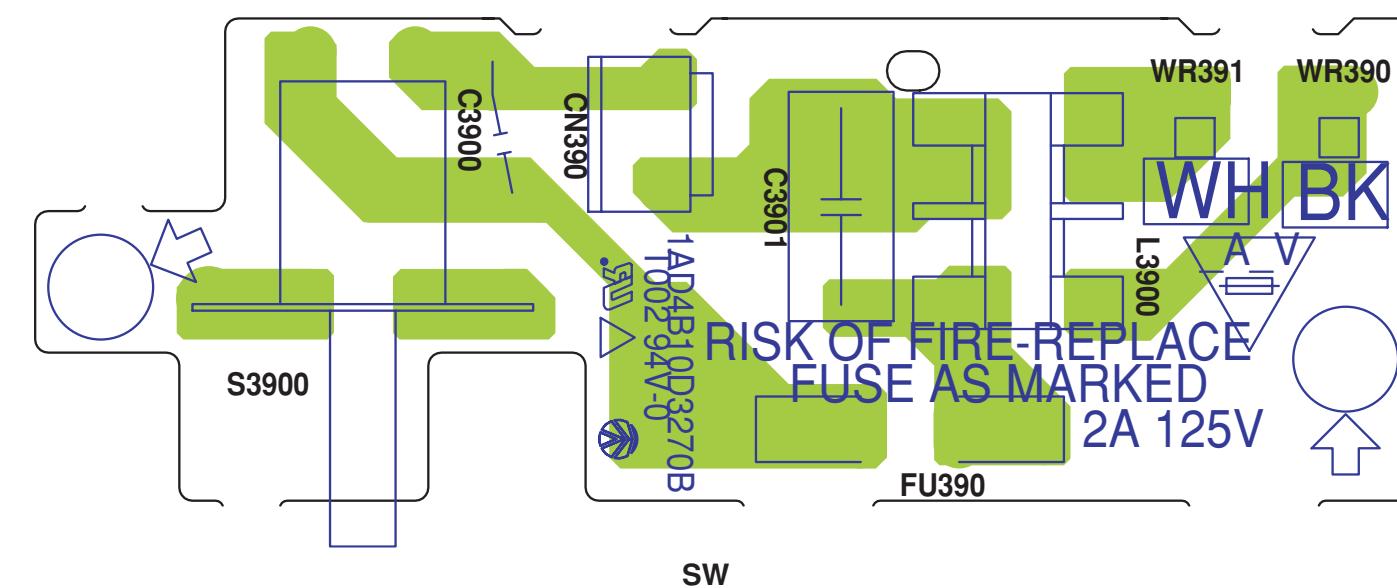
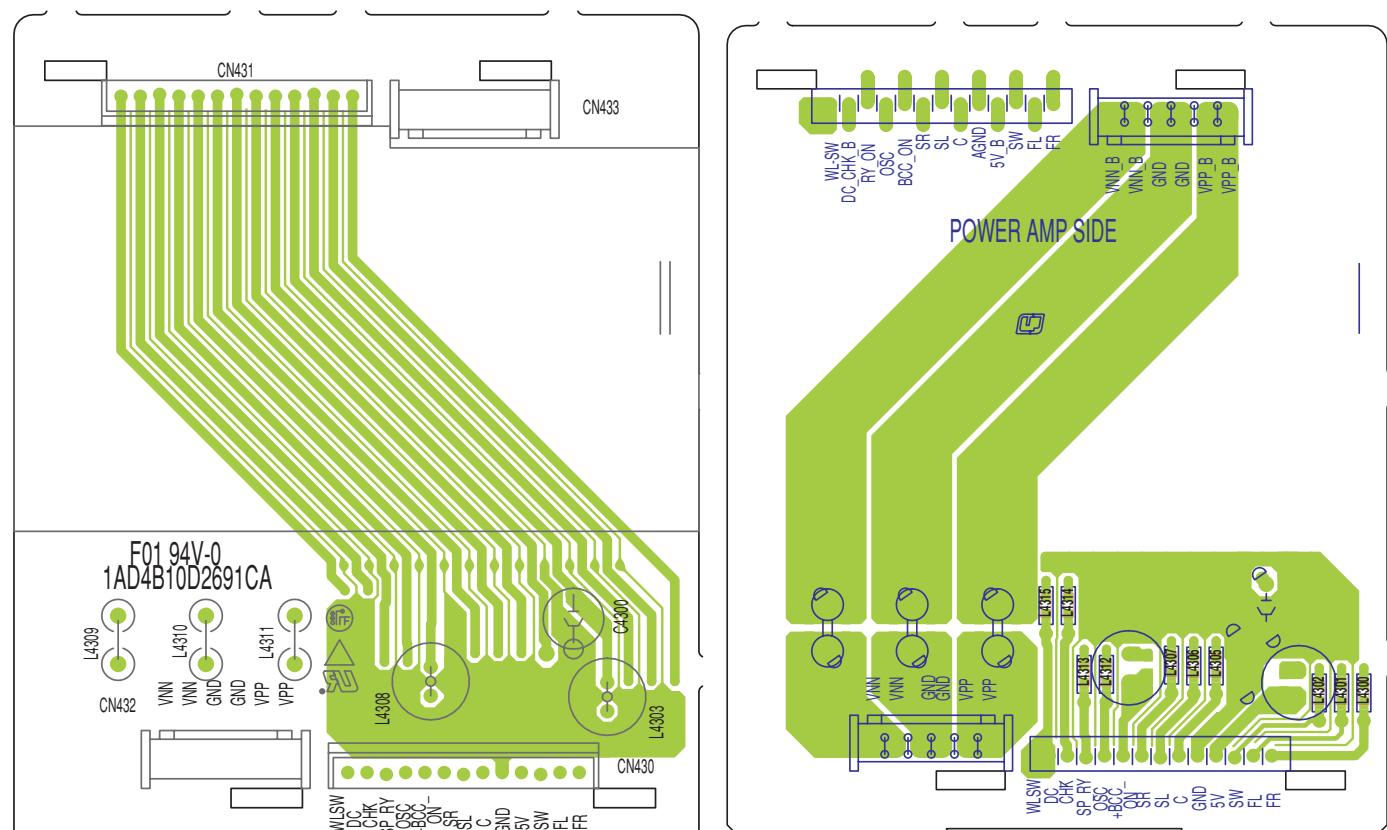
WIRING DIAGRAM (SUBWOOFER SPEAKER MAIN A SIDE)



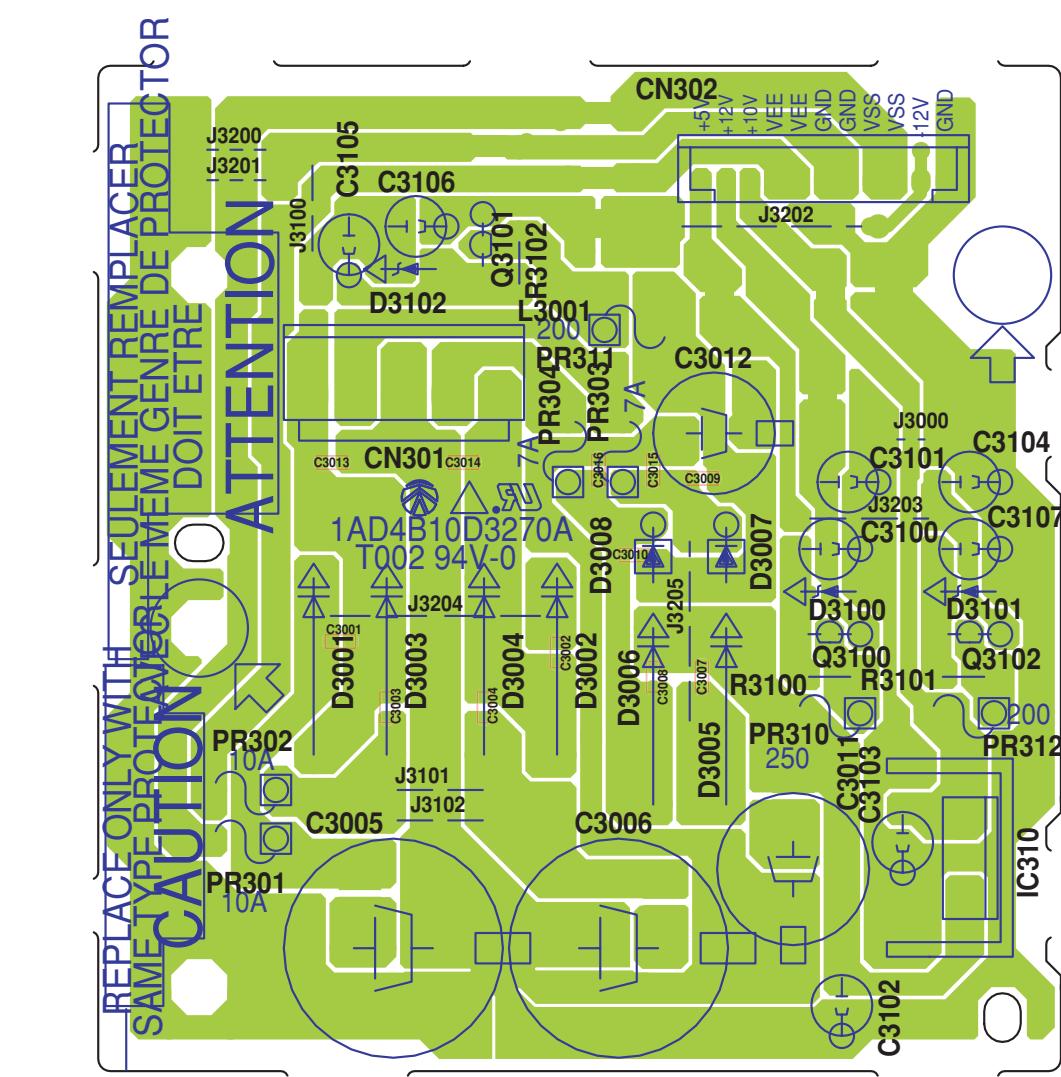
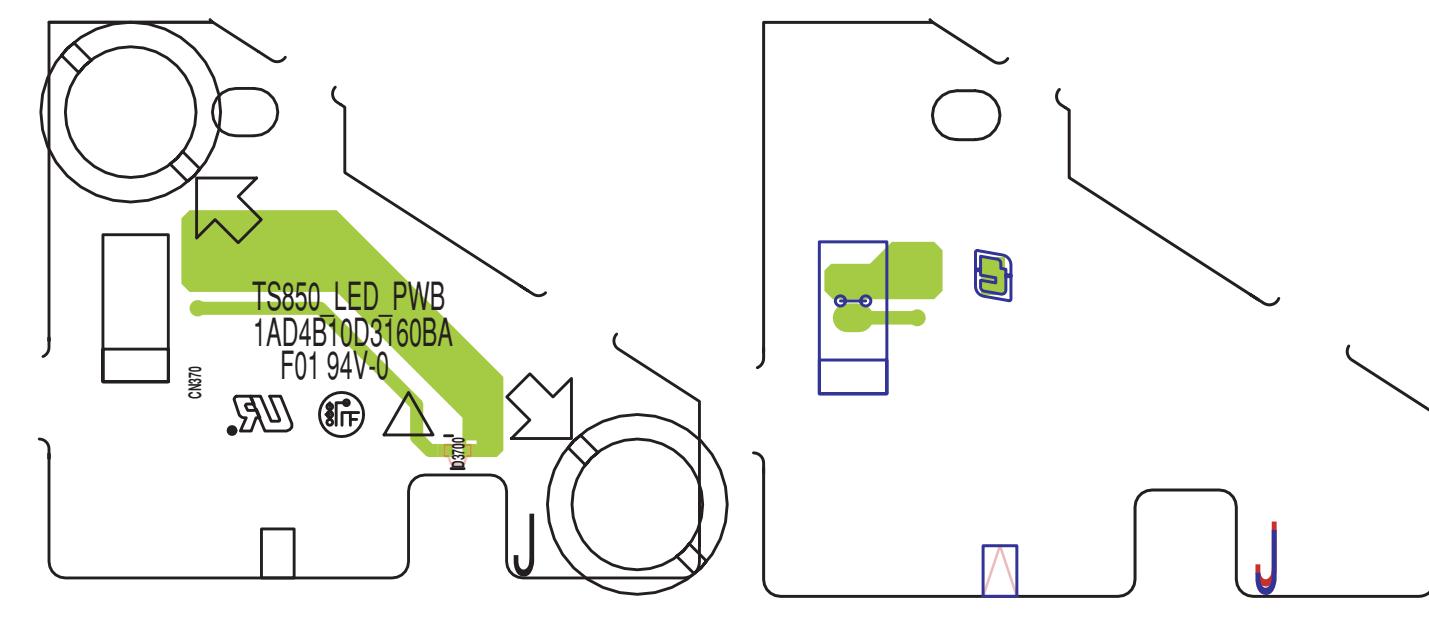
WIRING DIAGRAM (SUBWOOFER SPEAKER MAIN B SIDE)



WIRING DIAGRAM (SUBWOOFER SPEAKER SOCKET , SW)

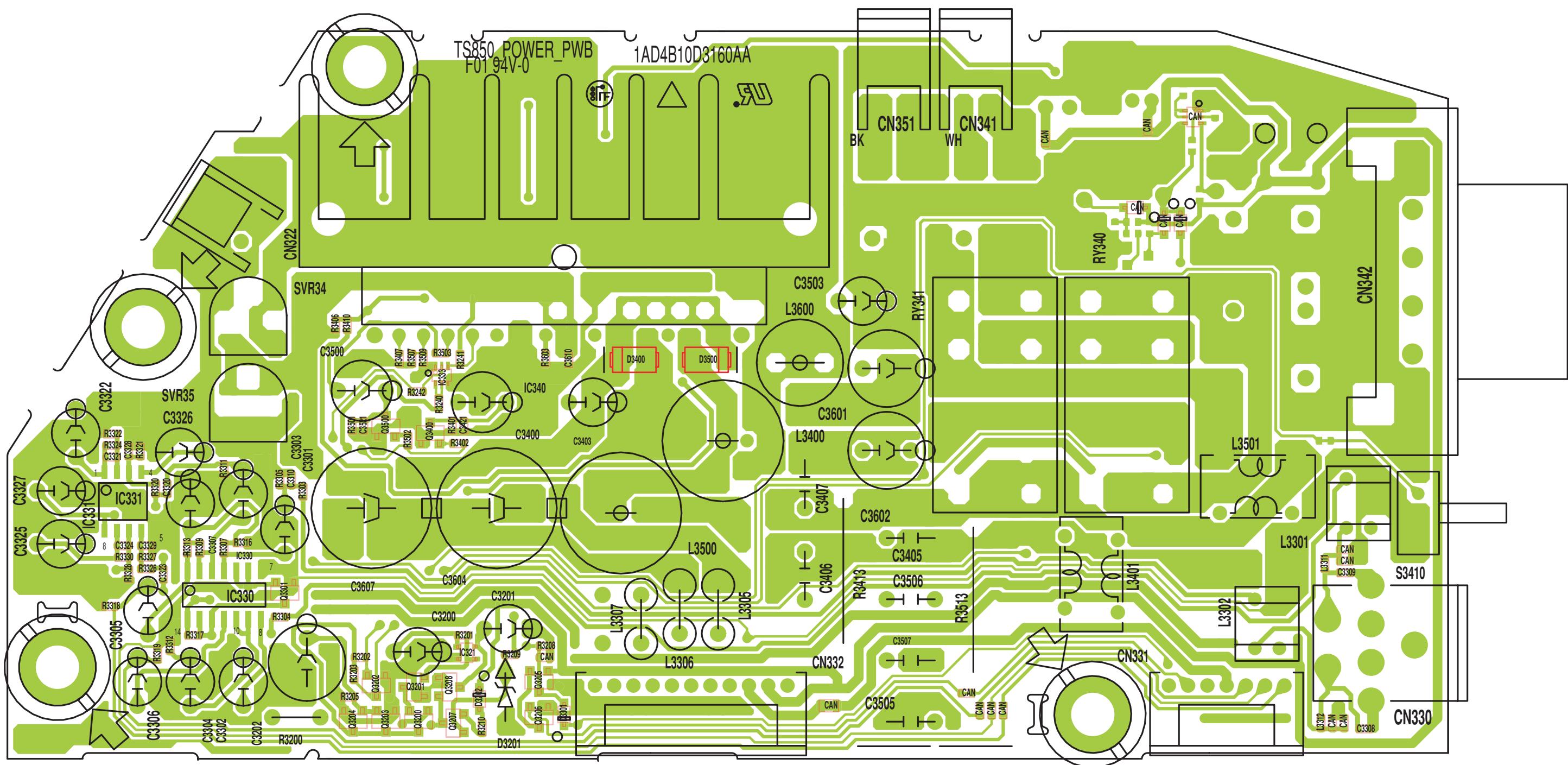


WIRING DIAGRAM (REAR SPEAKER LED,DG)



DG

WIRING DIAGRAM (REAR SPEAKER POWER)



WIRING DIAGRAM (REAR SPEAKER POWER)

