

Mnemonic, Operands	Description	Cycles	14-Bit Opcode MSb LSb	Status Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS					
ADDWF f, d	Add W and f	1	00 0111 dfff ffff	C,DC,Z	1,2
ANDWF f, d	And W with f	1	00 0101 dfff ffff	Z	1,2
CLRF f	Clear f	1	00 0001 1fff ffff	Z	2
CLRWF -	Clear W	1	00 0001 0xxx xxxx	Z	
COMF f, d	Complement f	1	00 1001 dfff ffff	Z	1,2
DECF f, d	Decrement f	1	00 0011 dfff ffff	Z	1,2
DECFSZ f, d	Decrement f, Skip if 0	1(2)	00 1011 dfff ffff		1,2,3
INCF f, d	Increment f	1	00 1010 dfff ffff	Z	1,2
INCFSZ f, d	Increment f, Skip if 0	1(2)	00 1111 dfff ffff		1,2,3
IORWF f, d	Inclusive OR W with f	1	00 0100 dfff ffff	Z	1,2
MOVF f, d	Move f	1	00 1000 dfff ffff	Z	1,2
MOVWF f	Move W to f	1	00 0000 1fff ffff		
NOP -	No Operation	1	00 0000 0xx0 0000		
RLF f, d	Rotate Left f through Carry	1	00 1101 dfff ffff	C	1,2
RRF f, d	Rotate Right f through Carry	1	00 1100 dfff ffff	C	1,2
SUBWF f, d	Subtract W from f	1	00 0010 dfff ffff	C,DC,Z	1,2
SWAPF f, d	Swap nibbles in f	1	00 1110 dfff ffff		1,2
XORWF f, d	Exclusive OR W with f	1	00 0110 dfff ffff	Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS					
BCF f, b	Bit Clear f	1	01 00bb bfff ffff		1,2
BSF f, b	Bit Set f	1	01 01bb bfff ffff		1,2
BTFSZ f, b	Bit Test f, Skip if Clear	1(2)	01 10bb bfff ffff		3
BTFS f, b	Bit Test f, Skip if Set	1(2)	01 11bb bfff ffff		3
LITERAL AND CONTROL OPERATIONS					
ADDLW k	Add literal and W	1	11 111x kkkk kkkk	C,DC,Z	
ANDLW k	AND literal with W	1	11 1001 kkkk kkkk	Z	
CALL k	Call subroutine	2	10 0kkk kkkk kkkk		
CLRWD -	Clear Watchdog Timer	1	00 0000 0110 0100	$\overline{TO}, \overline{PD}$	
GOTO k	Go to address	2	10 1kkk kkkk kkkk		
IORLW k	Inclusive OR literal with W	1	11 1000 kkkk kkkk	Z	
MOVLW k	Move literal to W	1	11 00xx kkkk kkkk		
RETFIE -	Return from interrupt	2	00 0000 0000 1001		
RETLW k	Return with literal in W	2	11 01xx kkkk kkkk		
RETURN -	Return from Subroutine	2	00 0000 0000 1000		
SLEEP -	Go into standby mode	1	00 0000 0110 0011	$\overline{TO}, \overline{PD}$	
SUBLW k	Subtract W from literal	1	11 110x kkkk kkkk	C,DC,Z	
XORLW k	Exclusive OR literal with W	1	11 1010 kkkk kkkk	Z	

Note 1: When an I/O register is modified as a function of itself (e.g., `MOVF PORTB, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

- If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.
- If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

f = file register address	W = working register (accumulator)
d = destination, W(0) or f(1)	k = literal field, constant data or label
b = bit address within an 8-bit file register	x = don't care location
TO = time-out bit	PO = power-down bit