Issues with Low-Input-Voltage Boost Converter Design

J. W. Kimball[1], T. L. Flowers[2], P. L. Chapman[1]

[1]University of Illinois at Urbana-Champaign, Urbana, IL USA
[2]Northrop Grumman Space Technology, Redondo Beach, CA USA

***Abstract*- This paper addresses boost converter circuits that are built for very low input voltages, i.e. less than 1 V. Such circuits can be useful for single-cell solar and fuel cell power supplies. Important issues are physical size, high conversion ratio, efficiency, and startup. Several experimental studies show the impact of these issues. A startup technique is proposed that works for arbitrarily low input voltages.**

I. Introduction

Power converters driven from low input voltage (< 1 V) would be of practical use for some applications, including micro fuel cell powered portable electronics. For reducing packing, fuel flow, and wiring overhead, single-cell versions of fuel or solar cells may be an optimal choice from the fuel cell design perspective, but has significant impact on power management. This work, which addresses various issues with low-input-voltage design, was motivated primarily by single-fuel-cell power supplies for portable electronics.

Virtually all of the low-power, portable electronics market requires power conversion from batteries. Primary alkaline cells are nominally 1.5 V, lithium-ion rechargeable cells are 3.6 V to 4.0 V, lead-acid cells are about 1.2 V, while NiMH is about 1.8 V. Thus, all low power (< few watts) dc-dc converters we could find available commercially (e.g. [1-4]) do not work with input significantly below 1 V.

A recent push for fuel cell power supplies may change this paradigm dramatically. Single fuel cells fundamental have voltages that vary from about 0.5 V (full load) to 1.0 V (no load), under the best conditions – as fuel is spent or air flow is blocked, the voltage can be lower. While fuel cells can be stacked, it comes with packaging and other complications. Therefore, a need may exist for low-power dc-dc converters that operate with as little as 0.4 V, or less. Even with a two-cell stack, the full load voltage can be as low as 0.8 V to 1.0 V.

Low-input-voltage power converters, somewhat surprisingly, have not been widely addressed. In [5], a 0.3 V thermoelectric generator was used for power scavenging. A complete system was shown that was essentially a synchronous boost with a resonant tank startup circuit. In [6], the authors investigate a few different circuit topologies for power coming from a single solar cell. The startup problem was not handled in a practical method, but the authors did demonstrate reasonable efficiency from a 0.5 V supply. Several issues encountered with their (high-power) system were discussed in some detail. This paper concentrates on low-power, low-input-voltage conversion wherein space and cost are very important (such as in portable electronics). In conference article [7], a new inductor design is presented in the context of a single-cell solar converter (0.4 V). The paper focuses on the inductor design, with telling details of converter and startup design absent. In a corresponding journal paper [8], the power converter material was not included.

In the following, we investigate efficiency and startup problems with some example converter specifications. The target application is a fuel-cell powered mobile phone. This work differs from previous work in that efficiency is more carefully analyzed and in application (low power fuel cells). A simple startup technique is suggested that is suitable for low input voltage. Several experiments illustrate the points.

II. Low-Voltage Boost Converter Efficiency

Efficiency of the basic power converter circuits such as buck, boost, etc. have been well established for some time. Here, we present some calculations specific to the application of low input voltage.

Given that the power level is low (< 3 W), the voltage is low (< 3.3 V) and efficiency demands are high, only synchronous rectification will be considered. Most commercial chip-based battery converter designs employ synchronous rectification. The majority of the loss with be in the inductor and power switches. The inductor losses can be separated into ohmic and core losses. In this application, the ohmic losses will dominate as is shown below. The losses in the switches will also be dominated by ohmic losses (though switching losses play some part) in this application.

The impedance levels (< 20 mΩ) will be very low for the given power level. In that range, there is a narrow selection of parts, leading to discrete choices in design. Interconnects and board traces become significant loss factors. For achieving low cost and size, there is fundamentally only so low the impedance can be. Thus, a good first-cut to efficiency analysis is to include only ohmic losses. Later, we budget a certain power loss to ohmic losses and leave the remainder to switching and core losses.

The dc resistance of the inductor is r_L, the trace resistance is r_t, and the on-resistance of either MOSFET is r_{sw}. In continuous mode, the converter input current, i_{in}, is conducted through the inductor and through one of the switches. Considering dc quantities (designated by corresponding capital letters),

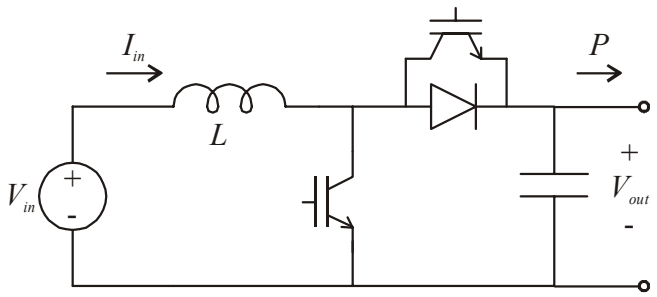

Fig. 1: Synchronous boost converter with signal definitions.

$$V_{in} I_{in} = P_{out} + K I_{in} + R I_{in}^2 + r_C I_C^2 + P_{oh} \quad (1)$$

where V_{in} is the input voltage, P_{out} is the output power, and R is the sum of r_L, r_t, and r_{sw} and any other, presumably much smaller, series resistance. The resistance r_C is the equivalent resistance of the capacitor, and I_C is the rms capacitor current. The factor K (volts) accounts for the switching loss. This constant factor is determined based on a given output voltage, V_{out}, and frequency, f_{sw}, that are fixed. K can be altered by various factors in design, but can be budgeted such that we can trade off switching losses with ohmic losses. That is, the lower the on-resistance of the MOSFET, the slower the turn-on time (and thus the higher the switching loss). The constant P_{oh} represents the control power (typically < few mW).

The capacitor conducts two levels of current, either $-I_{out}$ or $I_{in} - I_{out}$, approximately. By constraining the average capacitor current to be zero, we can determine the squared rms capacitor current as

$$I_C^2 = I_{out}(I_{in} - I_{out}) \quad (2)$$

where $I_{out} = P_{out} / V_{out}$.

The K factor can be estimated from turn-on or –off times of the MOSFETs. From [9], the switching energy loss of one switch is

$$W_{switch} = \frac{V_{off} I_{on} t_{switch}}{6} \quad (3)$$

where V_{off} is the off-state voltage, I_{on} is the on-state current, and t_{switch} is the sum of on and off switching transition times. Multiplying by switching frequency, f, to convert to power loss and accounting for both switches,

$$K = \frac{f V_{out} t_{switch}}{3} \quad (4)$$

Making appropriate substitutions into (1), we can solve the quadratic equation

$$0 = R I_{in}^2 + \left(K + r_C \frac{P_{out}}{V_{out}} - V_{in} \right) I_{in} + P_{ov} + P_{out} - r_C \left(\frac{P_{out}}{V_{out}} \right)^2 \quad (5)$$

The appropriate was chosen based on practical converter considerations. When solving (5) yields a complex number, it indicates that it is not possible to achieve the given output power for a low input voltage. Either the output power must be upper-bounded, or the input voltage lower-bounded for given component values.

The efficiency is straightforward from (1) and (5).

$$\eta = 100 \frac{P_{out}}{V_{in} I_{in}} \quad (6)$$

For given P_{out}, as V_{in} is lowered I_{in} must increase. Equation (6) shows that the efficiency will reduce quadratically as input voltage is reduced linearly.

III. Efficiency and Voltage Collapse Examples

To show a concrete example of these issues, a target design was considered. The maximum power output is 3 W at 3.3 V, similar to many portable applications. The input voltage varies from 1.0 V to 0.4 V, much like a single fuel cell. A synchronous boost converter was constructed to meet these requirements.

By studying (5) under these specifications, we find voltage collapse occurs if there is any significant magnitude to R at all. Therefore, the lowest resistance components were sought. For the MOSFETs, 4 mΩ devices were used. These devices have high gate capacitance and slow switching. Only 200 kHz was achievable. A lower switching frequency would yield much lower switching losses, but a larger inductor would need to withstand the current ripple. Even so, we settled for a commercially available 10 µH inductor that has 10 mΩ dc resistance. The output capacitor has equivalent series resistance of 13 mΩ. In the final board layout, approximately 4 mΩ of trace resistance resulted.

Based on these figures, $K = 0.022$ V, which is significantly lower than the minimum input voltage, 0.4 V. From (5), we see that K and V_{in} both impact the I_{in} term, meaning that the high value of K will have a high impact on efficiency. Though r_C is high relative to the other resistances, the rms capacitor current is not particularly high, and only milliwatts are lost in the capacitor at full load.

In Fig. 2, a plot of efficiency versus output power for four different input voltages is given. The decreasing efficiency with power output is apparent as well as the voltage collapse occurring at the 0.4 V input. This occurs

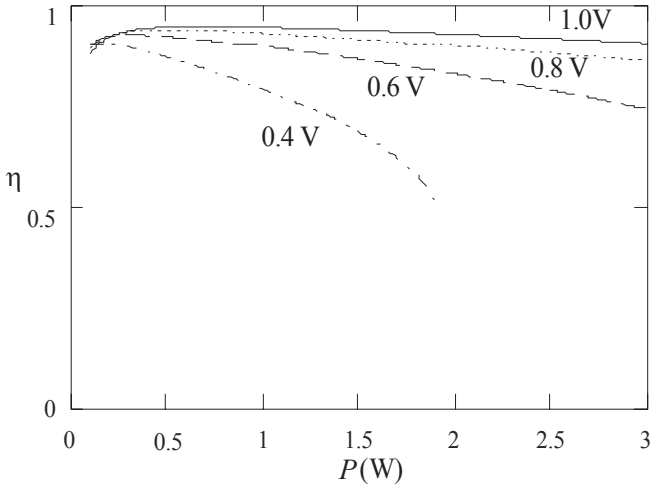

Fig. 2: Predicted efficiency versus power output for various input voltages.

despite using the lowest resistance MOSFETs available. Some improvement can be obtained by reducing trace resistance further, yet there will always be some. Using an inductor with a lower series resistance would help significantly for efficiency. However, the inductor is physically large as it is even at 200 kHz for the large MOSFETs.

In Fig. 3, a photograph of the test circuit is shown. Given that this is only intended to be a 1 W converter (at least at the 0.4 V input level), the size is very large. The large inductor is a consequence of requiring such low resistance combined with high inductance (since f is only 200 kHz). Several connectors are included on the board for test points, which would not be present in a final version.

Fig. 4 shows the efficiency as measured versus power output. Compared to Fig. 3, the trends are the same though the overall efficiency is lower. From experimenting with the model, the difference is due to underestimating switching losses by a factor of two to three. We also considered core losses, which were not included in the model. However, the effect was very small since the observed core loss was only a few milliwatts. Gating loss (the charging and discharging of the gate capacitance for the MOSFETs) was approximately 50 mW, and not shown in the model. However, it can simply be added to P_{ov}. Gating loss has the most effect on light load efficiency. The voltage collapse effect is very evident in the 0.4 V trace, as expected.

In Fig. 5, the efficiency versus input voltage is plotted for a constant 1 W power output. The collapse at low voltage is evident. The efficiency is low for all cases, despite the very low resistance MOSFETs and inductor used. For the fuel cell application, the voltage decreases with increasing load. Therefore, the fuel cell would need to be oversized in order to operate at high voltage, or suffer from very low cell and power converter efficiency. The best operating point will require careful optimization.

Fig. 3: Photograph of 3 W (nominal) low-input-voltage converter.

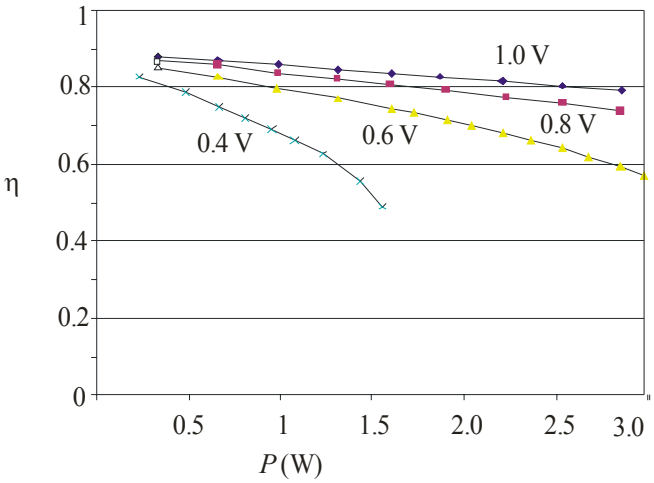

Fig. 4: Measured efficiency vs. power output.

IV. Startup From Low Voltage

Commercial circuits currently available do not start from less than 0.9 V. Some new logic devices will run from as little as 0.8 V, with thresholds down to 0.65 V on lateral MOS gates. Power FET gates still require more voltage, so starting the circuit from less than 1 V is nontrivial. The low-input-voltage commercial chips are strongly tied to battery management, and aren't likely to be reduced for the time being. Discrete circuits typically require much more voltage to start (1.8 V, for example). Therefore, a technique for starting low voltage power circuits required.

In [5], a circuit was proposed that uses a UJT and a resonant transformer circuit to step up a low voltage. The circuit works by first connecting the source, which conducts through the normally-on UJT and transformer primary, and

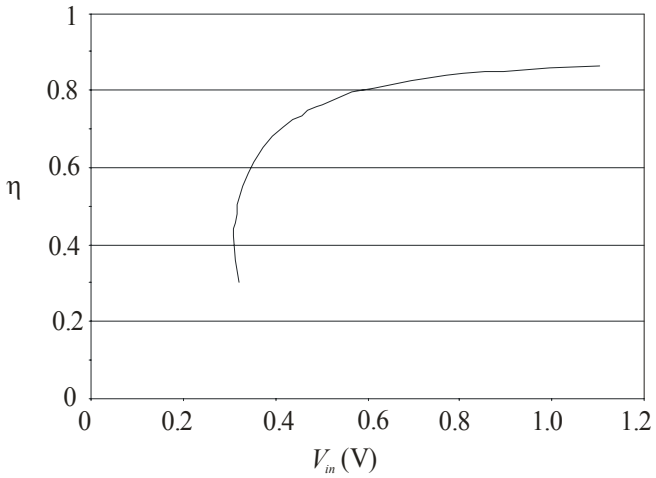

Fig. 5: Measured efficiency at 1 W versus input voltage.

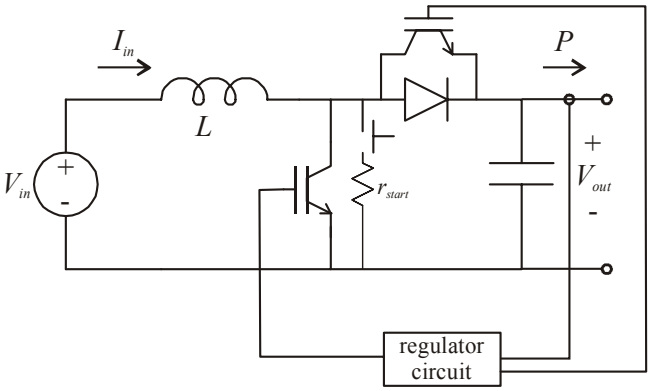

Fig. 6: Start-up circuit technique.

allowing the initial transient to resonate in secondary transformer windings and capacitors. A capacitor achieves enough voltage to switch off the UJT, and in doing so, starts another transient that builds up enough voltage to run a regulator circuit. While a very appropriate idea for a higher power converter in an application where space is not problematic, the circuit is complicated and space-consuming for portable electronics applications.

A simple way to start a low voltage circuit is shown in Fig. 6. Therein, a mechanical switch is placed in series with a small resistance r_{start} across the lower MOSFET. This switch is not an extra component – it is intended to be the same switch that would ordinarily be present for the user to turn on the device. When depressed, the inductor charges quickly. The current is limited by r_{start}. The switch is opened and the inductor current must divert through the diode and onto the capacitor. If r_{start} is selected appropriately, enough charge will store on the capacitor to supply the regulator circuit long enough for it to self-sustain.

The inductor L and capacitor C are chosen according to other factors in power converter design, such as allowable voltage ripple and core loss. As such, this leaves only r_{start} as a design parameter. The energy stored in the inductor after the switch is depressed for sufficient time (four or five time constants or more) is

$$W = \frac{1}{2} L \left(\frac{V_{in}}{r_{start}} \right) \tag{7}$$

When released, this energy will move through the diode and onto the capacitor. If all the energy transfers (neglecting loss), then

$$r_{start} = \sqrt{\frac{L}{C}} \frac{V_{in}}{V_{out}} \tag{8}$$

is the resistance that ideally produces the required output voltage that can be used to temporarily power the regulator circuit. In reality, (8) is only a starting point for design. A minimum value of V_{out} to trigger the control circuit should be considered. Generally, r_{start} will be a small resistance, but still significantly larger than r_L.

In Fig. 7, the start-up output voltage of a test circuit is shown, based on the new technique. Initially, the capacitor charges to V_{in} (about 0.7 V in this case). Then, the switch is depressed and released. The output voltage ramps up and briefly overshoots the desired set point. During the overshoot, the regulator circuit starts. In this case, a relatively high regulator current (about 8 mA) was required, so a quick discharge begins to occur. Then, the regulator begins to control the voltage. A second peak in voltage occurs as the controller responds. In the steady-state, the desired 4.0 V output is maintained.

Design of the startup circuit is very sensitive to resistance. Resistance of the switch and interconnects must be considered when choosing r_{start}. Furthermore, multi-pole switches may be considered for switching in the load or turning off the supply or both.

The circuit should work in other power converter circuits, including buck-boost, forward, half-bridge, and other converters. The essential point is that a switch and resistor be placed in parallel with the appropriate transistor.

V. Conclusions

Several facets of low-input-voltage boost converter design were shown. The main point is that for low voltage sources, such as single fuel or solar cells, the circuit impedances have to be very low to achieve high efficiency. The design is very delicate with respect to layout and inductor choice. The switching frequency will be low for the power level since the MOSFETs will be physically large. However, switching power losses will likely be low. A low-voltage start-up technique was suggested that may be helpful

if a mechanical switch is to be used to turn on the circuit. Overall, the power density is low and the cost is high when using boost converters for single-cell input applications. Whether this is a problem depends on the relative cost (packaging and wiring overhead) of going to multi-cell systems.

VI. Acknowledgment

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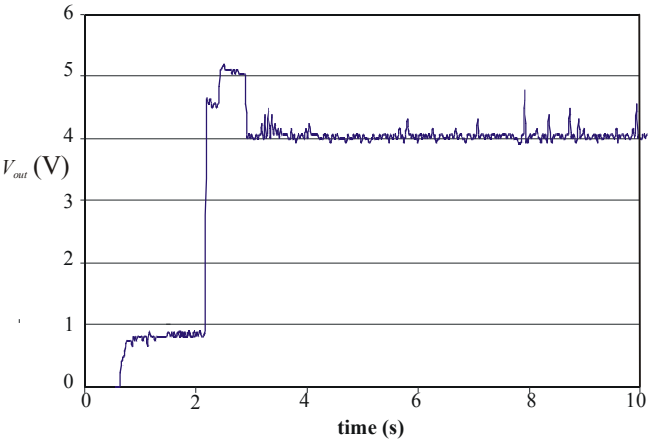

Fig. 7: Measured start-up output voltage.