Passive all-optical polarization switch, binary logic gates, and digital processor

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Abstract: We introduce the passive all-optical polarization switch, which modulates light with light. That switch is used to construct all the binary logic gates of two or more inputs. We discuss the design concepts and the operation of the AND, OR, NAND, and NOR gates as examples. The rest of the 16 logic gates are similarly designed. Cascading of such gates is straightforward as we show and discuss. Cascading in itself does not require a power source, but feedback at this stage of development does. The design and operation of an SR Latch is presented as one of the popular basic sequential devices used for memory cells. That completes the essential components of an all-optical polarization digital processor. The speed of such devices is well above 10 GHz for bulk implementations and is much higher for chip-size implementations. In addition, the presented devices do have the four essential characteristics previously thought unique to the microelectronic ones.

OCIS codes: (200.4660) Optical logic; (200.6715) Switching; (200.3050) Information processing; (230.1150) All-optical devices; (230.3750) Optical logic devices; (320.7080) Ultrafast devices; (320.7085) Ultrafast information processing.

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1. Introduction

Optical computers are a 60-year old evasive idea. Lots of scientific research has been carried out to achieve this goal over the years with a very limited success. In the last few years, several publications were devoted to comparing optical computers to microelectronic ones. Reference [1] discusses in some details why future supercomputing requires optics. Reference [2] takes the opposite position and enumerates the advantages of microelectronics over optics in a somewhat speculative manner. Reference [3] discusses the prospects of the optical transistor being the logical next step in logic devices. In addition, some characteristics of the semiconductor industry are thought to be unique to the industry and it is alluded that no optical counterpart can exist [2–4]. These characteristics are 1) cascadability, 2) fan-out, 3) logic-level restoration, 4) input-output isolation. Optics is known to have a much higher speed and consumes much less energy in propagation and in logic operations. In this paper, we prove that it is wrongly assumed that "any form of scalable digital computing requires nonlinear elements to process digital data [2]." In addition, we prove that it is also wrongly

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assumed that "for large scalable logic circuits, no optical element or circuit, either active or passive, can do this and at the same time compete with transistors in the key metrics of energy consumption and small device footprint [2]." In the next few sections, we introduce scalable, passive, all-optical devices that satisfy the 4-characterstics discussed above, and defy the speculative assumptions about optical-logic devices. The fact that the main thrust of research and discussions in optical-logic is focused on replacing the transistor and using intensity for digital level representation, in direct simulation of microelectronics, is in our opinion what is holding back the advancement of the subject [5–7].

In 1980, an overview of the then state-of-the-art of hybrid bistable optical devices was presented [8]. In 1981, masks are used with liquid crystals operated as controlled birefringent mirrors to implement the 16 logic gates, some as positive logic gates and some as negative logic gates [9]. In 1985, opto-electronic bistable devices using liquid crystals are reported for image processing and logic operations [10]. The possibility of using light polarization to represent binary logic was proposed in 1986 by providing a speculative account of combining nonlinear optics and polarization optics [11]. In 1987, the same author suggested spatial filtering logic based on polarization [12]. Also, in 1987, other authors introduced polarization-based optical parallel logic gates utilizing ferroelectric liquid crystals, where the two parallel and perpendicular polarizations were used to represent the two states of binary logic, where only the XOR and XNOR gates could be realized [13]. In the same year, other authors introduced polarization-encoded optical shadow-casting logic units and their design [14]. Masks and on/off logic representation were used, and multiple-valued logic based multiprocessor using polarization-encoded optical shadow-casting were later developed in 1993 [15]. In 1990, polarization-based optical logic using laser-excited gratings were introduced [16], and in 1992 polarization-coded optical logic gates for N-inputs using vertical/horizontal input logic representation and on/off output logic representation were introduced [17]. The polarization encoding was not carried through to the output in such a design. In 1993, polarization-encoded optical logic operations in photorefractive media were considered [18]. Theory of an improved polarization-encoded logic algebra used for the design of an optical gate for a two dimensional data array was introduced in 1995 [19]. That algebra is completely different from the well-established and widely used digital logic [20]. Also, in 1994, implementation of the 16 logic functions of two input patterns based on the birefraction of uniaxial crystals was suggested as an integrated polarization-optical logic processor [21]. In 1996, logic gates based on digital speckle pattern interferometry were introduced as the digital polarization-encoded technique for optical logic gate operations [22]. Shadow-gram based Boolean logic gates were introduced in 1997, and related analysis and evaluations of logical instructions called in parallel digital optical operations based on optical array logic were introduced in 2004 [23,24]. In 2007, an optics inspired logic architecture, which is similar to the Fredkin and Toffoli conservative logic, was introduced [25]. In 2008, ultrafast all-optical logic gates using a nonlinear optical loop mirror based multi-periodic transfer function was introduced, where a complete set of all-optical logic gate operations was reported [26]. In all the published literature, only the horizontal and vertical polarizations are used to represent logic "1" and logic "0", which limits the usefulness of an infinite complex plane to only two points, one at the origin and the other at infinity [27,28]. In the suggested gates, 1) some form of nonlinearity is used, 2) many require special untested algebra that is completely different from the well-known and mature digital logic, 3) many use spatial masks, which drastically reduce the speed of operation of the gates and impede cascading, 4) none uses other than the two vertical and horizontal polarizations, if any, and 5) none carries the polarization representation through to cascading, and on/off representation is defaulted to, which is actually intensity representation, leading to drastically reduced speed of operation.

In two recent publications, we introduced the use of any two orthogonal polarization states of an electromagnetic wave to represent logic "1" (L1) and logic "0" (L0) of two-valued binary logic. We also introduced several design architectures including the ortho-parallel design of any, and all, digital binary gates in which an electro-optic switch was used to input

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the second signal to the gate. The designs were easily cascadable because the information is carried on, and manipulated as, the signal polarization, and not as its intensity [27,28].

In this paper, we introduce the passive all-optical polarization switch, which has two optical inputs and one optical output, in which no electro-optic element is used and no energy is consumed. We also introduce binary logic gate designs using such a switch and feedforward within the gate itself. The use of feedback leads to the design of sequential logic devices, and we close by a design for an SR (set-reset) Latch.

The all-optical polarization designs of sequential and non-sequential logic devices clearly leads to the all-optical polarization digital processor. Such a processor, as its components, is of a very high speed of operation only determined by the speed of light. This is due to the fact that we are modulating light with light. A bulk device speed is to start at a higher speed than the current 3 GHz speed of semiconductor devices. A chip-size device speed is at a much higher value.

It is important to realize that the components used in the construction of the gates and the optical phenomena employed in their operation are all linear, as defined in the literature. Birefringence, propagation, and superposition are all linear optical processes. Nonlinear optics is usually triggered by high signal intensity and/or involves nonlinear physical phenomena [29–31].

Because the operation of the passive all-optical polarization (PAOP) gates and devices is achieved through routing of the optical signals and manipulation of their polarizations, and because polarization is well theoretically and experimentally developed and understood for more than a hundred years, the operation and performance is guaranteed as explained.

2. Passive all-optical polarization switch

The passive all-optical polarization switch (shown in Fig. 1) has two coherent input signals (X_1 and X_2) and one output signal (Z). In order for the switch to operate as indicated, the two signals must be in time phase. Practically, the simplest way to ensure this condition is to have both signals generated by the same source. The operation of this switch is based on changing or keeping the input polarization state of one signal X_1 depending on the polarization state of a second signal X_2, hence a switch. Therefore, X_2 is a control signal. Keep in mind that the two polarization states represent L0 and L1, and that they are two orthogonal polarization states. For the case of ± 45° polarization states representing the L1 and L0, respectively, we use a horizontal polarizer (HP) in the X_1 input, a vertical polarizer (VP) in the X_2 input, and a beam splitter acting as a beam collector (BC) as shown in Fig. 1(a). The output of the BC (shown by Z in Fig. 1a) is the switch output.

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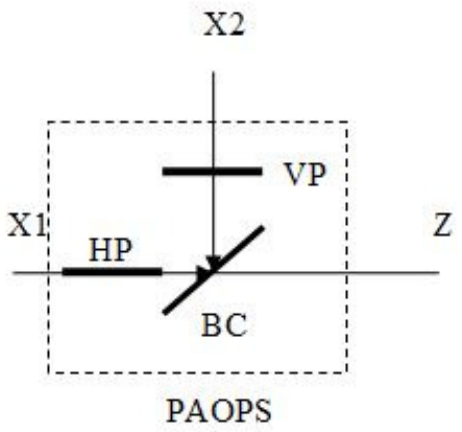
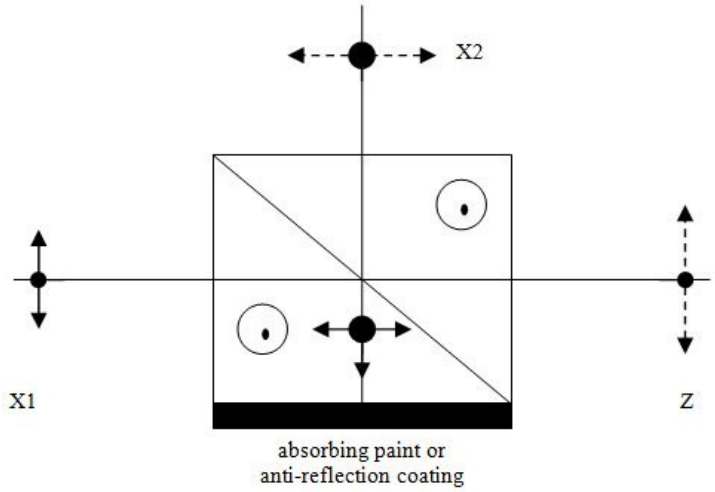


(a)



(b)

Fig. 1. (a) (Media 1) Passive all-optical polarization switch (PAOPS), where X_1 and X_2 are two coherent input signals (of the same source). HP and VP are horizontal and vertical polarizers, and Z is the output signal. (b) (Media 2). A birefringent-polarizer implementation of the passive all-optical polarization switch (PAOPS), where the dot and two-sided-arrow represent the horizontal and vertical components of the input signals (+/− 45°), respectively. The operation of this device is mathematically represented by Eq. (2), where $X_1 = C$ and $X_2 = D$.

Instead of using two input polarizers and a beam splitter, a polarizing beam splitter (PBS) is to be used in an actual implementation as shown in Fig. 1(b). A birefringent polarizer (BP) of the Glan-Foucault (sometimes called Glan-Air) type with or without a Taylor modification, or of the Glan-Thompson type, may be used for that purpose [29,30]. The optic axes of the two prisms are parallel to each other and perpendicular to the page plane, as shown in Fig. 1(b). The two input signals X_1 and X_2 are decomposed into two components one parallel to the optic axis (horizontal-polarization (HP) component) and the other perpendicular to the optic axis (vertical-polarization (VP) component). The HP component of each of the two optical signals goes straight through the device unchanged, and the VP component of each totally internally reflects at the diagonal of the BP. The absorbing paint or anti-reflection coating shown in Fig. 1(b) absorbs the falling optical signal on it, and the BP output Z is an

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optical signal composed of the HP component of the X_1 optical signal and the VP component of the X_2 optical signal. The chip implementation is different and uses waveguides instead. It is discussed in Section 7 as one of four possible technologies.

The operation of the switch is very simple. For the case of X_1 = L0 (–45° polarization state) the output is: 1) Z = L1 (+45°) for X_2 = L1, and 2) Z = L0 for X_2 = L0. That is a 0°/180° switch activated by an L0/L1 control signal [27,28]. On the other hand, if the negation of the output is required (180°/0° switch) the output signal is simply inverted using a 180° retarder R (HWP), or by negating the two inputs. The input/output signals are X_1/Z and the control signal is X_2. For the case 1) above, as the X_1 signal goes through HP, only its horizontal component reaches the BC; and as the X_2 signal goes through VP, only its vertical component reaches the BC. The BC combines both components into a +45° output signal polarization: L1. On the other hand, for case 2) the same takes place with an output signal polarization of –45°. It is clear that the vertical component of X_2 determines the polarization state of the output signal Z.

For the other case of X_1 = L1 (+45° polarization state) the output is: 1) Z = L1 (+45°) for X_2 = L1, and 2) Z = L0 for X_2 = L0, which is a 180°/0° switch activated by an L0/L1 control signal. Again, if the negation of the output is required (0°/180°), either the output signal is negated or the two input signals are. Still the input/output signals in this case are X_1/Z, and the control signal is X_2. The operation of the switch is the same as above.

As we discussed above, a properly aligned polarizing beam splitter PBS can replace the three element combination of HP, VP, and BC. The operation of the switch in this case still is as explained in the previous paragraphs. It is important to realize that the switch does not require a power source to operate, hence it is a passive switch. It functions on the signals themselves. It modulates light with light, since the polarization of one signal is changed according to the other signal, hence modulation: polarization modulation. One of the useful applications of the passive all-optical polarization switch is to build binary logic gates, any and all of them. In Section 3, we use the passive all-optical polarization switch to build some of the important gates.

This passive all-optical polarization switch (PAOPS) is equivalent to one of the 16 binary logic gates, the B gate. The switch actually has 8 states, See Table 1. The first 4 states are similar to the known truth table for the B gate. The following 4 states (the meta-states of the switch) are important and essential to the operation of the binary logic gates which are built using this switch and are presented in the following section, see Tables 2 and 3. Accordingly, no free propagator, or direct connection, can take place of the switch as one might be tempted to suggest.

Table 1. Truth Table of the PAOP switch of Fig. 1.

X_1	0	0	1	1	-	-	0	1	-
X_2	0	1	0	1	0	1	-	-	-
Z	0	1	0	1	↓	↑	→	→	-

We define the switching speed as the reciprocal of the propagation delay, as defined in microelectronics. Accordingly, we can compare the two technologies together. The propagation delay is defined as the time between the signal appearing on the input side and the signal showing on the output side: 50% of signal amplitude is used for delay measurements. Based on this definition, the shorter the signal travels in the PAOPS, the faster the switch speed is. In free space, a one millimeter switch operates at 300 GHz, and a 10 micron switch operates at 30 THz. These speeds are several orders of magnitude faster than the fastest semiconductor technology of today.

3. Passive all-optical polarization binary logic gates

Figure 2 shows one possible construction of a passive all-optical polarization AND gate. Two polarizing beam splitters PBS_1 and PBS_2 that are adjusted to direct polarized input beams of polarizations ± 45° into two separate branches (as shown schematically in Fig. 2) are used. In

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addition, two passive all-optical polarization switches ($PAOPS_1$ and $PAOPS_2$) are used to switch the respective beam polarizations as needed with outputs D and F, respectively. The inputs to $PAOPS_1$ are X_1 and X_2, and the output is D, which is composed of the HP component of X_1 and the VP component of X_2 as discussed in Section 2. Similarly, the inputs to $PAOPS_2$ are X_1' and X_2', and the output is F, which is composed of the HP component of X_1' and the VP component of X_2'. The inputs to the overall gate are signals A and B, and the output is a single beam obtained by using a beam splitter as a beam collector BC to collect Out_1 and Out_2 of Fig. 2. That BC is not shown in Fig. 2 for clarity.

The operation of the gate is straightforward. Table 2 gives the polarization state of the beams as they travel through the gate including the two input signal beams A and B, and the two output signals Out_1 and Out_2, where only one is active at a time, and both are never active simultaneously. Therefore, the BC output, which is the gate output, is composed of either Out_1 or Out_2. A polarizer P in the path of Out_1 is fixed at + 45°. Note that the combination of a beam splitter and the two ±45° polarizers (e.g. BS_1, +45° P, and –45° P) is replaced by a polarizing beam splitter (PBS) for practical implementation. With proper orientation of the polarization of the input signals to the two polarization axes of the PBS, each signal is routed in its totality to the proper corresponding branch. In such a case, the intensity of the output signal is equal to that of the input signal. Here we prefer to use the combination of BS and 2P's for better understanding of the gate operation. It is assumed here that the PBS is lossless. All polarizers are assumed to be ideal (zero loss in the desired polarization and perfect absorption of the undesired one).

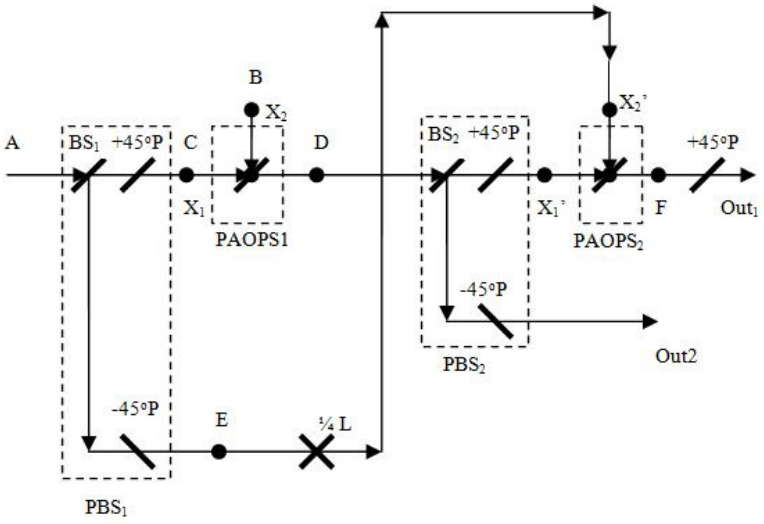

Fig. 2. Passive all-optical polarization AND (PAOP AND) gate. (Media 3) A and B are the two coherent input signals. $Out_1$and Out_2 combined by abeam collector to give the output signal. PBS is a polarization beamsplitter, BS is a beamsplitter, P is a polarizer, L is an attenuator, and PAOPS is a passive all-optical polarization switch (see Fig. 1).

To understand the operation of the logic gate shown in Fig. 2, we consider a case when both inputs A and B are of – 45° linear polarization (representing L0). For this choice of input polarizations, there is no signal at point C, and all of signal A is routed to point E. Therefore, the beam at point E has a polarization of – 45° with the full input beam intensity I_o. An attenuator is placed after point E to attenuate the signal intensity to one quarter of the input signal intensity (i. e., $I_o/4$). That attenuated signal reaches input X_2' of the $PAOPS_2$ leading to Out_1 signal. The two inputs to $PAOPS_1$ are $X_1 = C = 0$ and $X_2 = B$, which is the second input signal beam. The output of $PAOPS_1$ at point D is therefore the vertical component of signal B, which is the vertical component of a –45° polarized beam of intensity $I = I_o$: at D the intensity is therefore $I_D = I_o/2$. This signal travels to the PBS_2 (BS_2 and two ±45°P combination) and

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passes through as a + 45° polarized beam into the upper branch with an intensity of $I_o/4$ and a – 45° polarized beam into the lower branch with an intensity of $I_o/4$ also. The + 45° component inputs to $PAOPS_2$ through X_1' (the HP input). Therefore, the output of $PAOPS_2$ is a beam of –45° polarization which is then crossed by the output polarizer. Accordingly, Out_1 = 0, and no signal exists in that output branch. The – 45° component exits the gate at Out_2 with an intensity of $I_o/4$ and is collected by the output BC. The output is, therefore, L0. Accordingly, the first row of Table 2 represents the first row of an AND gate: A B Z / 0 0 0, where Z is the gate output signal. The performance of the gate represented in the second row of Table 2 is similar to the explanation of the first row just discussed.

Table 2. Operation table of a PAOP AND gate showing the polarization state of the signal beam at different points through the gate, see Fig. 2. The output signal intensity I_{out} is also shown, as a ratio of the input intensity I_o, for the 4 logic states of the gate. The polarization of the output signal of the gate Z is given, which is the output of a beam collector (BC) collecting the two signals Out_1 and Out_2 (not shown in Fig. 2)

A	B	C	D	E	F	Out_1	Out_2	I_{out}	Z	A	B	Z
–45	–45	0	↓	–45	–45	0	–45	$I_o/4$	–45	0	0	0
–45	+45	0	↑	–45	–45	0	–45	$I_o/4$	–45	0	1	0
+45	–45	+45	–45	0	0	0	–45	I_o	–45	1	0	0
+45	+45	+45	+45	0	→	+45	0	$I_o/4$	+45	1	1	1

For the case of an A input of L1 (i. e., + 45°) polarization, that input beam is directed to the upper branch. Therefore, the signal beam at point C is of a + 45° polarization and an intensity of I_o, that of the input beam A. The lower branch receives no signal by PBS_1 and no signal exists at point E or the X_2' input to $PAOPS_2$. The signal beam of point C inputs $PAOPS_1$ at input X_1' (HP input) and the input signal B of a – 45° polarization (L0) inputs $PAOPS_1$ at input X_2 (VP input). The signal at point D is the output signal of $PAOPS_1$ and is, therefore, a – 45° signal of intensity $I = I_o$, that of the input beam. Signal D now is directed by PBS_2 into the lower branch, Out_2, and exits the gate through the BC at the output, which is not shown in Fig. 2. Accordingly, the output beam is of a - 45° polarization and intensity I_o. The upper branch at PBS_2 receives no signal, and accordingly the X_1' input of $PAOPS_2$ receives no signal. Therefore, as both the two inputs of $PAOPS_2$ receive no signal, Out_1 will carry no signal, and only Out_2 is active. In this case, the two inputs to the gate A and B are L1 and L0, respectively, and the output is L0, which is the third row of Table 2. The fourth row of Table 2 can simply be understood in a similar way as row 3.

From Table 2, it is clear that the structure shown in Fig. 2 is an AND gate. It is also clear that the intensity of the gate output signal is not equal in all four input combinations: $I_o/4$, $I_o/4$, I_o, $I_o/4$, respectively. Therefore, for cascading purposes: 1) an optical amplifier, saturating at I_o, is to be used at the output to bring all to the same intensity of I_o, 2) a 4X optical amplifier is to be used within the gate to bring all to I_o, 3) a ¼ attenuator is to be used within the gate to continue to use the gate as a passive device, with no power source required; as discussed in Section 5. Finally, a NAND gate can be obtained from the AND gate discussed above by simply adding a 180° retarder (HWP) in the gate output: after the output BC.

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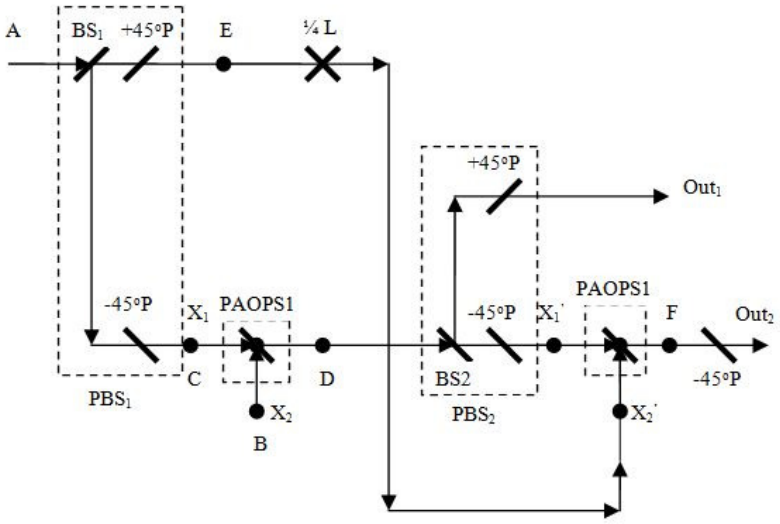

Fig. 3. Same as in Fig. 2, but for a passive all-optical polarization (PAOP) OR gate, see Table 3.

Table 3. Same as in Table 2, but for a PAOP OR gate, see Fig. 3.

A	B	C	D	E	F	Out_1	Out_2	I_{out}	Z	A	B	Z
–45	–45	–45	–45	0	↓	0	–45	$I_o/4$	–45	0	0	0
–45	+45	–45	+45	0	0	+45	0	I_o	+45	0	1	1
+45	–45	0	↓	+45	+45	+45	0	$I_o/4$	+45	1	0	1
+45	+45	0	↑	+45	+45	+45	0	$I_o/4$	+45	1	1	1

Figure 3 and Table 3 show the construction and operation of an OR gate. Clearly, a NOR gate is formed by adding a retarder to the output of an OR gate. Figures 4 and 5 give direct independent designs of NAND and NOR gates, which includes two retarders within the gate itself in each design. As an example, to understand the operation of the logic gate shown in Fig. 4 (PAOP NAND), we consider a case where both inputs A and B are of – 45° linear polarization (representing L0). For this choice of input polarizations there is no signal at point C, and all of signal A is routed to point E. Therefore, the beam at point E has a polarization of – 45° with the full input beam intensity I_o. An attenuator is placed after point E to attenuate the signal intensity to one quarter of the input signal intensity (i.e., $I_o/4$). The polarization of this attenuated signal is transformed to + 45° by passing through the retarder R (e.g., a HWP) and reaches input X_2' of the $PAOPS_2$. The two inputs to $PAOPS_1$ are $X_1 = C = 0$ and $X_2 = B$, which is the second input signal beam. The output of $PAOPS_1$ at point D is therefore the vertical component of signal B, which is the vertical component of a –45° polarized beam of intensity $I = I_o$: at D the intensity is therefore $I_D = I_o/2$. The polarization of this signal is changed to the vertical component of a + 45° by passing through R. It then travels to the PBS_2 (BS_2 and two ± 45°P combination) and passes through as a + 45° polarized beam into the upper branch with an intensity of $I_o/4$ as $Output_1$, and as a – 45° polarized beam into the lower branch with an intensity of $I_o/4$, also. The - 45° component inputs to $PAOPS_2$ through X_1' (the HP input). Therefore, the output of $PAOPS_2$ is a beam of + 45° polarization which is then crossed by the output polarizer; remember that the input to X_2' is a + 45° polarized signal of $I_o/4$ intensity as discussed above. Accordingly, $Out_2 = 0$, and no signal exists in that output branch. The + 45° component exits the gate at Out_1 with an intensity of $I_o/4$ and is collected by the output BC. The output is, therefore, L1. Accordingly, the first row of a NAND gate is satisfied: A B Z / 0 0 1, where Z is the gate output signal. Similarly, the other three rows of the NAND gate are satisfied.

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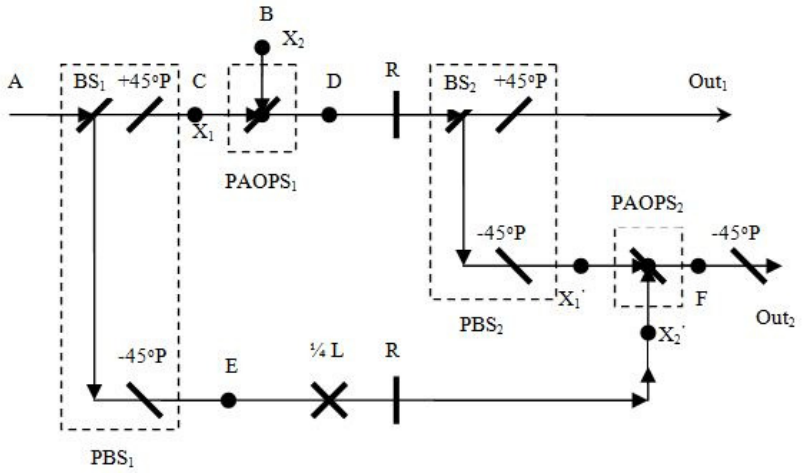

Fig. 4. Same as in Fig. 2, but for a passive all-optical polarization (PAOP) NAND gate, where R is a 180° retarder (e.g., a half-wave plate: HWP).

It is important to note that the gates action is achieved through propagation of the beams within the gate construction and that control of the gate is achieved through beam interaction: light is modulated with light. Also, the operation of the gates does not depend on the wavelength, and gates can be designed and operated at any desired frequency, as long as polarizers and beam splitters, or birefringent polarizers, at the desired wavelength exist.

It is also important to realize that the gate does not require a power source to operate. The operation is achieved through routing of the beam, and the use of a switch and a polarizing element that does not require power to operate, neither. See Section 5 for cascading considerations.

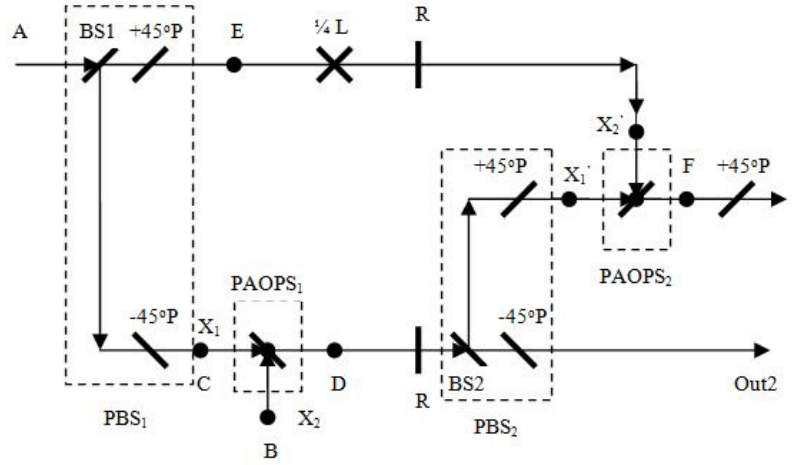

Fig. 5. Same as in Fig. 2, but for a passive all-optical polarization (PAOP) NOR gate.

Because of the use of light modulation using light, and due to the fact that there are no electro-optic devices used in the designs, the speed of operation of all gates is only limited by the speed of light which determines the propagation delay. A bulk gate would, therefore, operate at a speed well above the current 3 GHz speed of microelectronics. A chip-size gate would operate at a much higher speed since the distances travelled by the signal within the gate are much smaller in this case, leading to much smaller propagation delays, and accordingly to much higher speeds of operation.

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The feedforward used in the design, and feedback as shown in Section 6, allow direct design of sequential and non-sequential devices such as latches and flip flops. In addition, passive and non-passive AOP binary logic gates discussed in this and the following sections can be used for that purpose, using the well-developed regular digital design concepts already in use today for semiconductor devices.

4. Jones calculus

Jones Calculus was introduced in the early 1940s to simplify dealing with polarized waves and polarization devices [32,33]. In this section, we give the Jones Calculus analysis of the AND gate of Fig. 2 as an example. The input signals A and B are represented by the two vectors

$$A = \begin{bmatrix} 1 \\ \pm 1 \end{bmatrix}, B = \begin{bmatrix} 1 \\ \pm 1 \end{bmatrix}, \tag{1}$$

where + 1and – 1are for +45° and −45° linearly polarized signals, respectively. PAOPS1 is represented by the matrix equation

$$D = \begin{bmatrix} 1 & 0 \\ 0 & 0 \end{bmatrix} C + \begin{bmatrix} 0 & 0 \\ 0 & 1 \end{bmatrix} B, \tag{2}$$

and the attenuator is represented by

$$\frac{1}{4} L = \frac{1}{2}. \tag{3}$$

The + 45°P in Out_1 is represented by

$$\frac{1}{2} \begin{bmatrix} 1 & 1 \\ 1 & 1 \end{bmatrix}, \tag{4}$$

where the ½ factor is to normalize the relative intensity of the signal. The polarization state of the signal at different points along the gate are given by

$$(C, D, E) = \left(P_{+45} A, P_H C + P_V B, P_{-45} A\right), \tag{5a}$$

$$\left(X_1^{'}, X_2^{'}, F\right) = \left(P_{+45} D, \frac{1}{2} E, P_H X_1^{'} + P_V X_2^{'}\right), \tag{5b}$$

and

$$\left(Out_1, Out_2, Out\right) = \left(P_{+45} F, P_{-45} D, Out_1 + Out_2\right). \tag{5c}$$

Obviously, one can obtain a single vector representation for the output signal, but would lose the polarization information of the signal as it propagates through the gate.

Now, for the case of A = L0 and B = L0, we write

$$C = \frac{1}{2} \begin{bmatrix} 1 & 1 \\ 1 & 1 \end{bmatrix} \begin{bmatrix} 1 \\ -1 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}, \tag{6}$$

$$E = \frac{1}{2} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} 1 \\ -1 \end{bmatrix} = \begin{bmatrix} 1 \\ -1 \end{bmatrix}, \tag{7}$$

and from Eq. (2), we get

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$$D = \begin{bmatrix} 1 & 0 \\ 0 & 0 \end{bmatrix}\begin{bmatrix} 0 \\ 0 \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & 1 \end{bmatrix}\begin{bmatrix} 1 \\ -1 \end{bmatrix} = \begin{bmatrix} 0 \\ -1 \end{bmatrix}. \quad (8)$$

Therefore,

$$X_1^{'} = \frac{1}{2}\begin{bmatrix} 1 & 1 \\ 1 & 1 \end{bmatrix}\begin{bmatrix} 0 \\ -1 \end{bmatrix} = \frac{1}{2}\begin{bmatrix} -1 \\ -1 \end{bmatrix} = \frac{1}{2}\begin{bmatrix} 1 \\ 1 \end{bmatrix}. \quad (9)$$

Note that the two vectors [-1 -1] and [1 1] both represent a +45° linearly polarized signal. The control input to PAOPS2 is now calculated as

$$X_2^{'} = \frac{1}{2}\begin{bmatrix} 1 \\ -1 \end{bmatrix}, \quad (10)$$

and, the output becomes

$$F = \begin{bmatrix} 1 & 0 \\ 0 & 0 \end{bmatrix}\frac{1}{2}\begin{bmatrix} 1 \\ 1 \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & 1 \end{bmatrix}\frac{1}{2}\begin{bmatrix} 1 \\ -1 \end{bmatrix} = \frac{1}{2}\begin{bmatrix} 1 \\ -1 \end{bmatrix}. \quad (11)$$

Note that this output depends on the fact that the two input signals to $PAOPS_2$ are from the same source and that proper tuning of both signals travel paths is done. Accordingly, Out_1 is given by

$$Out_1 = \frac{1}{2}\begin{bmatrix} 1 & 1 \\ 1 & 1 \end{bmatrix}\frac{1}{2}\begin{bmatrix} 1 \\ -1 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}. \quad (12)$$

Out_2 is given by

$$Out_2 = \frac{1}{2}\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix}\begin{bmatrix} 0 \\ -1 \end{bmatrix} = \frac{1}{2}\begin{bmatrix} 1 \\ -1 \end{bmatrix}. \quad (13)$$

From Eq. (13), we conclude that the output of the gate is L0, and that the intensity of the output signal is ¼ the input signal. The case we just discussed is given in the first row of Table 2. The rest of the table is easily obtained by using the proper representation of the input signals A and B. Also, all other gates can be similarly analyzed using Jones Calculus.

5. Cascading

It is important to recognize that the two input signals to each logic gate described here, are of the same intensity I_o. From the operation tables of the AND and OR gates, (Tables 2 and 3, respectively) we see that the output intensity is not equal in the four states of the gate. Accordingly, for cascading purposes, we either make the output signal intensity equal to I_o for the four states, or make sure that the input signals to the gate, two or more, are of the same intensity I_o. This can be achieved using several approaches. Figure 6 provides one possible solution. We use the output of a properly designed attenuator to feedforward ¾ of the signal at that point to Out_2, which renders that signal in the corresponding three gate states to I_o [32]. The output signal of the fourth state, of the last row of Table 2 for the AND gate, is brought to an intensity of I_o by a 4X amplifier, as shown in Fig. 6. With that simple modification to the gate design, we now have the output intensity equal to the input intensity, neglecting any minute losses within the gate. Obviously, this solution requires power input to the gate, and the gate is not passive anymore. The 4X amplifier works only in the one case represented by the last row of Table 2, where both inputs to the gate are L1.

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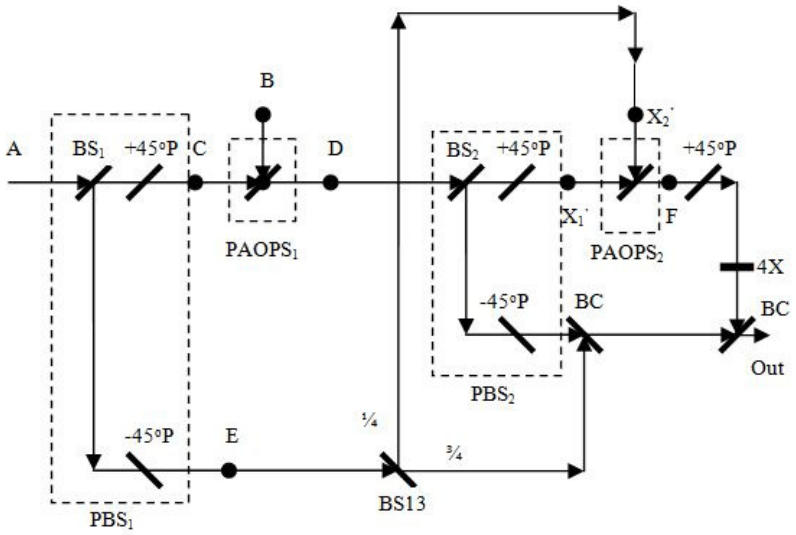

Fig. 6. Same as in Fig. 2, but for an all-optical polarization (AOP) AND gate with an output signal of the same intensity as that of the input signals. X is an amplifier, BC is a beam collector, and BS_{13} is a ¼ and ¾ beam splitter, which is easily implemented using a polarization preserving device (PPD) [43].

A second possible solution is to use a saturation amplifier in the output of the gate to bring the intensity to I_o. In this case, the gate requires more power to compensate for the power lost in the I/4 attenuator (see Fig. 2, for example). In this case, the saturation amplifier works in three of the four possible cases of operation of the gate. Another (similar but less economical) possible solution is to use two saturation amplifiers in the input beams to the gate to make sure that the input signals are of intensity I_o. Those solutions are presented just to show the simplicity of cascading. The use of amplifiers requires a power source. Regardless, a passive gate design that provides for cascading is to use an attenuator in Out_2, instead of an amplifier for Out_1, which requires no power source to operate. The gate output intensity is, therefore, reduced at each and every level of logic gates to $I_o/4$. If we start with a high input power, and the output power is reduced to one fourth the input power, we need to make sure in our digital design that the input to each and every gate is of the same power intensity by properly keeping track of the power level at every logic-design level (depth of the design). That is fine, since the intensity holds no information, and all information is in the polarization of the wave. Therefore, in this case the polarization signal-to-noise ratio (PSNR) would be used to compare the desired signal polarization to the background noise, instead of the traditional SNR which involves the intensity instead.

6. All-optical polarization digital processor

The possibility for the implementation of an all-optical polarization digital processor is evident at this point of discussion. The required memory element is easily achieved using a flip-flop device, which is a straightforward application of the discussions of Sections 3 and 5 above. Figure 7 shows an all-optical polarization SR Latch. SR Latches are the most popular digital sequential devices used to realize memories in digital designs. Following the operation of different gates discussed in Section 3, and using any of the cascading designs discussed in Section 5, one can easily follow the operation of the AOP SR Latch of Fig. 7, which is composed of two cross-coupled NOR gates. Note that a 2X amplifier is added right before the exit BC to provide a signal of intensity I_o for both feedback and gate outputs. Also, note that the two inputs are S for set and R for reset, and the two outputs are Q and Q', which is the negation of Q. When S and R are both L1, the output state is undefined, as in any SR Latch [20].

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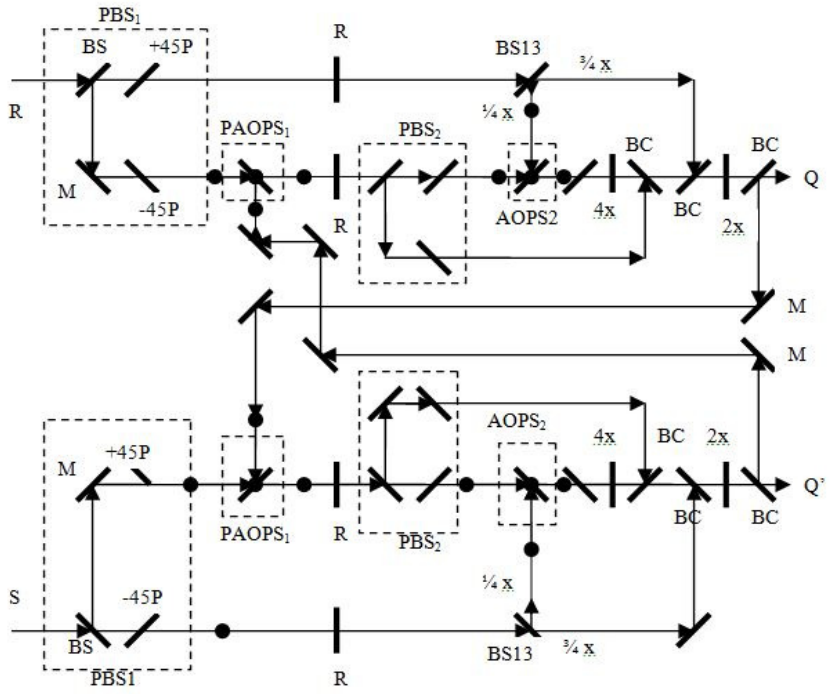

Fig. 7. All-optical polarization (AOP) set/rest (SR) Latch: two cross-connected all-optical polarization (AOP) NOR gates, see Fig. 5.

Clearly, AOP S'R' Latches are similarly designed using two AOP NAND gates. Also, AOP SR Latches with control input using 4 AOP NAND gates, and AOP D Latches using 4 AOP NAND gates and one AOP INV gate, are similarly implemented. In addition, the more complicated master-slave flip-fop, and all other digital devices (sequential or non-sequential), can all be similarly designed and implemented.

7. Implementation

Four technologies are currently available to implement the proposed design of the passive all-optical gates and devices: free space, fiber optics, photonic integrated circuits (PICs), and silicon photonics. Free space technology uses well established manufacturing tools to produce the needed optical components. Usually, the free space proof-of-concept prototypes are bulky and table-top mounted, with possibilities for miniaturization [29,34,35]. Fiber optics is a well-established industry for telecommunications applications, with plenty of readily available off-the-shelf components that could be used for implementing our prototypes [36]. The components could be easily mounted on a board to yield a portable device. PICs and silicon photonics are two chip-size technologies that are well developed to mass produce sub-millimeter-, micro-, and nano-scale products [37,38]. These two technologies are expensive and involve many industry-specific considerations including process-flow and mask design and manufacturing.

We can see that the experimental implementation of the suggested gates is straightforward with normal engineering considerations that depend on the technology to be used. If we consider implementation of any of the gates using silicon photonics, we see that all building blocks are available for prototyping, followed by manufacturing [38]. That includes waveguides to maintain polarization [39]. In addition, a polarization gate is reported in the literature [40,41]. We also need to keep in mind that the gates are polarization self-correcting. Note that there is a +45° linear polarizer in Out_1, and we can add a –45° linear polarizer in

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Out_2 if needed. That way, the output of the gate is always self-corrected. Also, there is no need to use mirrors, and they are only included to simplify the figures, see Figs. 2-7. A silicon photonics fabrication estimate for the length of the AND gate design of Fig. 2 is between 300 microns and 1 mm. That leads to a gate speed of 206 GHz to 685 GHz.

Industrially, there are many parameters available to control the implementation to preserve the polarization fidelity of the signal. That is equally valid for devices and waveguides, in addition to controlling the path length itself. Obviously, tuning is critical and is done at the prototype stage to reach a mask suitable for mass production. Also, material dispersion is one of the factors on which the wavelength bandwidth of the gate is determined. Keep in mind that no two signals pass through the same branch unless they have already been combined in a BC. Therefore, no interference would take place within the gate. In general, this discussion on implementation holds for the other technologies, too.

We propose to implement our optical circuits in a two-phase plan. First, all the needed components are fabricated side by side and independently tested to verify the fabrication processes. Second, the components are arranged in the required sequence and connections are adjusted (tuned) to give the expected output. For mass production, the mask is accordingly finalized and fabricated.

Clearly, the ultimate speed of operation of PAOP gates and circuits will be determined by the switching speed of the input signals. This field of research is moving fast towards very high speeds. Reference [42] reports experimental verification of a 26 Tbps (terra bits per second) switching speed using a single laser source. We expect improvements on such speeds in the near future.

8. Conclusions

In this paper we introduced the passive all-optical polarization switch (PAOPS), which employs no electro-optic element and no moving parts. Its input is an optical signal with ± 45° linear polarization, its control signal is an optical signal of either + 45° or – 45° polarization, and its output is an optical signal of either + 45° or – 45° polarization depending on the polarization of the input and control signals. Accordingly, the switch is modulating light with light. We used the PAOPS to design all-optical polarization (AOP) and PAOP binary logic gates using feedforward. The operation of a passive gate does not require a power source, and the speed is very high: well above 10 GHz for bulk implementation and much higher speeds for chip-size implementation. We presented and discussed the design and operation of PAOP AND and PAOP OR gates in details, as well as that for the two important global PAOP NAND and PAOP NOR gates. In addition, we discussed cascading with reduced intensity per logic gate level (passive gates) and with non-reduced intensity (non-passive gates) using simple and direct designs. We also presented, and briefly discussed, the AOP SR Latch using two cross-coupled NOR gates. Clearly, the introduced architecture can be used to design any and all sequential and non-sequential logic devices using the available wealth of digital design. With the most popular device used today for memory in digital logic, designed and implemented as an AOP device, the required components of a digital processor are completed.

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