Enabling Visual Communication

LEADIS®

LDS285

Data Sheet

720 Source (240 x RGB) + 320 Gate
16M-Color One-Chip TFT Driver

Feb. 27, 2007 PRELIMINARY

CONTENTS

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REVISION HISTORY

Date	Contents	Version
Oct. 17, 2006	- Preliminary Version 0.00.	Ver. 0.00 (Preliminary)
Feb. 1, 2007	Totally revised	Ver. 1.00 (Preliminary)
Mar. 1, 2007	Command , EEPROM and DBC description	Ver. 2.00 (Preliminary)

1 DESCRIPTION

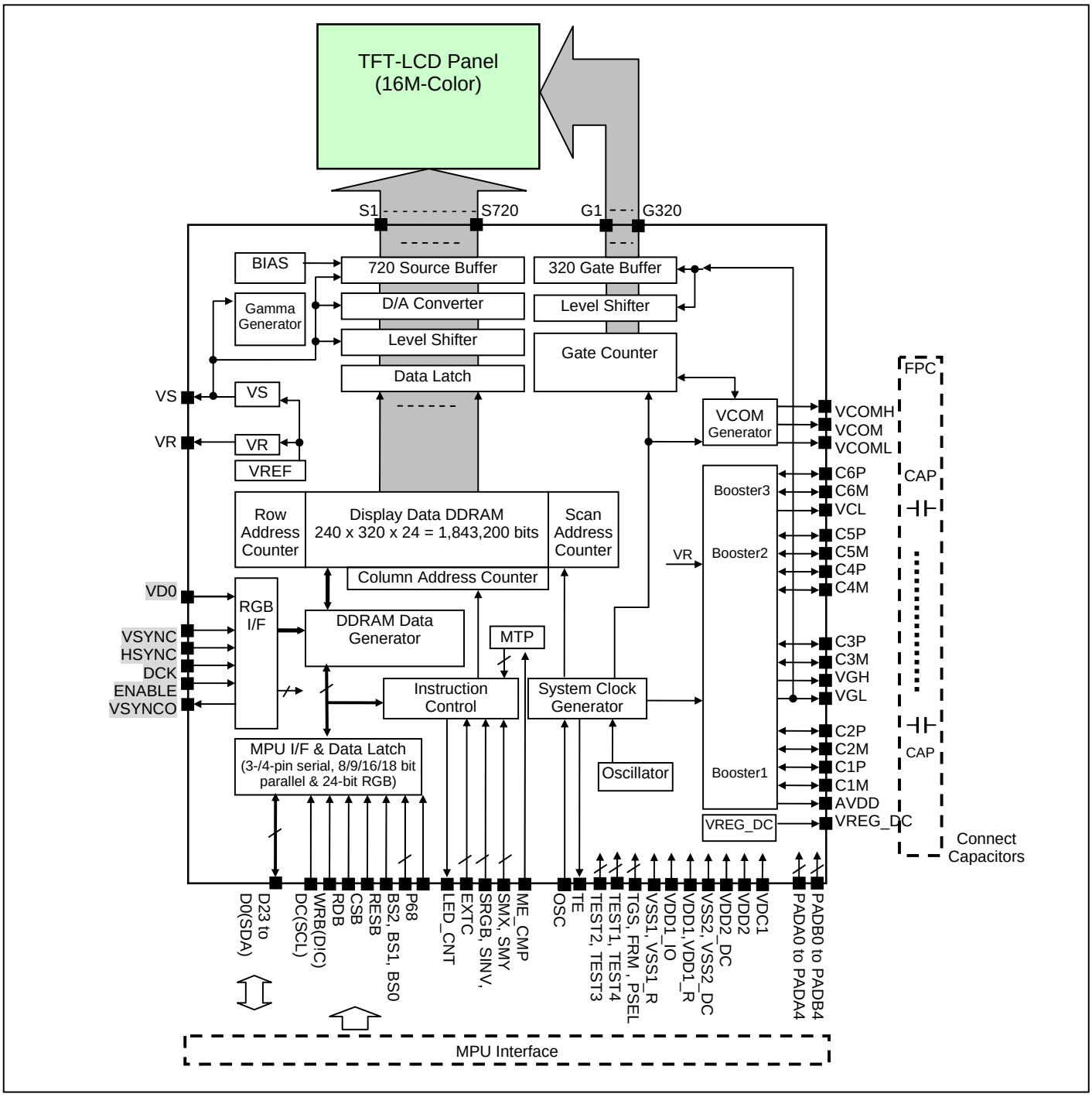
LDS285 is a single chip low power CMOS LCD controller/driver for color TFT-LCD displays of 320 gates and 240xRGB columns. It has a 1.84M-bit (240 x 24bit x 320) display RAM and a full set of control functions. LDS285 offers 10 kinds microprocessor interfaces: 8080-system (8-bit, 9-bit, 16-bit, 18-bit), 6800-system (8-bit, 9-bit, 16-bit, 18-bit) and serial (3-pin or 4-pin). It also supplies 24-bit or 8-bit RGB interface for driving Video signal directly from controller.

2 FEATURES

- Single chip TFT-LCD controller/driver
- Outputs:
  - 720 source outputs (240 x RGB)
  - 320 gate outputs
  - Common electrode output
- Display mode (Color modes):
  - Full colors (Idle mode off): 16M-colors,262K-colors
  - Reduced color (Idle mode on): 8-colors (3-bit binary mode)
- Interface mode (Color modes on the display host interface):
  - 24 bit/pixel: (RGB) = (888) using the 1.84M-bit frame memory directly
  - 18 bit/pixel: (RGB) = (666) using the 1.84M-bit frame memory with 256k-colors
- Display Data RAM (DDRAM): 240 x 320 x 24-bit = 1.84M bit
- MPU Interfaces:
  - 3-pin or 4-pin serial interface
  - 8-bit, 9-bit, 16-bit, 18-bit interface with 8080-series MPU
  - 8-bit, 9-bit, 16-bit, 18-bit interface with 6800-series MPU
  - 24-bit or 8-bit RGB interface with graphic controller
- Display features
  - Partial display mode
  - Software programmable color depth mode
  - N-line inversion for low cross talk
- On chip:
  - DC/DC converter
  - Adjusted VCOM generation by MTP
  - Oscillator for display clock generation.
  - One set of 4 gamma curves with micro-adjustment points
  - Temperature compensation for display quality
- Driving algorithm:
  - Line inversion, frame inversion

- I/O supply voltage range.
  1.65 to 3.3V
- Optional logic supply voltage range
  VDD1 to VSS1 (when PSEL=Low): 1.65 to 1.95V
  VDD1 to VSS1 (when PSEL=High): 1.95 to VDD2
- Analog supply voltage range VDD2 to VSS2:
  2.3 to 3.3V
- Output voltage levels:
  - Source output voltage range VS to VSS2: 3.0 to 6.0 V
  - Common electrode output voltage range Vcom amplitude (max) = 5.5V
  - VcomH output voltage range VcomH to VSS2 2.0 to 5.0V
  - VcomL output voltage range VcomL to VSS2 -2.0 to 1.0V
  - Positive Gate output voltage range: +12.0 to +16.0 V when VR=4
  - Negative Gate output voltage range: -8.0 to –12.0 V when VR=4
- Low power consumption, suitable for battery operated systems
- CMOS compatible inputs
- Optimized layout for COG assembly
- Temperature range: -30 ~ 70°C (to +85°C no damage)
- Support DBC(Dynamic Backlight Control) function and ALS(Ambient light sensing)Function
- Support normal black / normal white LCD
- Support wide view angle display

3 BLOCK DIAGRAM



4 PIN DESCRIPTION

Table 4.1.1 Pin Description

Name	Type	Description
Driver output pins		
S1 to S720	O	Source driver output pins.
G1 to G320	O	Gate driver output pins.
Power supply pins		
PSEL	I	I/O power voltage level selection pin. **When PSEL="VSS2"**: I/O signal voltage should be less than 1.95V and in this case, VDD1_IO and VDD1 should be connected together and external power for I/O system should be supplied to those pins (VDD1_IO and VDD1) **When PSEL="VDD2"**: I/O signal voltage should be larger than 1.95V and in this case, VDD1_IO and VDD1 should not be connected together and external power for I/O system should be supplied to VDD1_IO and VDD1 should have stabilization capacitor (about 2.2uF) to VSS.
VDD1_IO	P	Power supply for I/O circuit system. (Refer PSEL pin description)
VDD1, VDD1_R	P	Power supply for logic system. (Refer PSEL pin description)
VDD2, VDD2_DC	P	Power supply for analog system and boosting input voltage. 2.3V~3.3V supported. All VDD2 and VDD2_DC pins must be externally connected.
VSS1, VSS1_R, VSS2 VSS2_DC	P	System ground for logic and analog circuits. All VSS1,VSS1_R and VSS2,VSS2_DC pins MUST be externally connected to system ground.
D_VDD1O	PO	Dummy VDD1_IO power output pin. It can be used to fix some input pins to "H" level and must be left open if not used.
D_VSS1	PO	Dummy VSS1 power output pin. It can be used to fix some input pins to "L" level and must be left open if not used.
ME_CMP	P	MACRO EEPROM write - erase power. When you write on internal EEPROM you must provide power through this pin and it must be left open when you do not write on EEPROM.

Pin Description (continued)

Name	Type	Description
LCD supply voltage generation (DC-DC converter and Regulator)		
C1P to C6P, C1M to C6M	I/O	Capacitor connection pins for booster circuits.
AVDD	O	Output of booster circuit (2*VDD2 or 3*VREG_DC). Connect capacitor to VSS (GND)
VDC1	I	1st booster reference voltage Using VS<4.2V , VDC1 and VDD2_DC should be connected together Using VS>4.2V , VDC1 and VREG_DC should be connected together
VREG_DC	O	Output of the VREG_DC regulator Connect capacitor between VREG_DC and system ground (GND). Using VS>4.2V , VDC1 and VREG_DC should be connected together
VR	O	Output of the VR regulator. Connect capacitor between VR and system ground (GND).
VS	O	Output of the VS regulator. All VS pads in left side and right side must be connected together by external metal layer for lower resistance. Connect stabilizing capacitor between VS and system ground (GND).
VGH	O	Positive reference voltage for gate driver circuits (3*VR or 4*VR). Please refer to the **5.9.2 Various Boosting Steps** for details
VGL	O	Negative reference voltage for gate driver circuits (-2*VR or -3*VR). Please refer to the **5.9.2 Various Boosting Steps** for details
VCL	O	Negative voltage output of booster circuits for VCOM (-1*VDD2)
VCOMH	O	Positive voltage output of VCOM.
VCOML	O	Negative voltage output of VCOM.
VCOM	O	Common output signal. The swing voltage level is VCOML to VCOMH.

Pin Description (continued)

Name	Type	Description
Host interface pins		
P68,BS2,BS1, BS0	I	Interface mode setting (Please refer to the section 5.1). In the serial interface mode, RGB interface mode can be used by “ENABLE” pin.
RESB	I	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.
CSB (!SCE)	I	Chip select input pin (“Low” enable). This pin can be permanently fixed “Low” in parallel interface mode only. If CSB is connected to ground in Parallel interface mode, there will be no abnormal visible effect to the display module. Also there will be no restriction on using the Parallel Read/Write protocols, Power On/Off Sequences or other functions. Furthermore there will be no influence to the Power Consumption of the display module.
D/!C(SCL)	I	Display data / Command selection pin in parallel interface. In serial I/F, this is used SCL. If not used, please connect to ground or VDD1_IO this pin.
WRB (RW) (D/!C)	I	Write enable in 8080-series parallel interface. Read write selection in 6800-series parallel interface. In serial I/F, this is used D/!C for 4-line serial. If not used, please connect to ground or VDD1_IO this pin.
RDB (E)	I	Read enable in 8080-series parallel interface. Read/write enable in 6800-series parallel interface. If not used, please connect to ground or VDD1_IO this pin.
TE	O	Tearing effect output. If not used, please open this pin.
D23to D8, D7 to D0	I/O	18-Bit bi-directional display data bus for parallel interface with MPU. 16-Bit bi-directional display data bus for parallel interface with MPU. 9-Bit bi-directional display data bus for 9-bit parallel interface. 8-Bit bi-directional display data bus for 8-bit parallel interface. 8-Bit command bus for 18-bit, 16-bit, 9-bit and 8-bit parallel interface. In 8-bit parallel, D7 to D0 are used and the others (D23 to D8) should be connected to VSS1. In 9-bit parallel, D8 to D0 are used and the others (D23 to D9) should be connected to VSS1. In 16-bit parallel, D23 to D16 are not used and should be connected to VSS1. In 18-bit parallel, D23 to D18 are not used and should be connected to VSS1. In serial interface, D23 to D1 are not used and should be let open or connected to VSS1. In only RGB interface, D23 to D18 are used.

Pin Description (continued)

Name	Type	Description
Mode Select		
SRGB	I	Module RGB order select pin. (Refer section 8.2)
SINV	I	Source output data polarity select pin. (SINV=H: Data reverse) (Refer section 8.2)
SMX	I	Module Source output direction select pin. (Refer section 8.2)
SMY	I	Module Gate output direction select pin. (Refer section 8.2)
EXTC	I	Enable pin for extended command set and test command set. To use extended command set and test command set (such as EEPROM WRITE), please connect this pin to VDD1_IO. During normal operation, please open this pin. (Internal Rpull-down=15KΩ)
TGS	I	Enable pin for extended command set. To use extended command and normal command sets only, please connect this to VSS1 and make EXTC connected to VSS1 or open. (The test commands can not be used and are treated as NOPs). To use normal command set only, please connect this to VDD1 and open EXTC.
LED_Control		
LED_CNT	O	Back-light control output. If not used, please open this pin

Pin Description (continued)

Name	Type	Description
Clock input and RGB interface		
OSC	I	Oscillator input for test purpose. If not used, please connect this pin to VSS1
VSYNC	I	Vertical sync input for RGB interface. It used as a start pulse input for the gate driver circuits. If not used, please connect this pin to VSS1.
HSYNC	I	Horizontal sync input for RGB interface. It used as a start pulse input to receive the valid data for the source driver circuits. If not used, please connect this pin to VSS1.
DCK	I	Pixel data clock input for RGB interface. When the RGB interface is used, the dot clock is input. The RGB data of VD17 to VD0 pins are read at the rising edge or falling edge of this signal. If not used, please connect this pin to VSS1.
ENABLE	I	RGB interface enable pin. This pin is used for the RGB data enable signal when RGB interface is used. If not used, please connect this pin to VSS1.
VD0	I	LSB of RGB interface data bus. Since D23~D1 are shared between RGB interface and parallel interface, only VD0 is used. If not used, please connect these pins to VSS1.
VSYNCO	O	RGB interface vertical sync output for RGB interface. If not used, please open this pin.
Test pins		
PADA0 PADB0	I	Pins for display glass break detection. Refer to the section 5.14.4 for details. If not used, please open these pins.
PADA1 to PADA4 PADB1 to PADB4	I	Pins for chip attachment detection. Refer to the section 5.14.3 for details. If not used, please open these pins.
FRM	I	Test input pin. Free Running Mode test. You can use this pin when you do reliability test for your panel. If not used, please open this pin (Internal Rpull-down=15KΩ).
TEST1	O	Test pin, not accessible to user must be left open.
TEST2	I	Test pin, not accessible to user must be left open.
TEST3	I	Test pin, not accessible to user must be left open.
TEST4	O	Test pin, not accessible to user must be left open.
Dummy	-	Dummy pins. These pins can be used for ITO routing.

NOTE: DUMMY – These pins should be open (float).

5 FUNCTIONAL DESCRIPTION

5.1 MPU INTERFACE

LDS285 can interface with MPU at high speed. However, if the interface cycle time is faster than the limit, MPU needs to have dummy wait(s) to meet the cycle time limit.

5.1.1 Interface Type Selection

The selection of a given interfaces are done by setting P68, BS2, BS1 and BS0 pins as shown in ***Table 5.1.1*** and ***Table 5.1.2.***

Table 5.1.1 Interface Type Selection

P68	BS1	BS1	BS0	Interface	Read back select
0	0	0	0	3-Pin Serial Interface	Via the read instruction (8-bit, 24-bit and 32-bit read parameter)
0	0	0	1	8080 MPU 8-bit Parallel	RDB strobe (8-bit read data and 8-bit read parameter)
0	0	1	1	8080 MPU 16-bit Parallel	RDB strobe (16-bit read data and 16-bit read parameter)
0	1	0	0	8080 MPU 9-bit Parallel	RDB strobe (9-bit read data and 8-bit read parameter)
0	1	1	0	8080 MPU 18-bit Parallel	RDB strobe (18-bit read data and 16-bit read parameter)
1	0	0	0	4-Pin Serial Interface	Via the read instruction (8-bit, 24-bit and 32-bit read parameter)
1	0	0	1	6800 MPU 8-bit Parallel	E strobe (8-bit read data and 8-bit read parameter)
1	0	1	1	6800 MPU 16-bit Parallel	E strobe (16-bit read data and 16-bit read parameter)
1	1	0	0	6800 MPU 9-bit Parallel	E strobe (9-bit read data and 8-bit read parameter)
1	1	1	0	6800 MPU 18-bit Parallel	E strobe (18-bit read data and 16-bit read parameter)

Table 5.1.2 Pin Connection according to the Interface Type

P68	BS2	BS1	BS0	Interface	RDB	WRB	DC	D23-D0
0	0	0	0	3-Pin Serial Interface	*1)	*1)	SCL	*1) D23-D1: Unused, D0: SDA
0	0	0	1	8080 MPU 8-bit Parallel	RDB	WRB	DC	*1) D23-D8: Unused, D7-D0: 8-bit Data
0	0	1	1	8080 MPU 16-bit Parallel	RDB	WRB	DC	*1) D23-D16: Unused, D15-D0: 16-bit Data
0	1	0	0	8080 MPU 9-bit Parallel	RDB	WRB	DC	*1) D23-D9: Unused, D8-D0: 9-bit Data
0	1	1	0	8080 MPU 18-bit Parallel	RDB	WRB	DC	*1) D23-D18: Unused, D17-D0: 18-bit Data
1	0	0	0	4-Pin Serial Interface	*1)	DC	SCL	*1) D23-D1: Unused, D0: SDA
1	0	0	1	6800 MPU 8-bit Parallel	E	RW	DC	*1) D23-D8: Unused, D7-D0: 8-bit Data
1	0	1	1	6800 MPU 16-bit Parallel	E	RW	DC	*1) D23-D16: Unused, D15-D0: 16-bit Data
1	1	0	0	6800 MPU 9-bit Parallel	E	RW	DC	*1) D23-D9: Unused, D8-D0: 9-bit Data
1	1	1	0	6800 MPU 18-bit Parallel	E	RW	DC	*1) D23-D18: Unused, D17-D0: 18-bit Data

NOTE: 1) Unused pins can be open, connected to VSS1

5.1.2 General Protocol

For programming of the LCD driver, the general supported protocol is shown in ***Fig. 5.1.1***

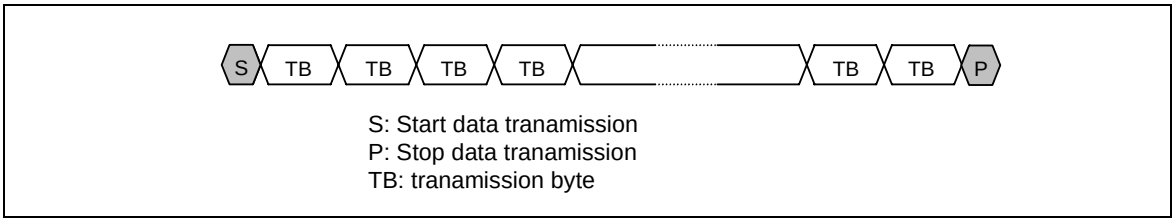


Fig. 5.1.1 Programming protocol

If data write or parameter write is interrupted by any other command, data write command or parameter write command should be done again to write the remained data or parameter.

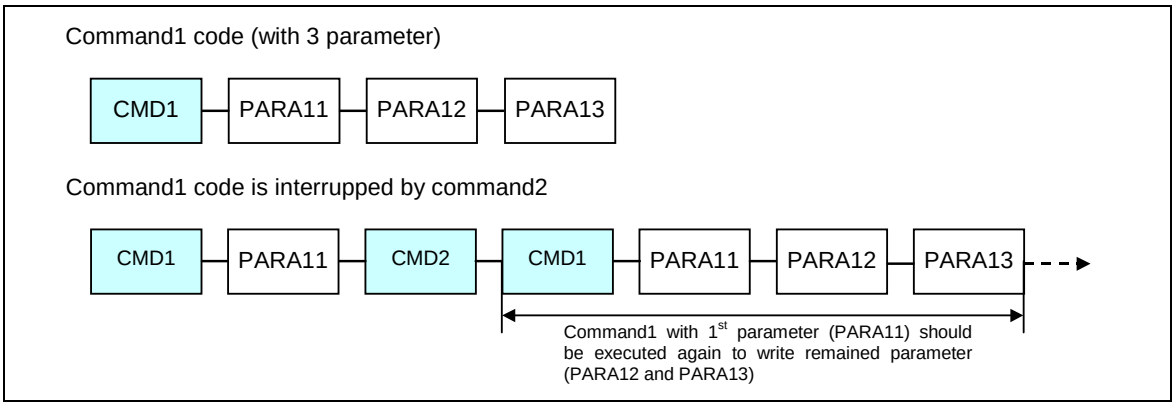


Fig. 5.1.2 Write interrupt sequence

5.1.3 8080-Series Parallel Interface (P68 = "L")

The 8080-series bi-directional interface can be used for communication between the micro controller and the LCD driver chip. The selection of this interface is done when P68 pin is “L” state (VSS1). Interface bus width can be selected with BS2, BS1 and BS0.

The interface functions of the parallel interface (8080-series) are given in ***Table 5.1.3.***

Table 5.1.3 Parallel Interface Function (8080-series, P68=”L”)

BS2	BS1	BS0	Interface	DC	8080-series		Function
					RDB	WRB	
0	0	1	8-bit interface	1	1	↑	Write 8-bit display data or 8-bit parameter (D7 to D0)
				0	1	↑	Write 8-bit command (D7 to D0)
				1	↑	1	Read 8-bit display data (D7 to D0)
				1	↑	1	*1) Read 8-bit parameter or status (D7 to D0)
0	1	1	16-bit interface	1	1	↑	Write 16-bit display data (D15 to D0) or 8-bit parameter (D7 to D0)
				0	1	↑	Write 8-bit command (D7 to D0)
				1	↑	1	Read 16-bit display data (D15 to D0)
				1	↑	1	*1) Read 8-bit parameter or status (D7 to D0)
1	0	0	9-bit interface	1	1	↑	Write 9-bit display data(D8 to D0) or 8-bit parameter (D7 to D0)
				0	1	↑	Write 8-bit command (D7 to D0)
				1	↑	1	Read 9-bit display data (D8 to D0)
				1	↑	1	*1) Read 8-bit parameter or status (D7 to D0)
1	1	0	18-bit interface	1	1	↑	Write 18-bit display data (D17 to D0) or 8-bit parameter (D7 to D0)
				0	1	↑	Write 8-bit command (D7 to D0)
				1	↑	1	Read 18-bit display data (D17 to D0)
				1	↑	1	*1) Read 8-bit parameter or status (D7 to D0)

NOTE: “↑”= rising edge

**1) Applied for command code: DAh, DBh, DCh, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh, 04h and 09h*

The parallel interface timing diagram is given in ***Fig. 5.1.3*** and ***Fig. 5.1.4.***

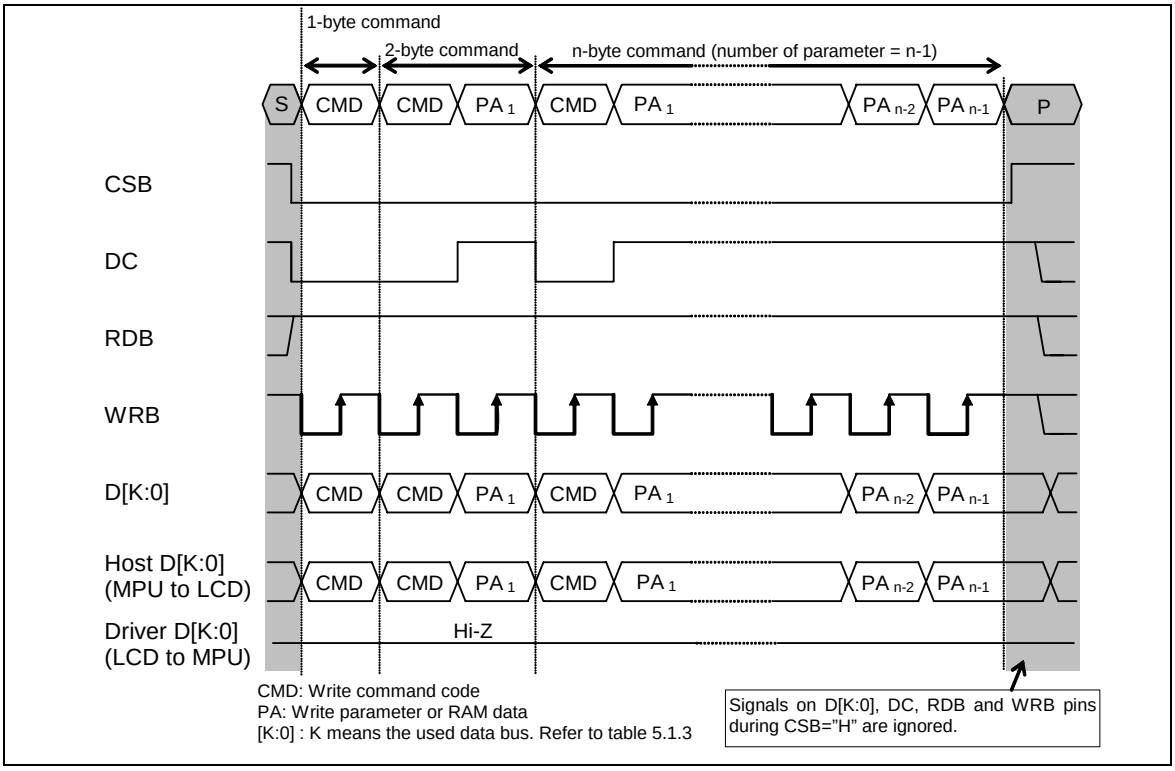


Fig. 5.1.3 8080-Series parallel bus protocol, write to register or display DDRAM

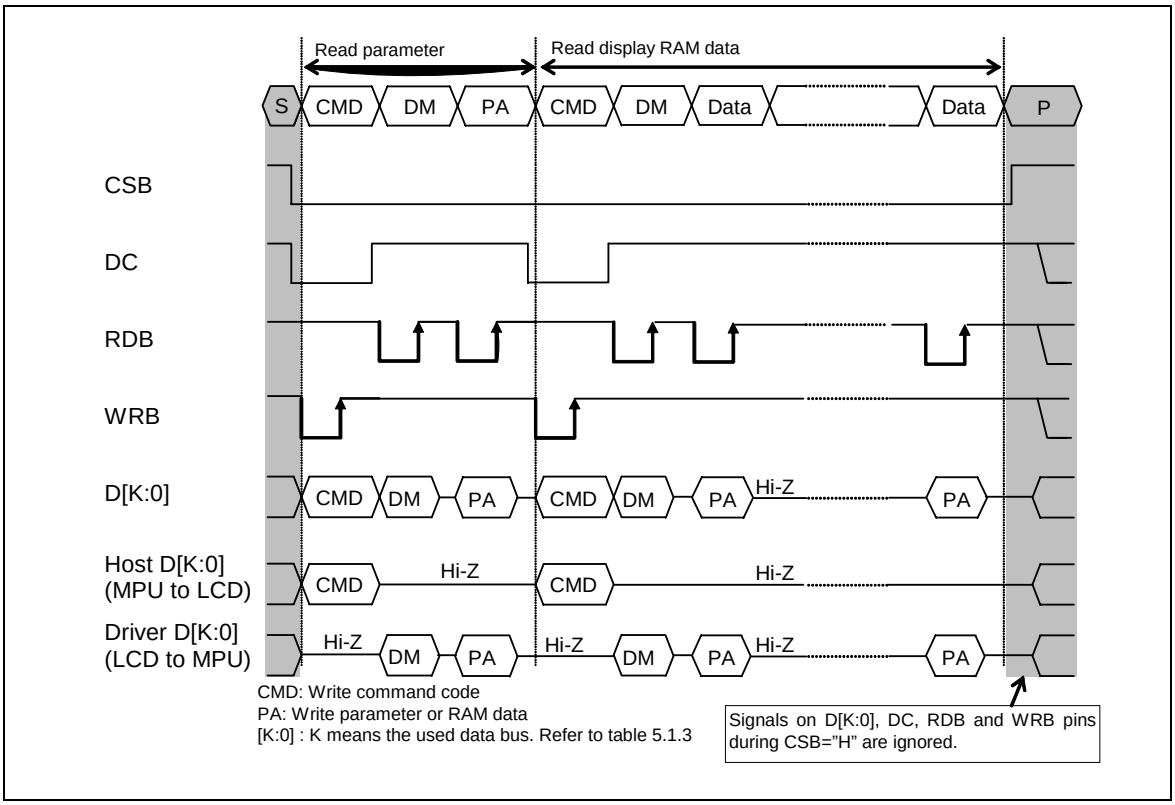


Fig. 5.1.4 8080-Series parallel bus protocol, read from register

5.1.4 6800-Series Parallel Interface (P68 = "H")

The 6800-series bi-directional interface can be used for communication between the micro controller and the LCD driver chip. The selection of this interface is done when P68 pin is “H” state (VDD1_IO). Interface bus width can be selected with BS2, BS1 and BS0.

The interface functions of the parallel interface (6800-series) are given in ***Table 5.1.4.***

Table 5.1.4 Parallel Interface Function (6800-series, P68=”H”)

BS2	BS1	BS0	Interface	DC	6800-series		Function
					RW	E	
0	0	1	8-bit interface	1	0	↓	Write 8-bit display data or 8-bit parameter (D7 to D0)
				0	0	↓	Write 8-bit command (D7 to D0)
				1	1	↓	Read 8-bit display data (D7 to D0)
				1	1	↓	*1) Read 8-bit parameter or status (D7 to D0)
0	1	1	16-bit interface	1	0	↓	Write 16-bit display data (D15 to D0) or 8-bit parameter (D7 to D0)
				0	0	↓	Write 8-bit command (D7 to D0)
				1	1	↓	Read 16-bit display data (D15 to D0)
				1	1	↓	*1) Read 8-bit parameter or status (D7 to D0)
1	0	0	9-bit interface	1	0	↓	Write 9-bit display(D8 to D0) data or 8-bit parameter (D7 to D0)
				0	0	↓	Write 8-bit command (D7 to D0)
				1	1	↓	Read 9-bit display data (D8 to D0)
				1	1	↓	*1) Read 8-bit parameter or status (D7 to D0)
1	1	0	18-bit interface	1	0	↓	Write 18-bit display data (D17 to D0) or 8-bit parameter (D7 to D0)
				0	0	↓	Write 8-bit command (D7 to D0)
				1	1	↓	Read 18-bit display data (D17 to D0)
				1	1	↓	*1) Read 8-bit parameter or status (D7 to D0)

NOTE: “↓”= falling edge

**1) Applied for command code: DAh, DBh, DCh, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh, 04h and 09h*

The parallel interface timing diagram is given in ***Fig. 5.1.5*** and ***Fig. 5.1.6.***

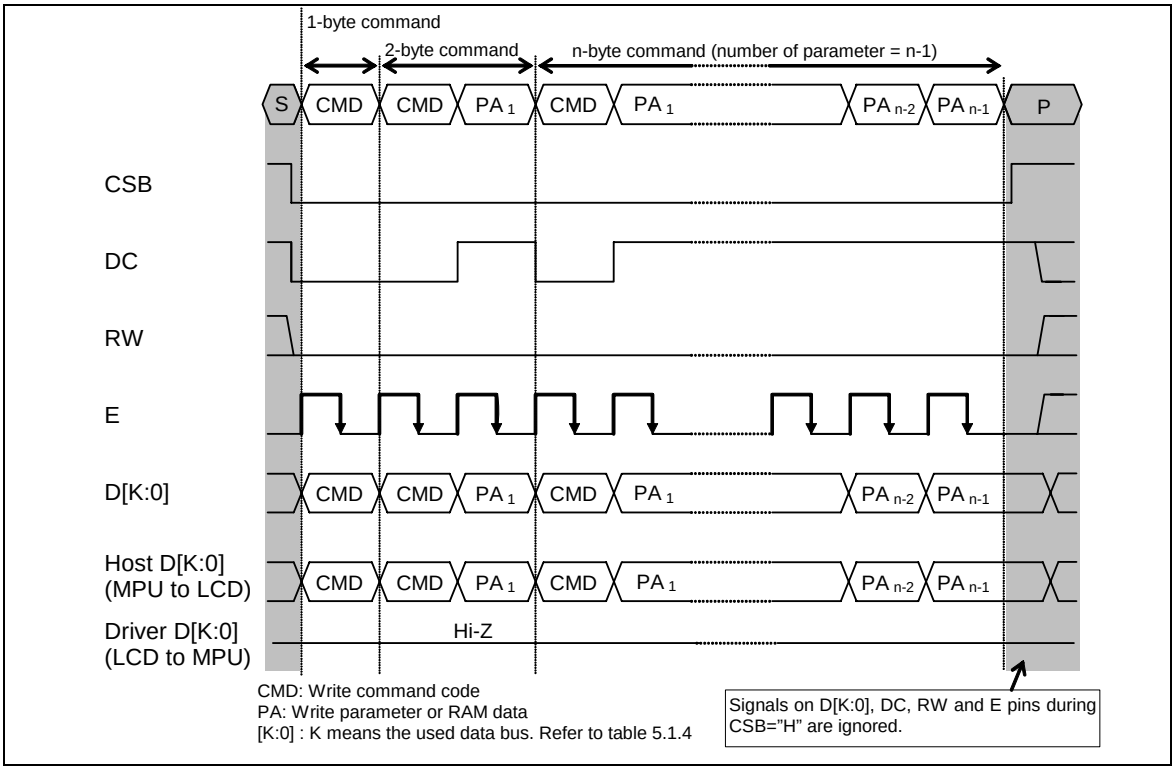


Fig. 5.1.5 6800-Series parallel bus protocol, write to register or display DDRAM

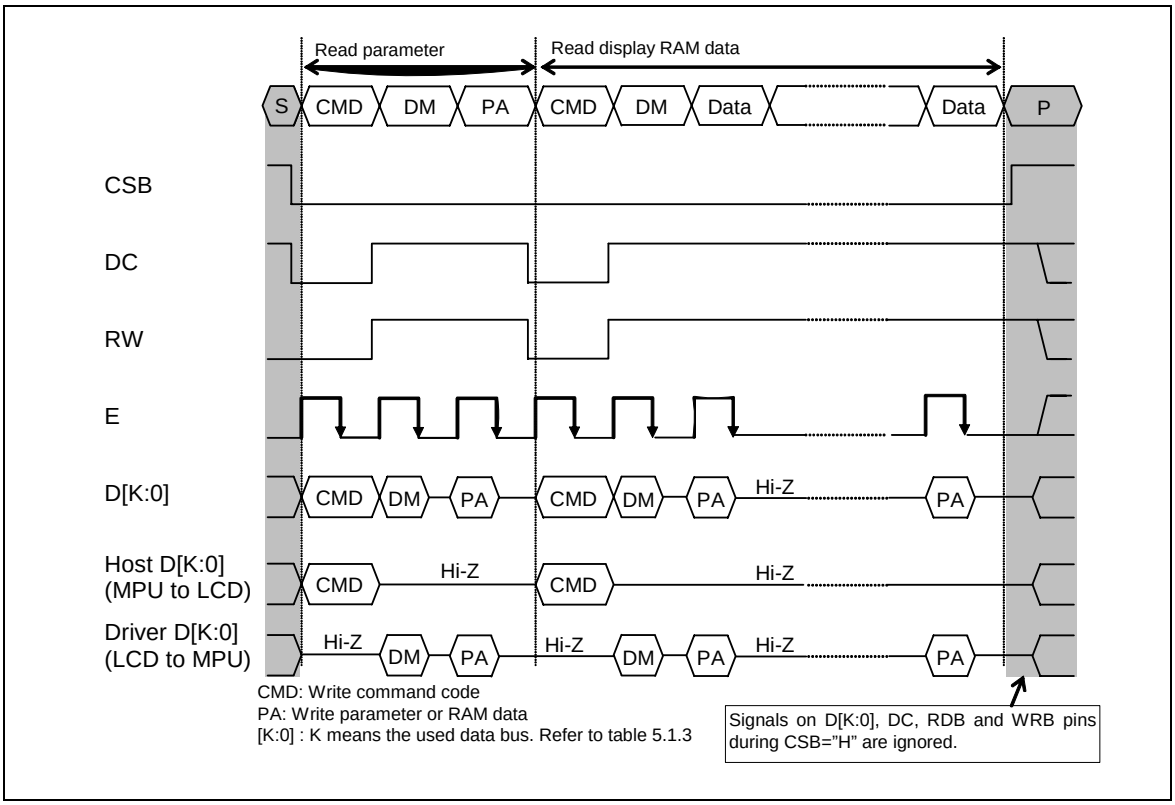


Fig. 5.1.6 6800-Series parallel bus protocol, read from register

5.1.5 Serial Interface

Communication with the microprocessor can also be done via a clock-synchronized serial peripheral interface. The selection of this interface is done when all of BS2, BS1 and BS0 are “L” state (VSS1).

The serial interface is a 3-pin or 4-pin bi-directional interface for communication between the micro controller and the LCD driver chip. The 3-pin serial use: SCEB (chip enable), SCL (serial clock) and SDA (serial data input/output) and 4-pin serial use: SCEB (chip enable), DC (data / command select), SCL (serial clock) and SDA (serial data input/output). Serial clock (SCL) is controlled for interface only by MPU, so it can be stopped when the communication is not necessary.

5.1.5.1 Write Mode

The write mode of the interface means the micro controller writes commands and data to the LDS285. 3-Pin serial data packet contains a control bit DC and a transmission byte and in 4-pin serial case, data packet contains just transmission byte and control bit DC is transferred by the DC pin. If DC is “L”, the transmission byte is interpreted as a command byte. If DC is “H”, the transmission byte is stored in the display data RAM (Memory write command), or command register as a parameter.

Any instruction can be sent in any order to the LDS285. The MSB is transmitted first. The serial interface circuits are initialized when the SCEB is “H” state. In this initialize state, SCL clock pulse or SDA data inputs have no effect. A falling edge of SCEB enables the serial interface and indicates the start of data transmission.

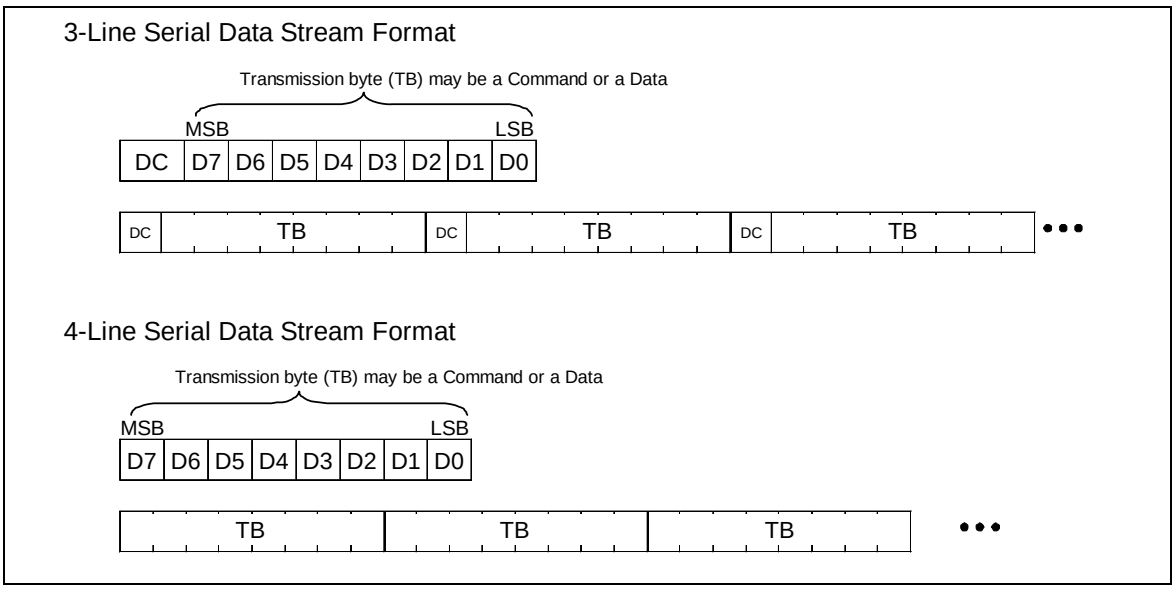


Fig. 5.1.7 Serial data stream, write mode

When SCEB is “H” state, SCL clock is ignored. During the high time of SCEB the serial interface is initialized. At the falling SCEB edge, SCL can be high or low (see ***Fig 5.1.8***). SDA is sampled at the rising edge of SCL. DC indicates, whether the byte is command code (DC=0) or parameter/DDRAM data (DC=1). It is sampled when first rising SCL edge (3-line serial interface) or 8th rising SCLK edge (4-line serial interface). If SCEB stays low after the last bit of command/data byte, the serial interface expects the DC bit (3-line serial interface) or D7 (4-line serial interface) of the next byte at the next rising edge of SCL.

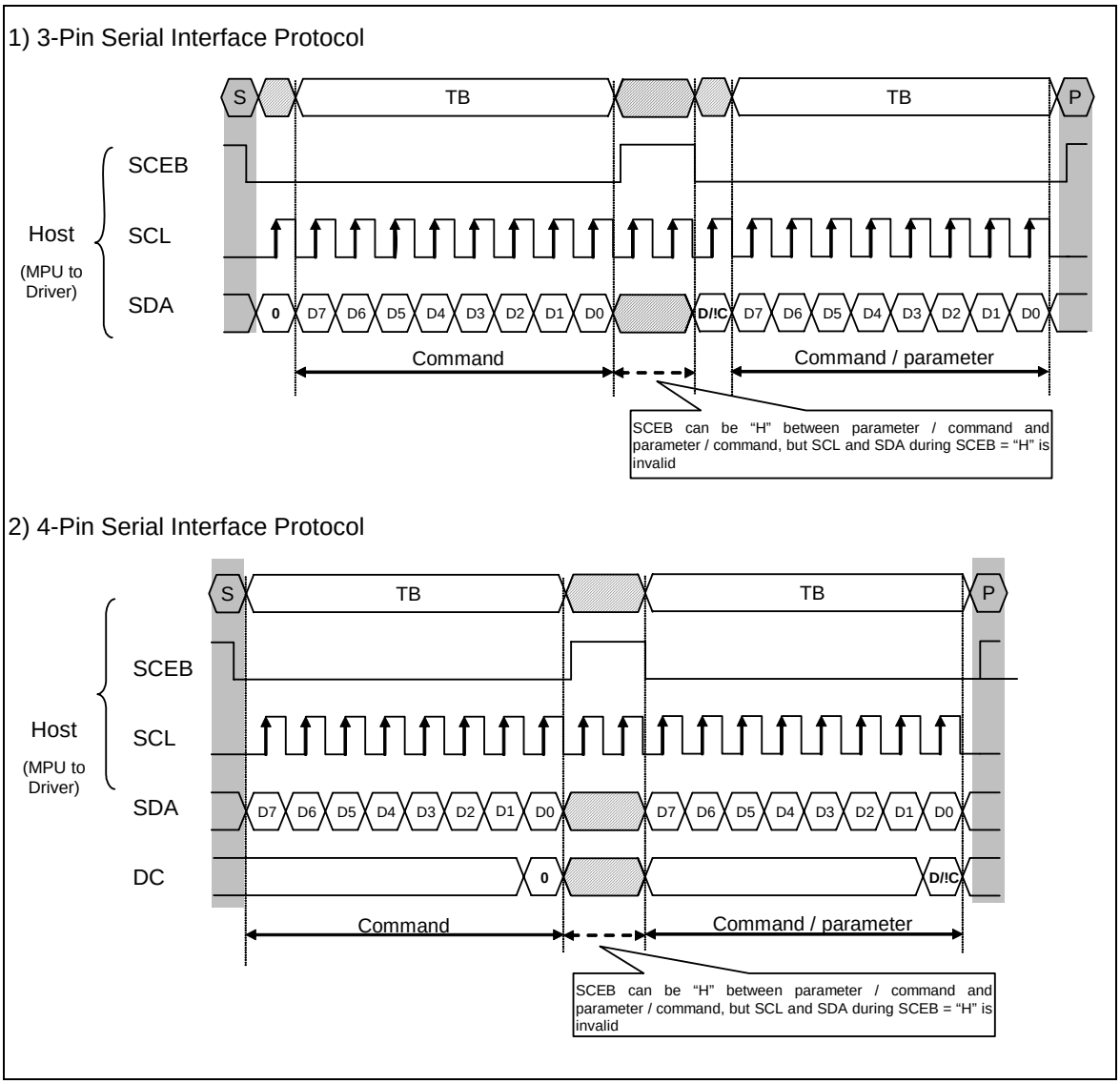


Fig. 5.1.8 Serial bus protocol, write to register with control bit in transmission

5.1.5.2 Read Mode

The read mode of the interface means that the micro controller reads register value from the LDS285. To do so the micro controller first has to send a command (Read ID or Read Register command) and then the following byte is transmitted in the opposite direction. After that, SCEB is required to go high before a new command is send (see ***Fig. 5.1.9*** and ***Fig. 5.1.10***). The LDS285 samples the SDA (input data) at the rising edges, but shifts SDA (output data) at the falling SCL edges. Thus the micro controller is supported to read data at the rising SCL edges.

After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling SCL edge of the last bit (see ***Fig. 5.1.9*** and ***Fig. 5.1.10***).

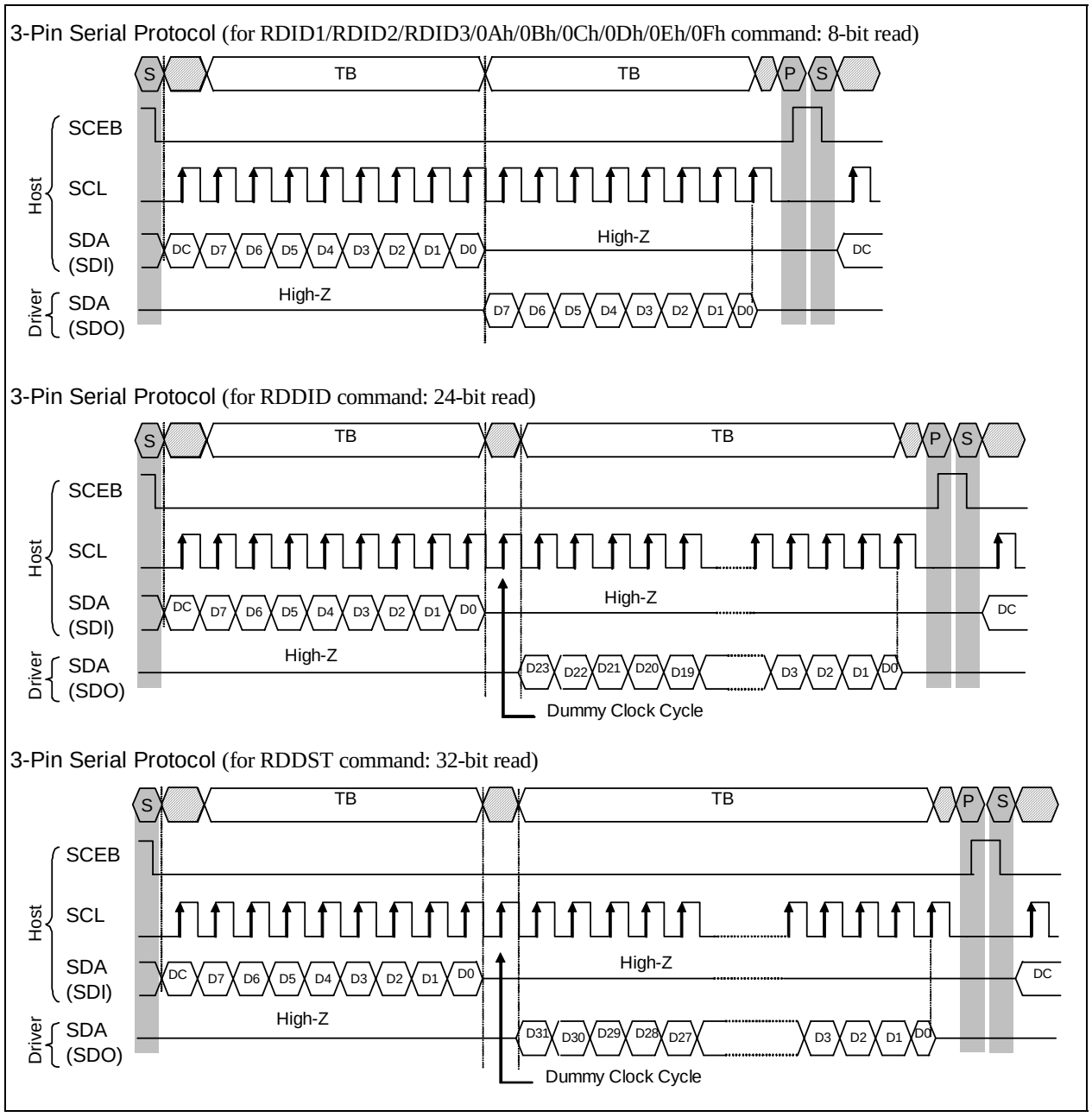
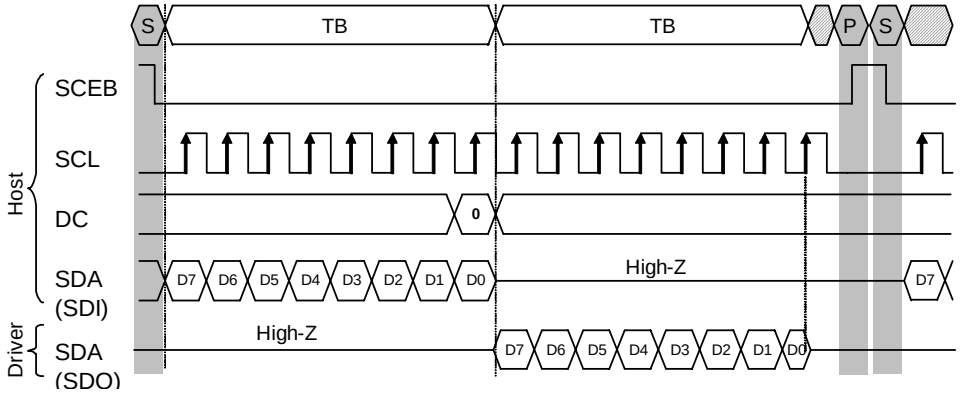
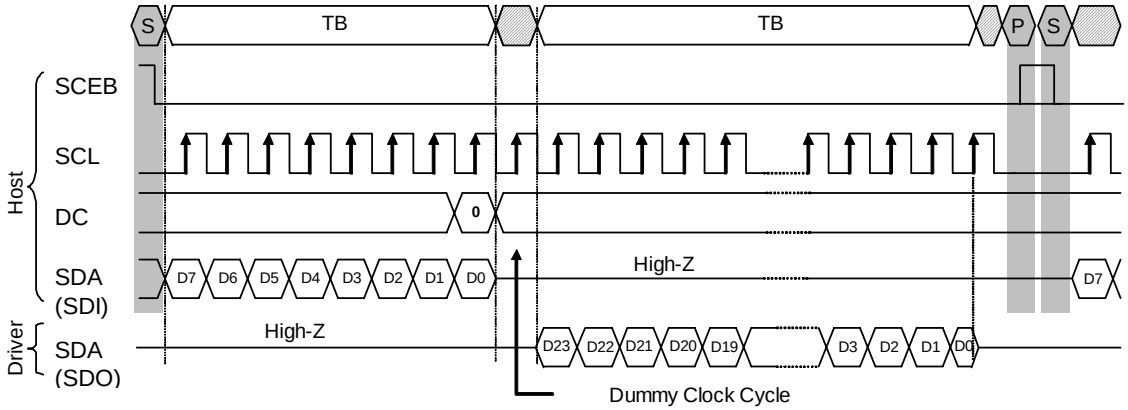


Fig. 5.1.9 Serial bus protocol, read mode (3-Pin serial interface case)

4-Pin Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)



4-Pin Serial Protocol (for RDDID command: 24-bit read)



4-Pin Serial Protocol (for RDDST command: 32-bit read)

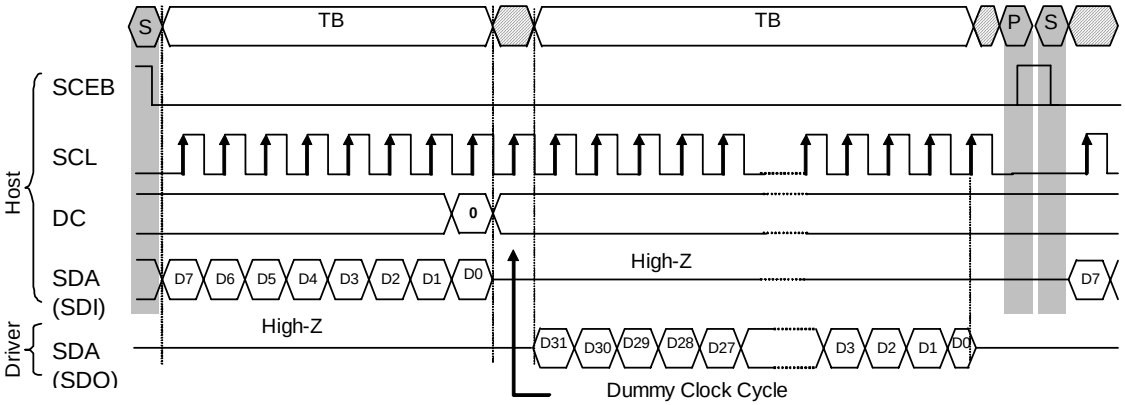


Fig. 5.1.10 Serial bus protocol, read mode (4-Pin serial interface case)

5.1.6 Interface Pause

It will be possible when transferring a Command, DDRAM Data or Multiple Parameter Data to invoke a pause in the data transmission. If the Chip Select Line (CSB) is released after a whole byte of a DDRAM Data or Multiple Parameter Data has been completed, then LDS285 will wait and continue the DDRAM Data or Parameter Data Transmission from the point where it was paused. If the Chip Select Line is released after a whole byte of a command has been completed, then the Display Module will receive either the command's parameters (if appropriate) or a new command when the Chip Select Line is next enabled as shown below.

This applies to the following 4 conditions:

1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter

5.1.6.1 Parallel Interface Pause

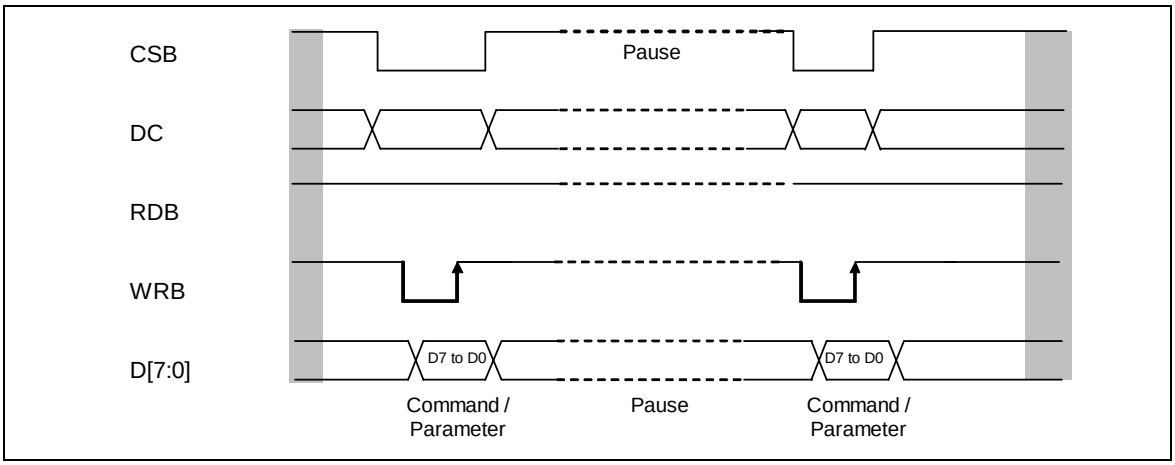


Fig. 5.1.11 Parallel bus protocol, write mode – paused by CSB

5.1.6.2 Serial Interface Pause

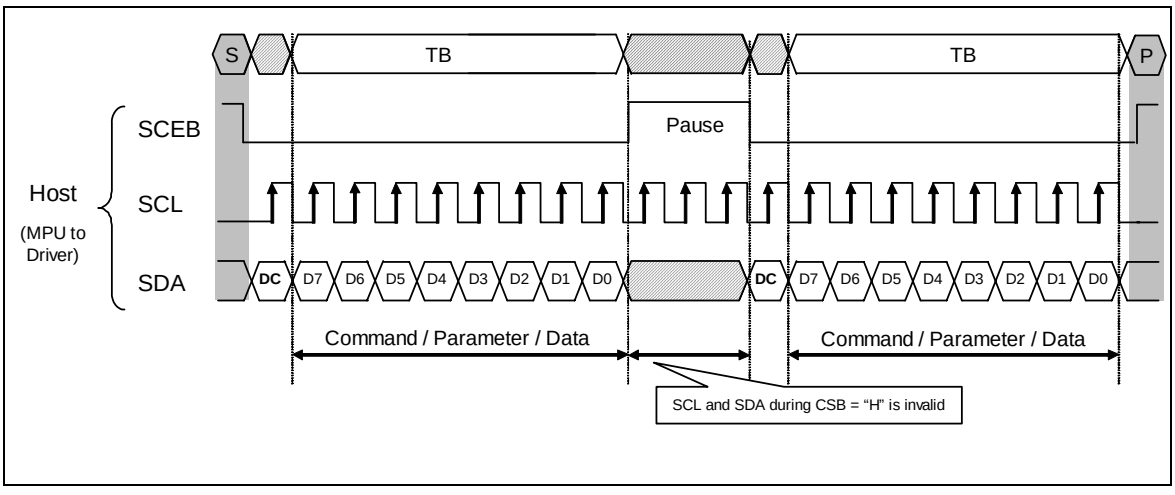


Fig. 5.1.12 Serial bus protocol, write mode – paused by SCEB (3-Pin serial case)

5.1.7 Data Transfer Recovery

If there is a break in data transmission by RESB pulse, while transferring a Command or DDRAM Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then LDS285 will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select line (SCEB) is next activated after RESB have been High state. See the following example (See ***Fig. 5.1.13***)

If there is a break in data transmission by SCEB pulse, while transferring a Command or DDRAM Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then LDS285 will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (SCEB) is next activated. See the following example (See ***Fig. 5.1.14***)

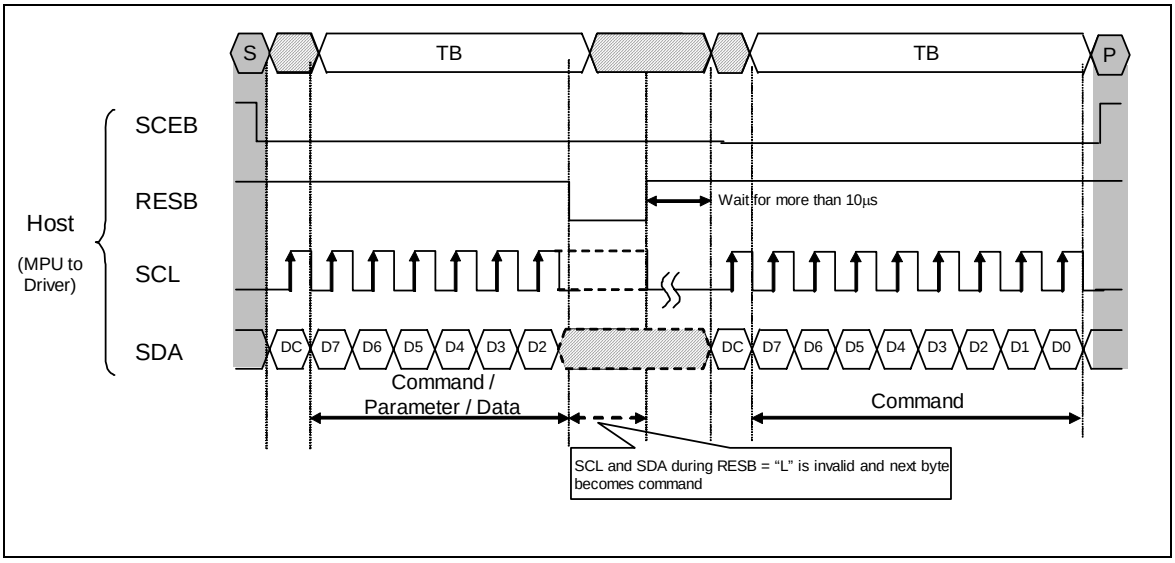


Fig. 5.1.13 Serial bus protocol, write mode – interrupted by RESB

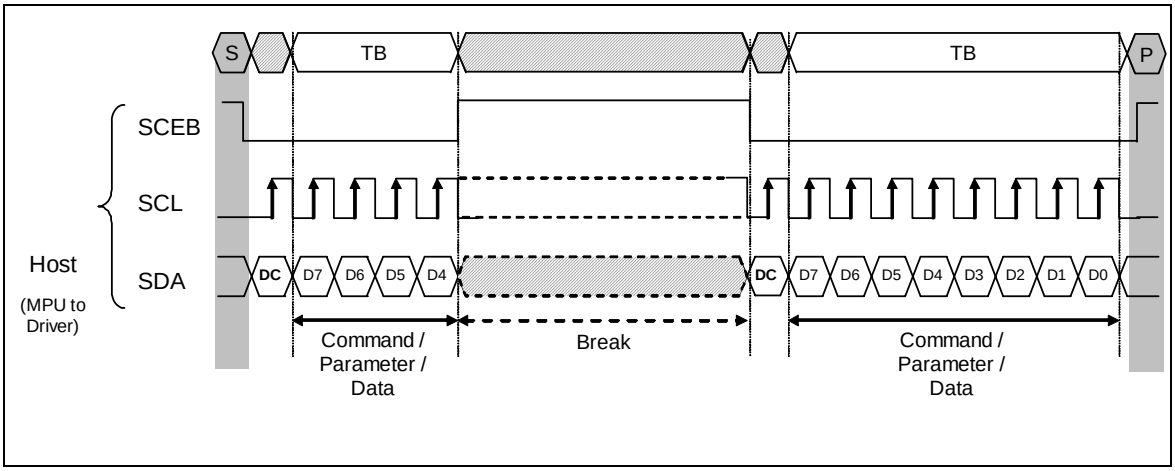


Fig. 5.1.14 Serial bus protocol, write mode – interrupted by SCEB

If 1, 2 or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown in ***Fig. 5.1.15***.

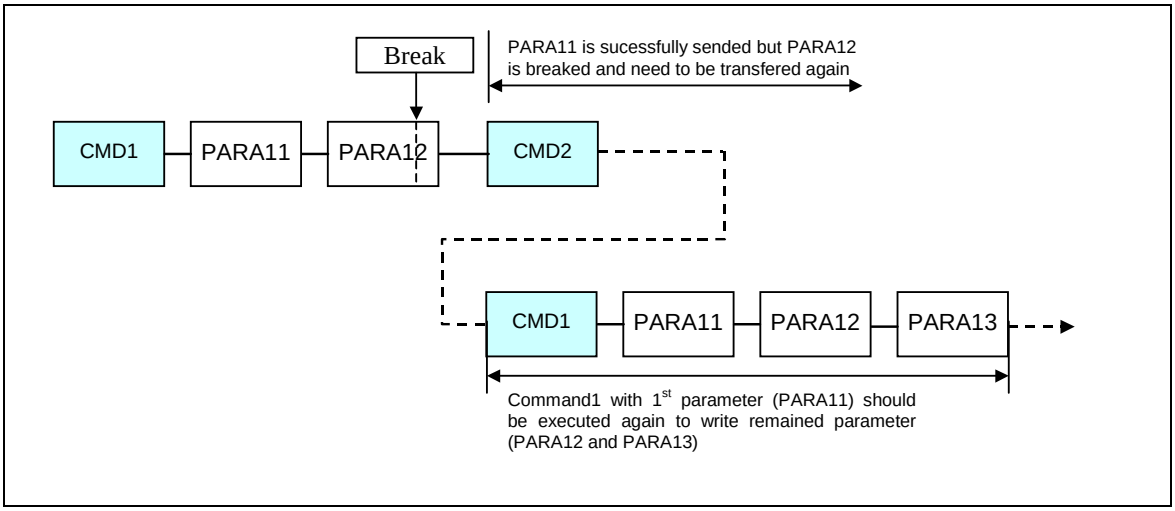


Fig. 5.1.15 Write interrupt recovery (serial interface)

If a 2 or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters that were successfully sent are stored and the other parameter of that command remains previous value.

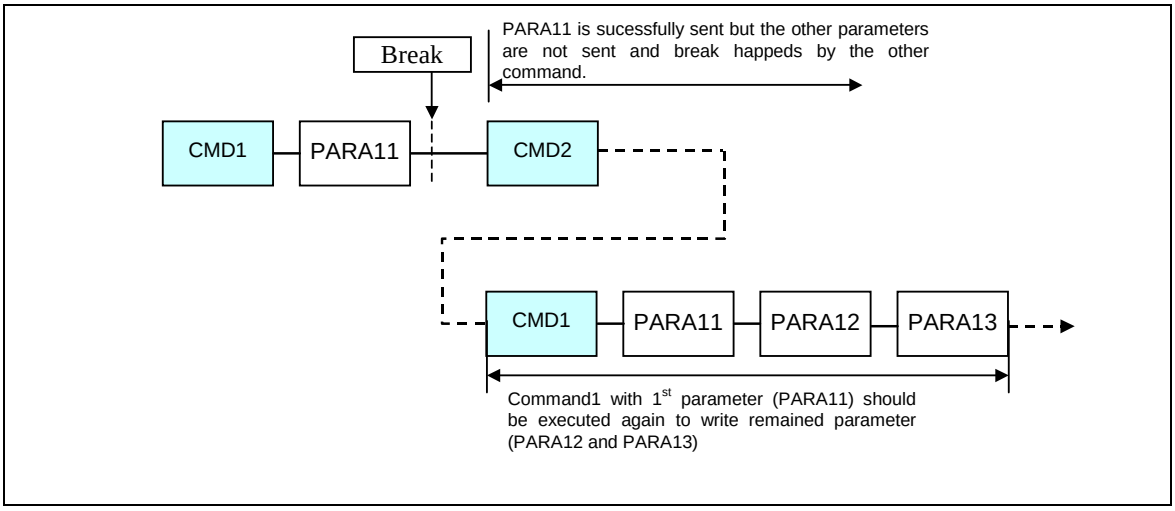


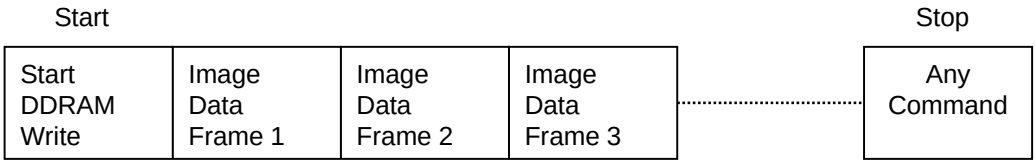
Fig. 5.1.16 Write interrupt recovery (both serial and parallel interface)

5.1.8 Display Module Data Transfer Modes

The Module has two kinds color modes for transferring data to the display RAM. These are 18-bit color per pixel and 24-bit color per pixel. The data format is described for each interface. Data can be downloaded to the DDRAM by 2 methods.

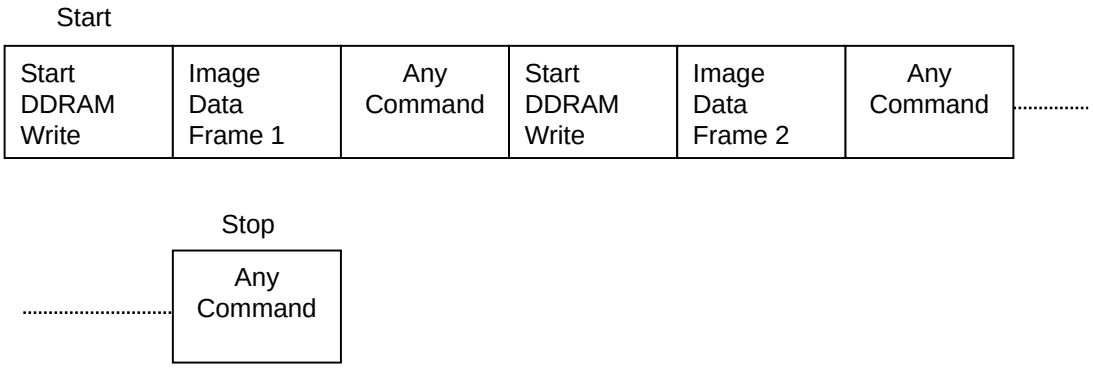
5.1.8.1 Method 1

The Image data is sent to the DDRAM in successive Frame writes, each time the DDRAM is filled, the DDRAM pointer is reset to the start point and the next Frame is written.



5.1.8.2 Method 2

Image Data is sent and at the end of each DDRAM download, a command is sent to stop DDRAM Write. Then Start Memory Write command is sent, and a new Frame is downloaded.



Note:

1) These apply to all Data Transfer Color modes on both Serial and Parallel interfaces.

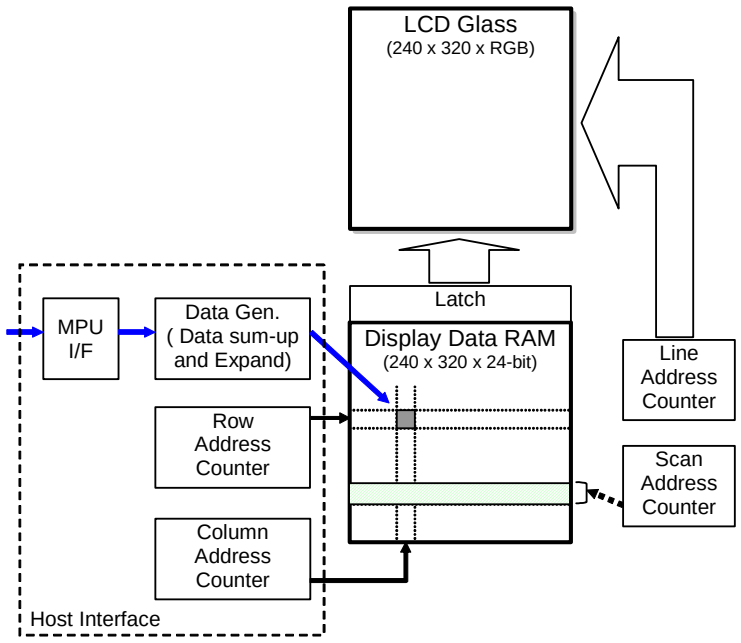
2) The DDRAM can contain both odd and even number of pixels for both Methods. Only complete pixel data will be stored in the DDRAM.

5.2 DISPLAY DATA RAM (DDRAM)

The LDS285 has an integrated 240x320x24-bit graphic type static RAM. This 1.84M-bit memory allows to store on-chip a 240xRGBx320 image with an 24-bpp resolution (16M-color).

There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or write to the same location of the DDRAM.

Display Data RAM Organization



5.2.1 Display Data Formats

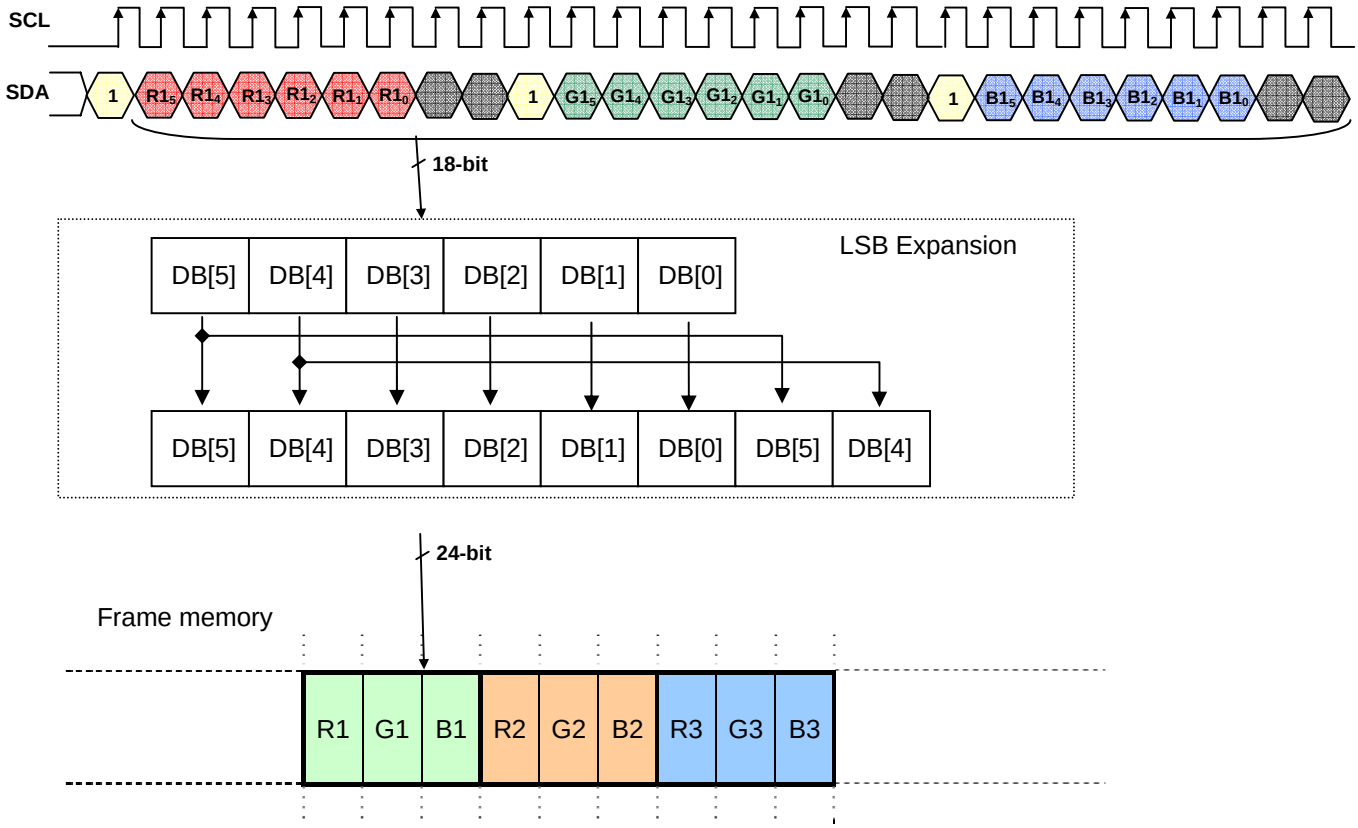
5.2.1.1 Serial Interface Mode (3-Pin serial I/F)

Different display data formats are available for two colors depth supported by the LDS285 listed below.

262k colors, RGB 6-6-6-bits input (see ***Table 5.2.1***)

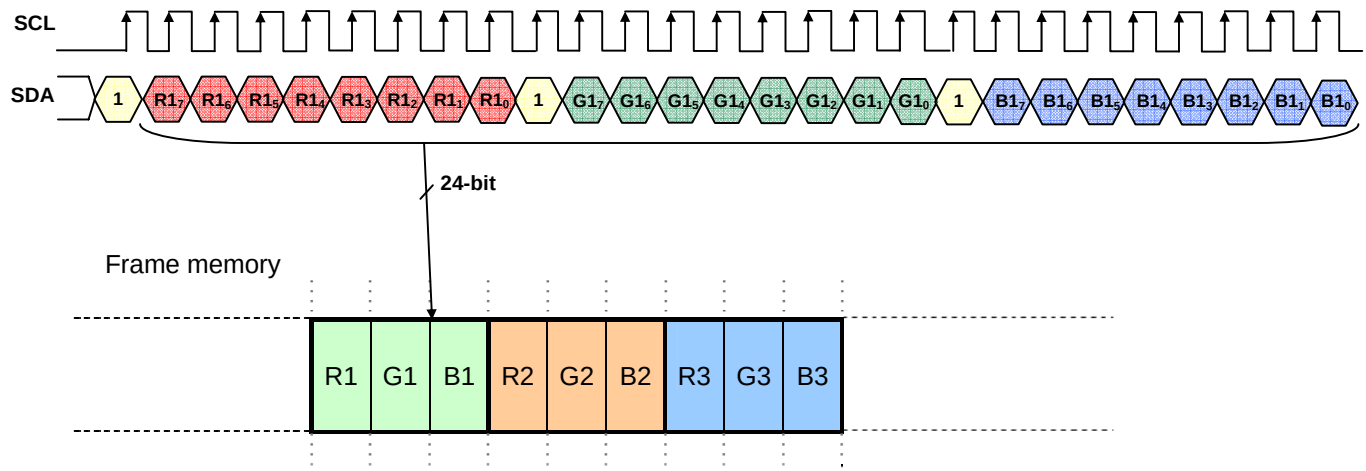
16M colors, RGB 8-8-8-bits input (see ***Table 5.2.2***)

Table 5.2.1 Write data for RGB 6-6-6-bits input



NOTE: 1 pixel data with the 18-bit color depth information.
The most significant bits are: Rx5, Gx5 and Bx5.
The least significant bits are: Rx0, Gx0 and Bx0.

Table 5.2.2 Write data for RGB 8-8-8-bits input



NOTE: 1 pixel data with the 24-bit color depth information.
The most significant bits are: Rx7, Gx7 and Bx7.
The least significant bits are: Rx0, Gx0 and Bx0.

5.2.1.2 8-Bit Parallel Interface Mode

Different display data formats are available for two colors depth supported by the LDS285 listed below.

262k colors, RGB 6-6-6-bits input (see ***Table 5.2.3***)

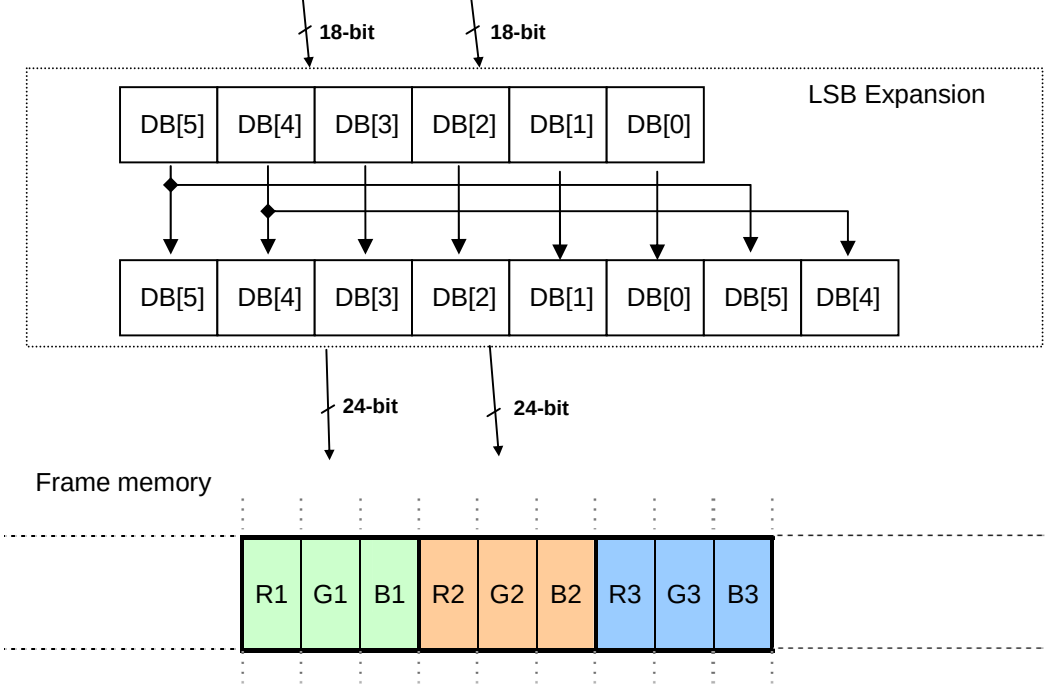
16M colors, RGB 8-8-8-bits input (see ***Table 5.2.4***)

Read (see ***Table 5.2.5***)

Table 5.2.3 Write data for RGB 6-6-6-bits input

"X" : Don't care

262k Color data	DC	D7	D6	D5	D4	D3	D2	D1	D0	Memory Write
MEMWR	0	Memory Write Command Code								-
1st write	1	$R1_5$	$R1_4$	$R1_3$	$R1_2$	$R1_1$	$R1_0$	x	x	-
2nd write	1	$G1_5$	$G1_4$	$G1_3$	$G1_2$	$G1_1$	$G1_0$	x	x	-
3rd write	1	$B1_5$	$B1_4$	$B1_3$	$B1_2$	$B1_1$	$B1_0$	x	x	1st pixel data (R1/G1/B1)
4th write	1	$R2_5$	$R2_4$	$R2_3$	$R2_2$	$R2_1$	$R2_0$	x	x	-
5th write	1	$G2_5$	$G2_4$	$G2_3$	$G2_2$	$G2_1$	$G2_0$	x	x	-
6th write	1	$B2_5$	$B2_4$	$B2_3$	$B2_2$	$B2_1$	$B2_0$	x	x	2nd pixel data (R2/G2/B2)

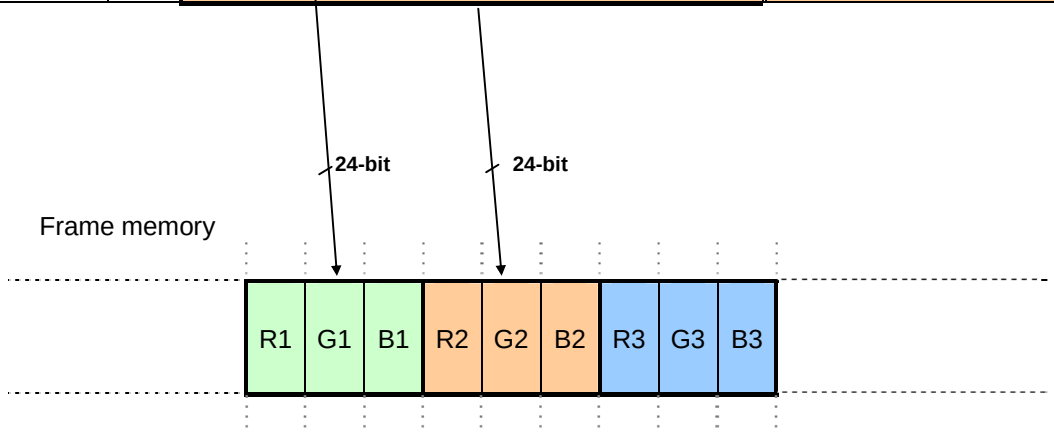


NOTE: 3 times transfer is used to transmit 1 pixel data with the 18-bit color depth information.
The most significant bits are: Rx5, Gx5 and Bx5.
The least significant bits are: Rx0, Gx0 and Bx0.

Table 5.2.4 Write data for RGB 8-8-8-bits input

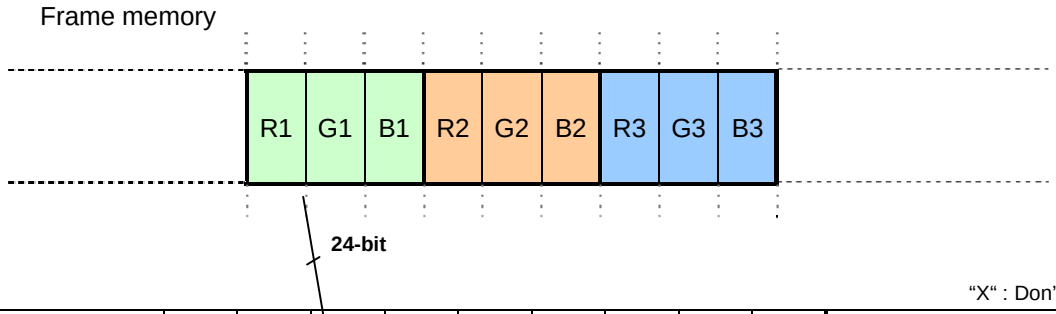
"X" : Don't care

262k Color data	DC	D7	D6	D5	D4	D3	D2	D1	D0	Memory Write
MEMWR	0	Memory Write Command Code								-
1st write	1	$R1_7$	$R1_6$	$R1_5$	$R1_4$	$R1_3$	$R1_2$	$R1_1$	$R1_0$	-
2nd write	1	$G1_7$	$G1_6$	$G1_5$	$G1_4$	$G1_3$	$G1_2$	$G1_1$	$G1_0$	-
3rd write	1	$B1_7$	$B1_6$	$B1_5$	$B1_4$	$B1_3$	$B1_2$	$B1_1$	$B1_0$	1st pixel data (R1/G1/B1)
4th write	1	$R2_7$	$R2_6$	$R2_5$	$R2_4$	$R2_3$	$R2_2$	$R2_1$	$R2_0$	-
5th write	1	$G2_7$	$G2_6$	$G2_5$	$G2_4$	$G2_3$	$G2_2$	$G2_1$	$G2_0$	-
6th write	1	$B2_7$	$B2_6$	$B2_5$	$B2_4$	$B2_3$	$B2_2$	$B2_1$	$B2_0$	2nd pixel data (R2/G2/B2)



NOTE: 3 times transfer is used to transmit 1 pixel data with the 18-bit color depth information.
The most significant bits are: Rx5, Gx5 and Bx5.
The least significant bits are: Rx0, Gx0 and Bx0.

Table 5.2.5 Read



"X" : Don't care

16M Color data	DC	D7	D6	D5	D4	D3	D2	D1	D0	Memory Read
MEMRD	0	Memory Read Command Code								-
dummy	1	x	x	x	x	x	x	x	x	
1st Read	1	$R1_7$	$R1_6$	$R1_5$	$R1_4$	$R1_3$	$R1_2$	$R1_1$	$R1_0$	-
2nd Read	1	$G1_7$	$G1_6$	$G1_5$	$G1_4$	$G1_3$	$G1_2$	$G1_1$	$G1_0$	-
3rd Read	1	$B1_7$	$B1_6$	$B1_5$	$B1_4$	$B1_3$	$B1_2$	$B1_1$	$B1_0$	1st pixel data (R1/G1/B1)

NOTE: 3 times transfer is used to transmit 1 pixel data with the 24-bit color depth information.
The read data can be different to the written data because of the LSB Expansion.

5.2.1.3 9-Bit Parallel Interface Mode

Different display data formats are available for two colors depth supported by the LDS285 listed below.

262k colors, RGB 6-6-6-bits input (see ***Table 5.2.6***)

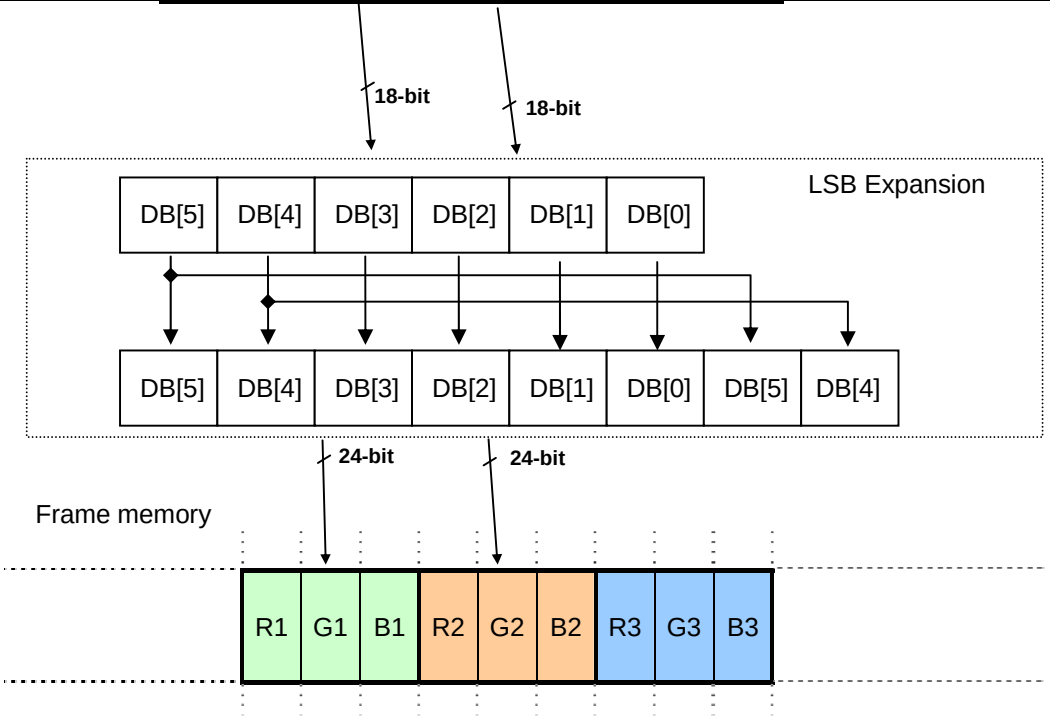
16M colors, RGB 8-8-8-bits input (see ***Table 5.2.7***)

Read (see ***Table 5.2.8***)

Table 5.2.6 Write data for RGB 6-6-6-bits input

"X" : Don't care

262k Color data	DC	D8	D7	D6	D5	D4	D3	D2	D1	D0	Memory Write
MEMWR	0	x	Memory Write Command Code								-
1st write	1	$R1_5$	$R1_4$	$R1_3$	$R1_2$	$R1_1$	$R1_0$	$G1_5$	$G1_4$	$G1_3$	-
2nd write	1	$G1_2$	$G1_1$	$G1_0$	$B1_5$	$B1_4$	$B1_3$	$B1_2$	$B1_1$	$B1_0$	-1st pixel data (R1/G1/B1)
3rd write	1	$R2_5$	$R2_4$	$R2_3$	$R2_2$	$R2_1$	$R2_0$	$G2_5$	$G2_4$	$G2_3$	
4th write	1	$G2_2$	$G2_1$	$G2_0$	$B2_5$	$B2_4$	$B2_3$	$B2_2$	$B2_1$	$B2_0$	-2nd pixel data (R2/G2/B2)

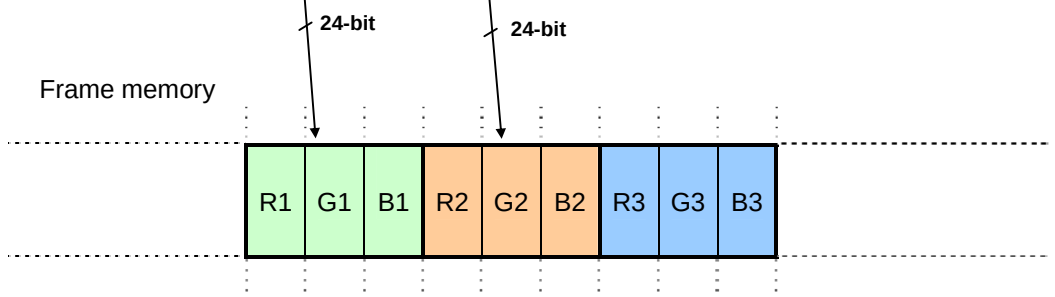


NOTE: 3 times transfer is used to transmit 1 pixel data with the 18-bit color depth information.
The most significant bits are: Rx5, Gx5 and Bx5.
The least significant bits are: Rx0, Gx0 and Bx0.

Table 5.2.7 Write data for RGB 8-8-8-bits input

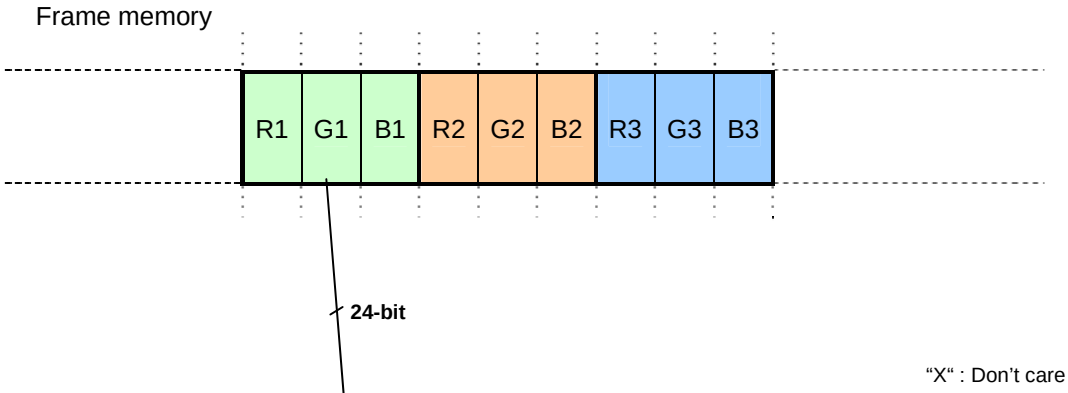
"X" : Don't care

262k Color data	DC	D8	D7	D6	D5	D4	D3	D2	D1	D0	Memory Write
MEMWR	0	Memory Write Command Code									-
1st write	1	x	$R1_7$	$R1_6$	$R1_5$	$R1_4$	$R1_3$	$R1_2$	$R1_1$	$R1_0$	-
2nd write	1	x	$G1_7$	$G1_6$	$G1_5$	$G1_4$	$G1_3$	$G1_2$	$G1_1$	$G1_0$	-
3rd write	1	x	$B1_7$	$B1_6$	$B1_5$	$B1_4$	$B1_3$	$B1_2$	$B1_1$	$B1_0$	1st pixel data (R1/G1/B1)
4th write	1	x	$R2_7$	$R2_6$	$R2_5$	$R2_4$	$R2_3$	$R2_2$	$R2_1$	$R2_0$	-
5th write	1	x	$G2_7$	$G2_6$	$G2_5$	$G2_4$	$G2_3$	$G2_2$	$G2_1$	$G2_0$	-
6th write	1	x	$B2_7$	$B2_6$	$B2_5$	$B2_4$	$B2_3$	$B2_2$	$B2_1$	$B2_0$	2nd pixel data (R2/G2/B2)



NOTE: 3 times transfer is used to transmit 1 pixel data with the 18-bit color depth information.
The most significant bits are: Rx5, Gx5 and Bx5.
The least significant bits are: Rx0, Gx0 and Bx0.

Table 5.2.8 Read



"X" : Don't care

16M Color data	DC	D8	D7	D6	D5	D4	D3	D2	D1	D0	Memory Read
MEMRD	0	x	Memory Read Command Code								-
dummy	1	x	x	x	x	x	x	x	x	x	
1st Read	1	$R1_7$	$R1_6$	$R1_5$	$R1_4$	$R1_3$	$R1_2$	$R1_1$	$R1_0$	x	-
2nd Read	1	$G1_7$	$G1_6$	$G1_5$	$G1_4$	$G1_3$	$G1_2$	$G1_1$	$G1_0$	x	-
3rd Read	1	$B1_7$	$B1_6$	$B1_5$	$B1_4$	$B1_3$	$B1_2$	$B1_1$	$B1_0$	x	1st pixel data (R1/G1/B1)

NOTE: 3 times transfer is used to transmit 1 pixel data with the 24-bit color depth information.
The read data can be different to the written data because of the LSB Expansion.

5.2.1.4 16-Bit Parallel Interface Mode

Different display data formats are available for two colors depth supported by the LDS285 listed below.

262k colors, RGB 6-6-6-bits input (see ***Table 5.2.9***)

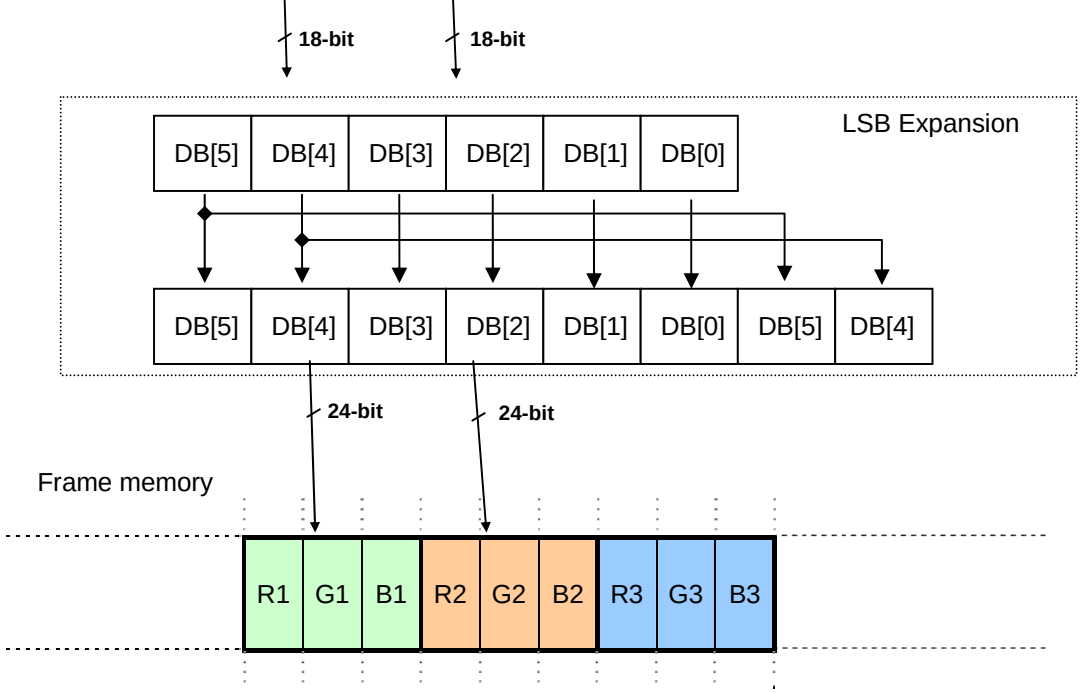
16M colors, RGB 8-8-8-bits input (see ***Table 5.2.10***)

Read (see ***Table 5.2.11***)

Table 5.2.9 Write data for RGB 6-6-6-bits input in 16-bit parallel Interface

"X" : Don't care

262k Color data	DC	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Memory Write
MEMWR	0	x								Memory Write Command Code								-
1st write	1	$R1_5$	$R1_4$	$R1_3$	$R1_2$	$R1_1$	$R1_0$	x	x	$G1_5$	$G1_4$	$G1_3$	$G1_2$	$G1_1$	$G1_0$	x	x	-
2nd write	1	$B1_5$	$B1_4$	$B1_3$	$B1_2$	$B1_1$	$B1_0$	x	x	$R2_5$	$R2_4$	$R2_3$	$R2_2$	$R2_1$	$R2_0$	x	x	1st pixel (R1/G1/B1)
3rd write	1	$G2_5$	$G2_4$	$G2_3$	$G2_2$	$G2_1$	$G2_0$	x	x	$B2_5$	$B2_4$	$B2_3$	$B2_2$	$B2_1$	$B2_0$	x	x	2nd pixel (R2/G2/B2)



NOTE: 3 times transfer is used to transmit 2 pixels data or 2 times transfer are used to transmit 1 pixel data with the 18-bit color depth information..

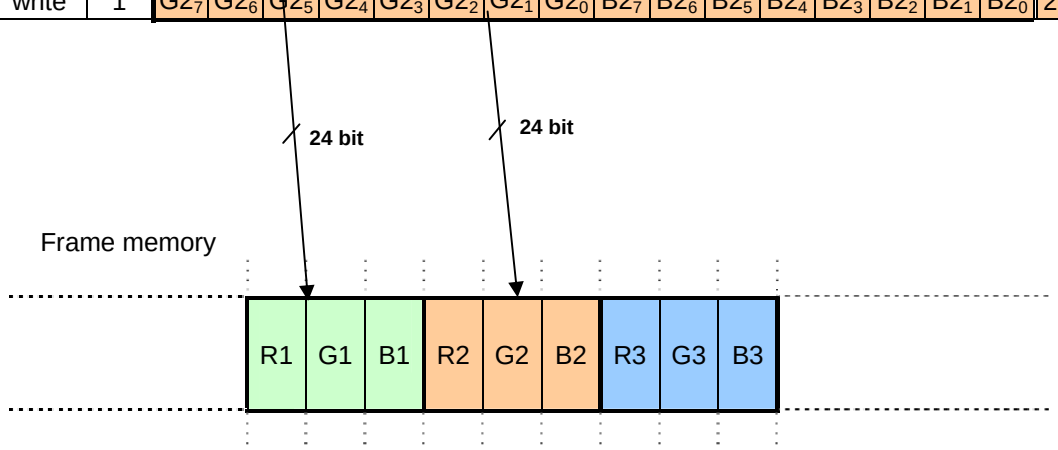
The most significant bits are: Rx5, Gx5 and Bx5.

The least significant bits are: Rx0, Gx0 and Bx0.

Table 5.2.10 Write data for RGB 8-8-8-bits input in 16-bit parallel Interface

"X" : Don't care

16M Color data	DC	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Memory Write
MEMWR	0	x								Memory Write Command Code								-
1st write	1	$R1_7$	$R1_6$	$R1_5$	$R1_4$	$R1_3$	$R1_2$	$R1_1$	$R1_0$	$G1_7$	$G1_6$	$G1_5$	$G1_4$	$G1_3$	$G1_2$	$G1_1$	$G1_0$	-
2nd write	1	$B1_7$	$B1_6$	$B1_5$	$B1_4$	$B1_3$	$B1_2$	$B1_1$	$B1_0$	$R2_7$	$R2_6$	$R2_5$	$R2_4$	$R2_3$	$R2_2$	$R2_1$	$R2_0$	1st pixel (R1/G1/B1)
3rd write	1	$G2_7$	$G2_6$	$G2_5$	$G2_4$	$G2_3$	$G2_2$	$G2_1$	$G2_0$	$B2_7$	$B2_6$	$B2_5$	$B2_4$	$B2_3$	$B2_2$	$B2_1$	$B2_0$	2nd pixel (R2/G2/B2)

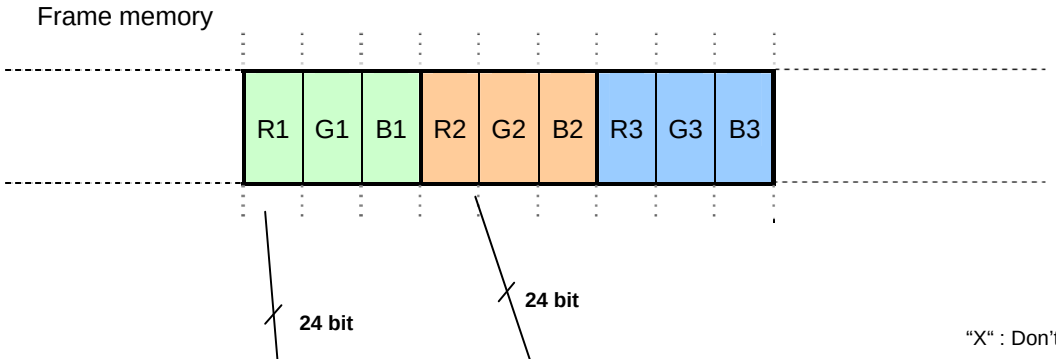


NOTE: 3 times transfer is used to transmit 2 pixels data or 2 times transfer are used to transmit 1 pixel data with the 24-bit color depth information..

The most significant bits are: Rx7, Gx7 and Bx7.

The least significant bits are: Rx0, Gx0 and Bx0.

Table 5.2.11 Read



"X" : Don't care

16M Color data	DC	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Memory Read
MEMRD	0	x								Memory Read Command Code								-
dummy	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
1st Read	1	$R1_7$	$R1_6$	$R1_5$	$R1_4$	$R1_3$	$R1_2$	$R1_1$	$R1_0$	$G1_7$	$G1_6$	$G1_5$	$G1_4$	$G1_3$	$G1_2$	$G1_1$	$G1_0$	-
2nd Read	1	$B1_7$	$B1_6$	$B1_5$	$B1_4$	$B1_3$	$B1_2$	$B1_1$	$B1_0$	$R2_7$	$R2_6$	$R2_5$	$R2_4$	$R2_3$	$R2_2$	$R2_1$	$R2_0$	1st pixel (R1/G1/B1)
3rd Read	1	$G2_7$	$G2_6$	$G2_5$	$G2_4$	$G2_3$	$G2_2$	$G2_1$	$G2_0$	$B2_7$	$B2_6$	$B2_5$	$B2_4$	$B2_3$	$B2_2$	$B2_1$	$B2_0$	2nd pixel (R2/G2/B2)

NOTE: 3 times transfer is used to transmit 2 pixels data or 2 times transfer are used to transmit 1 pixel data with the 24-bit color depth information..

The read data can be different to the written data because of the LSB Expansion.

5.2.1.5 18-Bit Parallel Interface Mode

Different display data formats are available for four colors depth supported by the LDS285 listed below.

262k colors, RGB 6-6-6-bits input (see ***Table 5.2.12***)

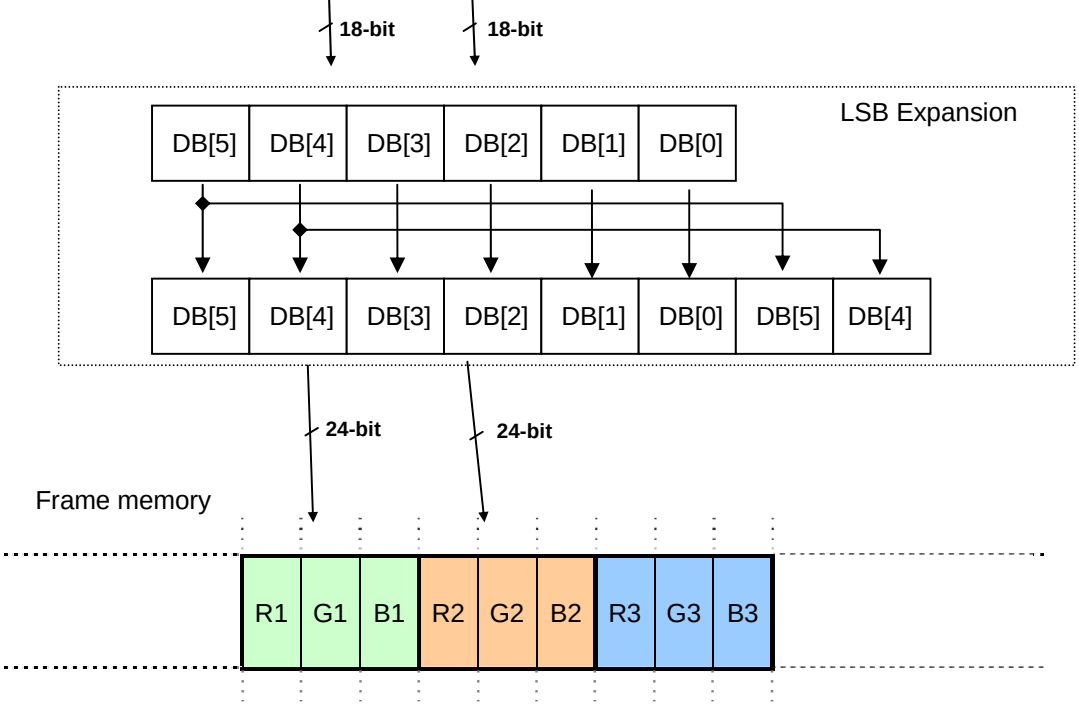
16M colors, RGB 6-6-6-bits input (see ***Table 5.2.13***)

Read (see Table 5.2.14)

Table 5.2.12 Write data for RGB 6-6-6-bits input in 18-bit parallel Interface

"X" : Don't care

262k Color data	DC	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Memory Write
MEMWR	0	x									Memory Write Command Code									-
1st write	1	$R1_5$	$R1_4$	$R1_3$	$R1_2$	$R1_1$	$R1_0$	$G1_5$	$G1_4$	$G1_3$	$G1_2$	$G1_1$	$G1_0$	$B1_5$	$B1_4$	$B1_3$	$B1_2$	$B1_1$	$B1_0$	-1st pixel (R1/G1/B1)
2nd write	1	$R2_5$	$R2_4$	$R2_3$	$R2_2$	$R2_1$	$R2_0$	$G2_5$	$G2_4$	$G2_3$	$G2_2$	$G2_1$	$G2_0$	$B2_5$	$B2_4$	$B2_3$	$B2_2$	$B2_1$	$B2_0$	2nd pixel (R2/G2/B2)



NOTE: 3 times transfer is used to transmit 2 pixels data or 2 times transfer are used to transmit 1 pixel data with the 18-bit color depth information..

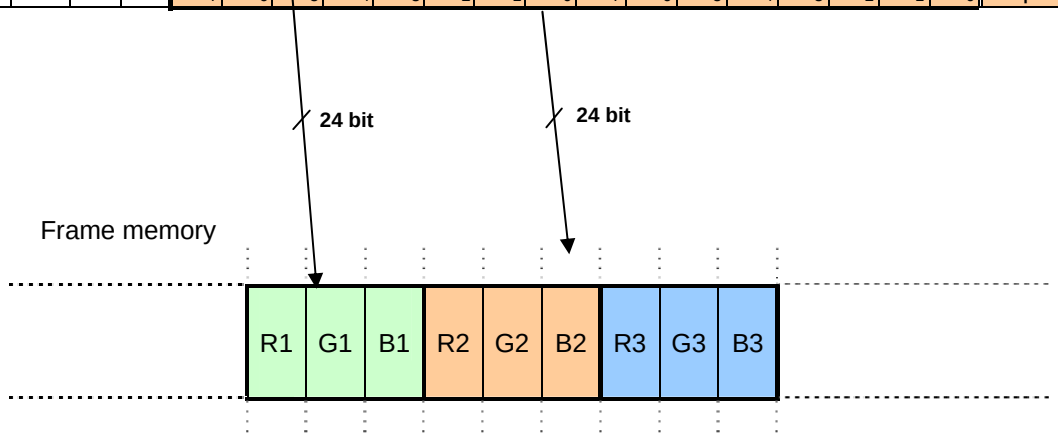
The most significant bits are: Rx5, Gx5 and Bx5.

The least significant bits are: Rx0, Gx0 and Bx0.

Table 5.2.13 Write data for RGB 8-8-8-bits input in 18-bit parallel Interface

"X" : Don't care

16M Color data	DC	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Memory Write
MEMWR	0	x									Memory Write Command Code									-
1st write	1	x	x	$R1_7$	$R1_6$	$R1_5$	$R1_4$	$R1_3$	$R1_2$	$R1_1$	$R1_0$	$G1_7$	$G1_6$	$G1_5$	$G1_4$	$G1_3$	$G1_2$	$G1_1$	$G1_0$	-
2nd write	1	x	x	$B1_7$	$B1_6$	$B1_5$	$B1_4$	$B1_3$	$B1_2$	$B1_1$	$B1_0$	$R2_7$	$R2_6$	$R2_5$	$R2_4$	$R2_3$	$R2_2$	$R2_1$	$R2_0$	1st pixel (R1/G1/B1)
3rd write	1	x	x	$G2_7$	$G2_6$	$G2_5$	$G2_4$	$G2_3$	$G2_2$	$G2_1$	$G2_0$	$B2_7$	$B2_6$	$B2_5$	$B2_4$	$B2_3$	$B2_2$	$B2_1$	$B2_0$	2nd pixel (R2/G2/B2)

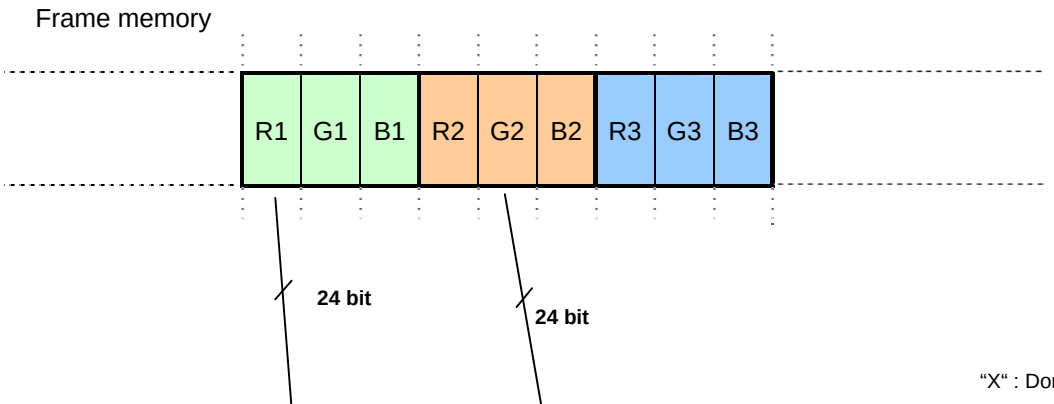


NOTE: 3 times transfer is used to transmit 2 pixels data or 2 times transfer are used to transmit 1 pixel data with the 24-bit color depth information..

The most significant bits are: Rx7, Gx7 and Bx7.

The least significant bits are: Rx0, Gx0 and Bx0.

Table 5.2.14 Read



"X" : Don't care

16M Color data	DC	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Memory Read
MEMRD	0	x									Memory Read Command Code									-
dummy	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
1st Read	1	$R1_7$	$R1_6$	$R1_5$	$R1_4$	$R1_3$	$R1_2$	$R1_1$	$R1_0$	x	$G1_7$	$G1_6$	$G1_5$	$G1_4$	$G1_3$	$G1_2$	$G1_1$	$G1_0$	x	-
2nd Read	1	$B1_7$	$B1_6$	$B1_5$	$B1_4$	$B1_3$	$B1_2$	$B1_1$	$B1_0$	x	$R2_7$	$R2_6$	$R2_5$	$R2_4$	$R2_3$	$R2_2$	$R2_1$	$R2_0$	x	1st pixel (R1/G1/B1)
3rd Read	1	$G2_7$	$G2_6$	$G2_5$	$G2_4$	$G2_3$	$G2_2$	$G2_1$	$G2_0$	x	$B2_7$	$B2_6$	$B2_5$	$B2_4$	$B2_3$	$B2_2$	$B2_1$	$B2_0$	x	2nd pixel (R2/G2/B2)

NOTE: 3 times transfer is used to transmit 2 pixels data or 2 times transfer are used to transmit 1 pixel data with the 24-bit color depth information..

The Read data can be different to the written data because of the LSB Expansion.

5.2.2 RGB Interface

For direct interface with both graphic controller and MPU, LDS285 offers RGB interface mode to receive video data. In RGB interface mode, video data bus becomes (D23 to D1, VD0) and grahic controller can write 24-bit RGB data to predefined row and column address area (by CASET and RASET command) of the DDRAM. Command and parameter to control LDS285 can be accessed by MPU via serial interface mode.

5.2.2.1 RGB Interface Bus Width Set

All 2-kinds of bus width can be available during RGB interface mode. (selected by the 2nd parameter of IFMODE command: DW).

DW	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bus Width
0	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	24-bit data
1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	R7	R6	R5	R4	R3	R2	R1	R0	8-bit data
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	G7	G6	G5	G4	G3	G2	G1	G0	
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B7	B6	B5	B4	B3	B2	B1	B0	

NOTE: Unused RGB data bus must be connected to VSS1.

- 24-Bit RGB Interface Mode

Different display data formats are available for four colors depth supported by the LDS285 listed below.

262k colors, RGB 6-6-6-bits input when (see ***Table 5.2.15***)

16M colors, RGB 8-8-8-bits input when (see ***Table 5.2.16***)

Table 5.2.15 Write data for RGB 6-6-6-bits input in 24-bit rgb Interface

65k Color data	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Memory Write
1st write	x	x	$R1_5$	$R1_4$	$R1_3$	$R1_2$	$R1_1$	$R1_0$	x	x	$G1_5$	$G1_4$	$G1_3$	$G1_2$	$G1_1$	$G1_0$	x	x	$B1_5$	$B1_4$	$B1_3$	$B1_2$	$B1_1$	$B1_0$	1st pixel (R1/G1/B1)
2nd write	x	x	$R2_5$	$R2_4$	$R2_3$	$R2_2$	$R2_1$	$R2_0$	x	x	$G2_5$	$G2_4$	$G2_3$	$G2_2$	$G2_1$	$G2_0$	x	x	$B2_5$	$B2_4$	$B2_3$	$B2_2$	$B2_1$	$B2_0$	2nd pixel (R2/G2/B2)

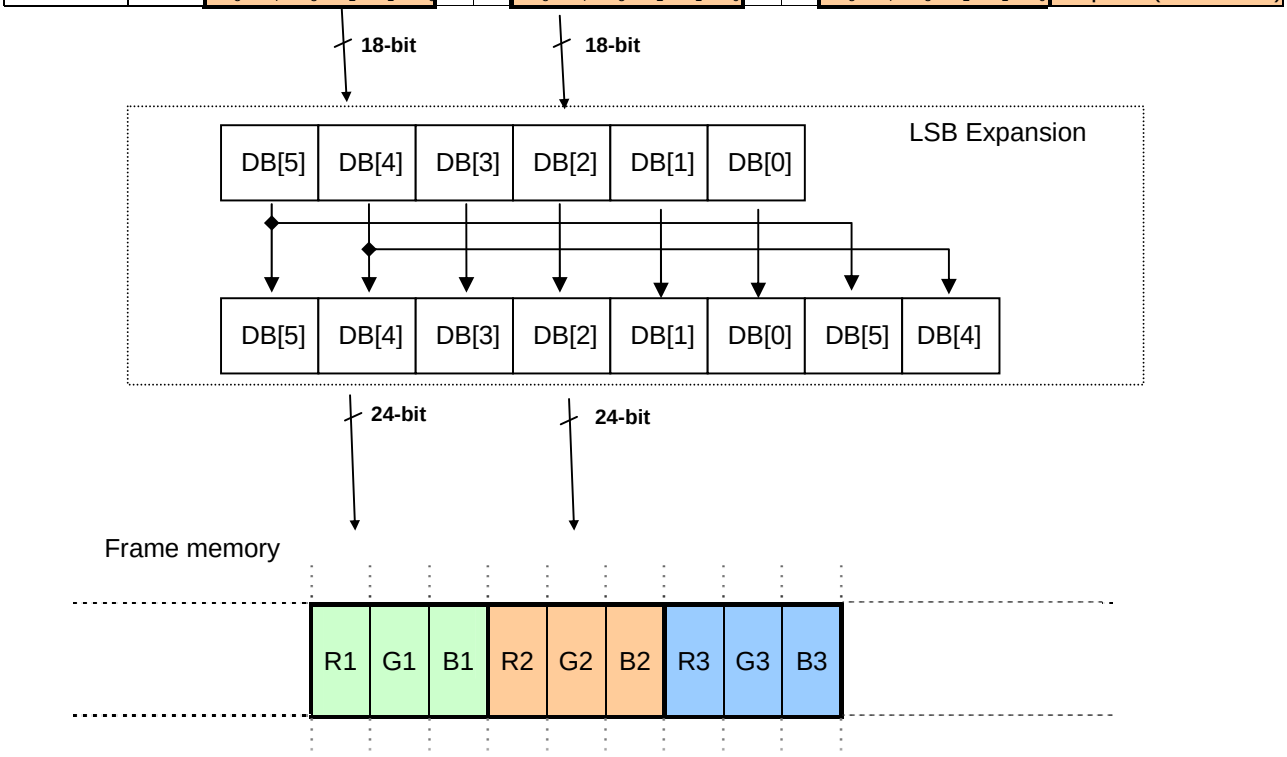
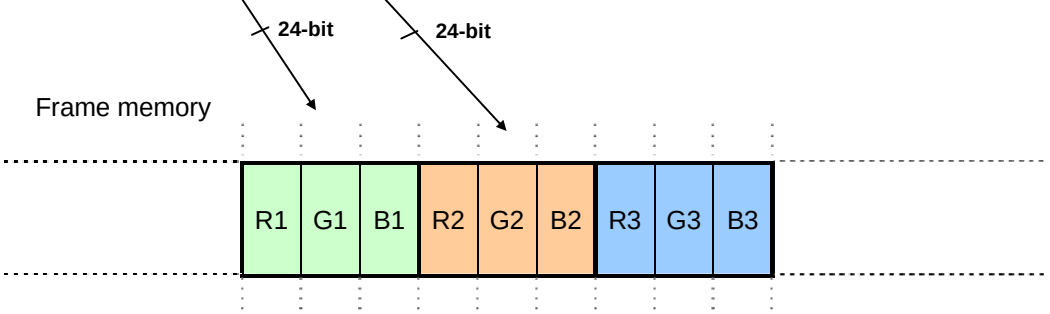


Table 5.2.16 Write data for RGB 8-8-8-bits input in 24-bit rgb Interface

65k Color data	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Memory Write
1st write	$R1_7$	$R1_6$	$R1_5$	$R1_4$	$R1_3$	$R1_2$	$R1_1$	$R1_0$	$G1_7$	$G1_6$	$G1_5$	$G1_4$	$G1_3$	$G1_2$	$G1_1$	$G1_0$	$B1_7$	$B1_6$	$B1_5$	$B1_4$	$B1_3$	$B1_2$	$B1_1$	$B1_0$	1st pixel (R1/G1/B1)
2nd write	$R2_7$	$R2_6$	$R2_5$	$R2_4$	$R2_3$	$R2_2$	$R2_1$	$R2_0$	$G2_7$	$G2_6$	$G2_5$	$G2_4$	$G2_3$	$G2_2$	$G2_1$	$G2_0$	$B2_7$	$B2_6$	$B2_5$	$B2_4$	$B2_3$	$B2_2$	$B2_1$	$B2_0$	2nd pixel (R2/G2/B2)



- 8-Bit RGB Interface Mode

Different display data formats are available for four colors depth supported by the LDS285 listed below.

262k colors, RGB 6-6-6-bits input when (see ***Table 5.2.17***)

16M colors, RGB 8-8-8-bits input when (see ***Table 5.2.18***)

Table 5.2.17 Write data for RGB 6-6-6-bits input in 24-bit rgb Interface

65k Color data	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Memory Write
1st write	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	$R1_5$	$R1_4$	$R1_3$	$R1_2$	$R1_1$	$R1_0$	
2nd write	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	$G1_5$	$G1_4$	$G1_3$	$G1_2$	$G1_1$	$G1_0$	
3rd write	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	$G1_5$	$G1_4$	$G1_3$	$G1_2$	$G1_1$	$G1_0$	1st pixel (R1/G1/B1)
4th write	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	$R2_5$	$R2_4$	$R2_3$	$R2_2$	$R2_1$	$R2_0$	
5th write	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	$G2_5$	$G2_4$	$G2_3$	$G2_2$	$G2_1$	$G2_0$	
6th write	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	$B2_5$	$B2_4$	$B2_3$	$B2_2$	$B2_1$	$B2_0$	2nd pixel (R1/G1/B1)

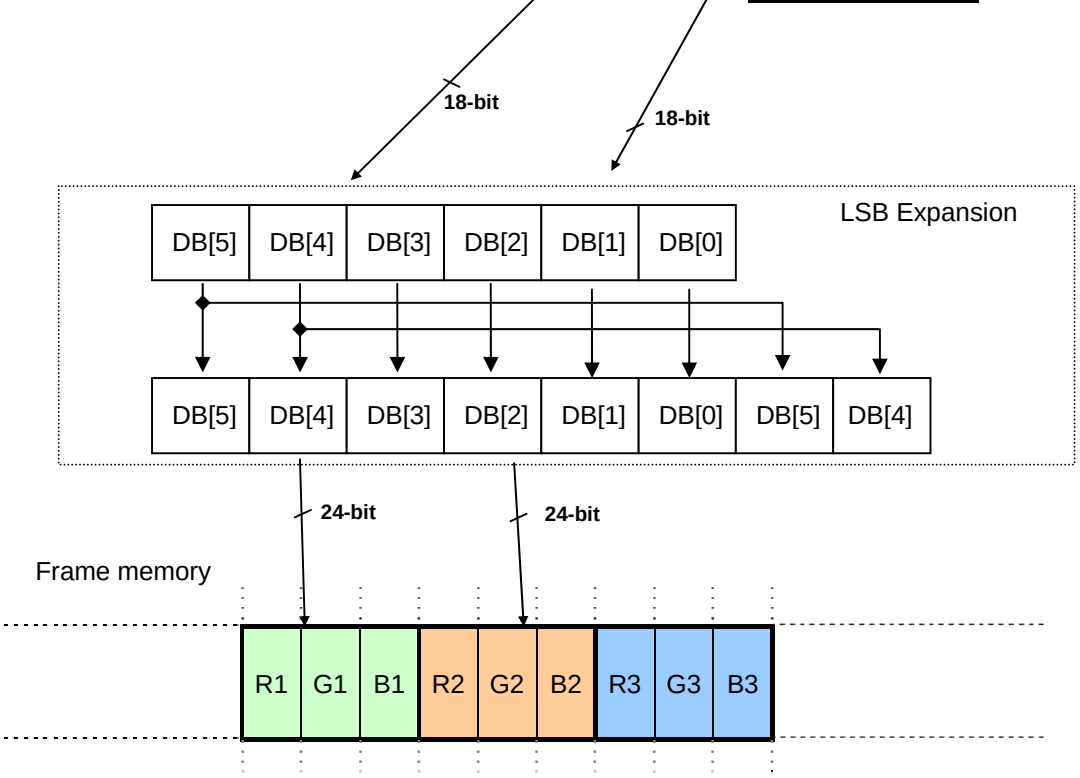
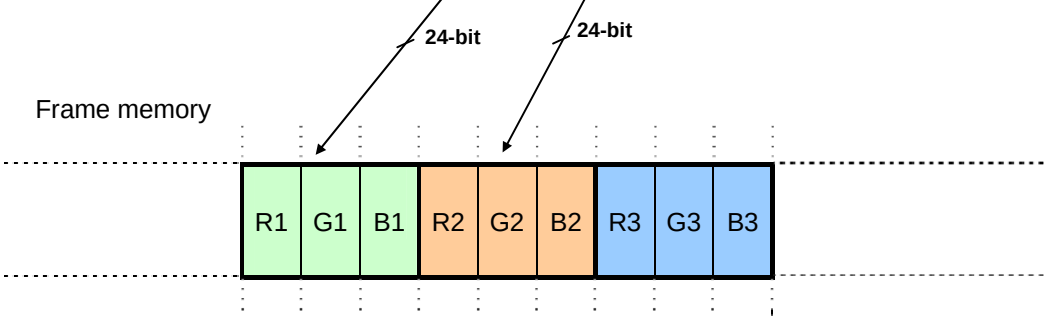


Table 5.2.18 Write data for RGB 8-8-8-bits input in 24-bit rgb Interface

65k Color data	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Memory Write
1st write	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	$R1_7$	$R1_6$	$R1_5$	$R1_4$	$R1_3$	$R1_2$	$R1_1$	$R1_0$	
2nd write	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	$G1_7$	$G1_6$	$G1_5$	$G1_4$	$G1_3$	$G1_2$	$G1_1$	$G1_0$	
3rd write	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	$G1_7$	$G1_6$	$G1_5$	$G1_4$	$G1_3$	$G1_2$	$G1_1$	$G1_0$	1st pixel (R1/G1/B1)
4th write	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	$R2_7$	$R2_6$	$R2_5$	$R2_4$	$R2_3$	$R2_2$	$R2_1$	$R2_0$	
5th write	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	$G2_7$	$G2_6$	$G2_5$	$G2_4$	$G2_3$	$G2_2$	$G2_1$	$G2_0$	
6th write	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	$B2_7$	$B2_6$	$B2_5$	$B2_4$	$B2_3$	$B2_2$	$B2_1$	$B2_0$	2nd pixel (R1/G1/B1)



5.2.2.2 RGB Interface Mode Set

All 3-kinds of RGB interface mode can be available to fit the various controller type.(selected by 1st parameter of IFMODE command : IF1,IF0)

RGB I/F Mode	DCK	ENABLE	Video Data Bus D23 to D1, VD0	VSYNC	VSYNCO	HSYNC	Reference clock for display
RGB Mode1	Used	Used	Used	Not used	Used	Not used	Internal Oscillator
RGB Mode2	Used	Used	Used	Used	Not used	Not used	Internal Oscillator
RGB Mode3	Used	Used	Used	Used	Not used	Used	DCK

NOTE: Unused RGB data bus must be connected to VSS1.

RGB Interface Mode1

Data write to the DDRAM is done by DCK and Video Data Bus (D23 to D1, VD0) when ENABLE is "H" state.
To make the internal displaying clock, internal oscillator is used. So, to write the video data without flickering, controller needs to transfer the data with synchronous to the VSYNCO output signal.

RGB Interface Mode2

Data write to the DDRAM is done by DCK and Video Data Bus (D23 to D1, VD0) when ENABLE is "H" state.

To make the internal displaying clock, internal oscillator is used. But frame display starts with synchronous to VSYNC input. So, to write the video data without flickers, the graphic controller must always transfer VSYNC signal to LDS285.

RGB Interface Mode3

Data write to the DDRAM is done by DCK and Video Data Bus (D23 to D1, VD0) when ENABLE is "H" state.
To make the internal displaying clock, external clocks (DCK, VSYNC and HSYNC) are used. So, the graphic controller must always transfer DCK, VSYNC and HSYNC signal to LDS285.

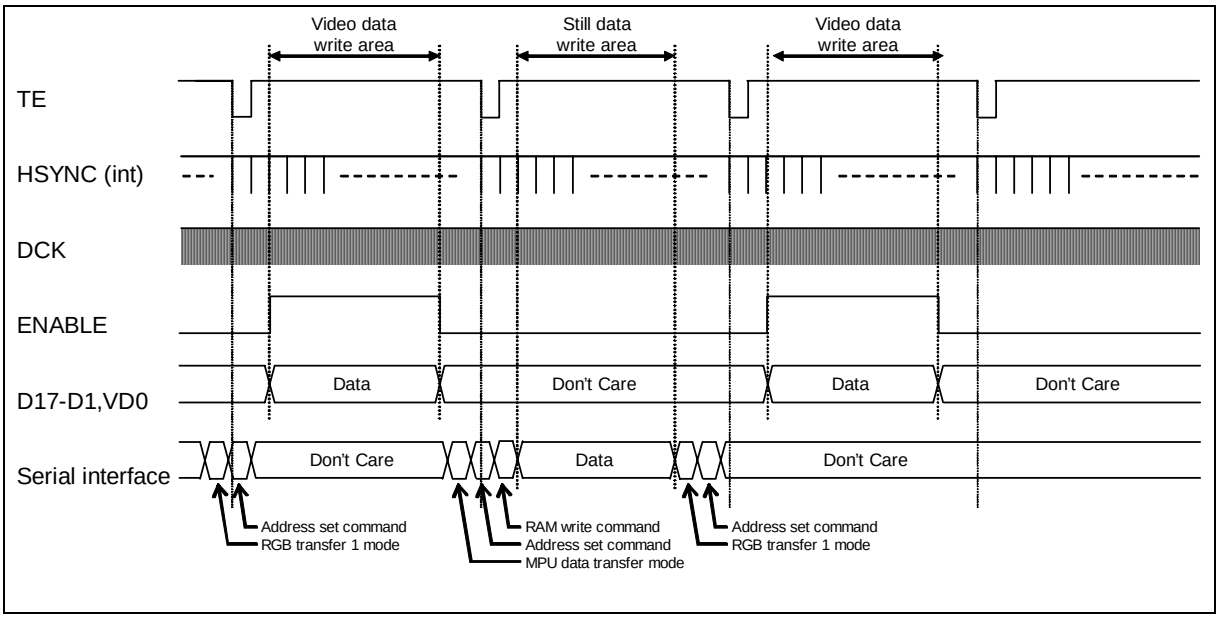


Fig. 5.2.1 An example to overwrite still picture data during moving picture display (RGB Interface Mode1)

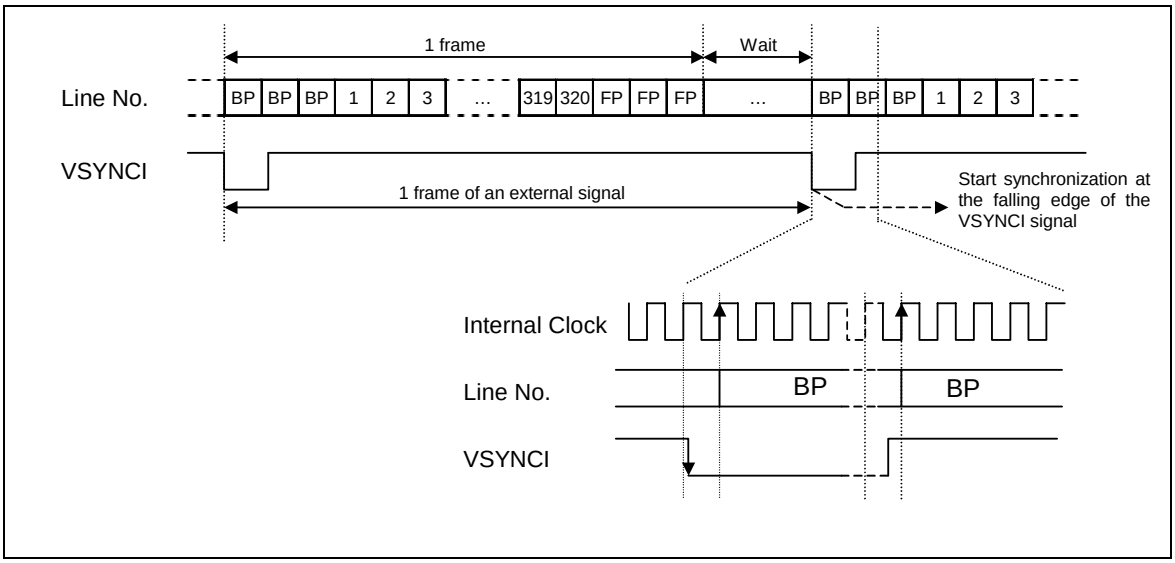


Fig. 5.2.2 An example of RGB Interface Mode2

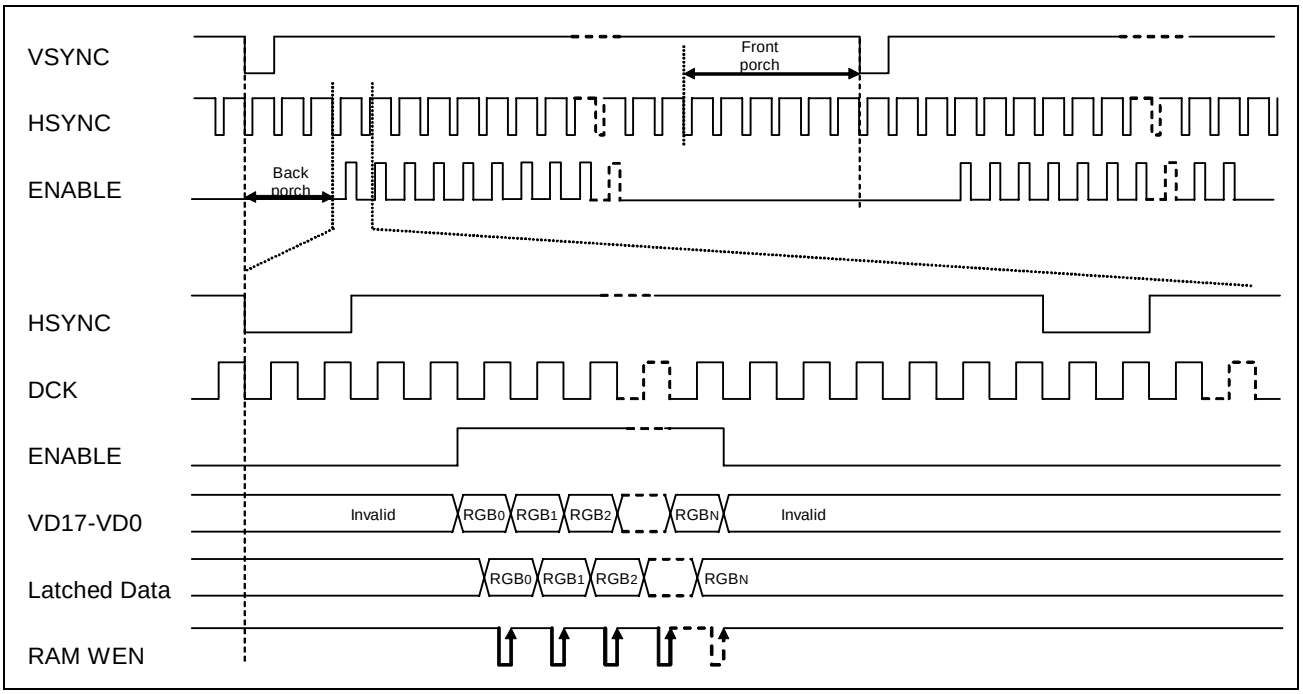


Fig. 5.2.3 Video signal data writing method in RGB Interface Mode 3

5.2.3 Address Counter

The address counter sets the addresses of the display data RAM for writing and reading.

Data is written pixel-wise into the DDRAM matrix of LDS285. The data for one pixel or two pixels is collected (RGB 8-8-8-bit), according to the data formats. As soon as this pixel-data information is complete the "Write access" is activated on the DDRAM. The locations of DDRAM are addressed by the address pointers. When MV = 0 (MV is one of register value controlled by instruction MADCTL), the address ranges are X=0 to X=239 (0EFhex) and Y=0 to Y=319 (13Fh). When MV = 1, the address ranges are X=0 to X=319(13Fh) and Y=0 to Y=239 (0EFh). Addresses outside these ranges are not allowed. Before writing to the DDRAM, a window where data will be written must be defined. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

For example the whole display contents will be written, the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=239 (0EFh), YE=319 (13Fh).

In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (MV=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS).

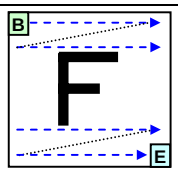
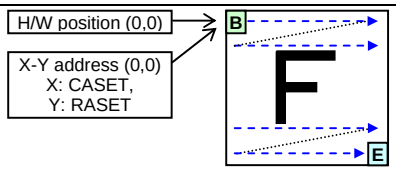
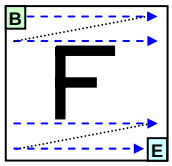
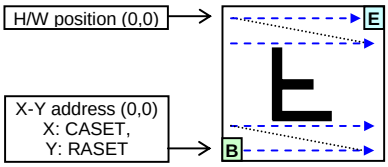
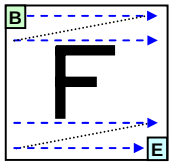
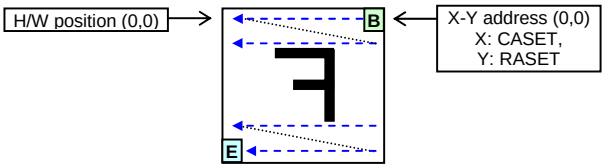
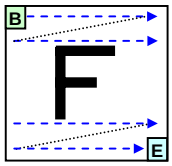
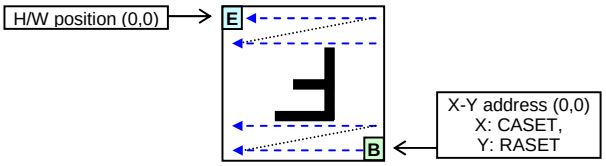
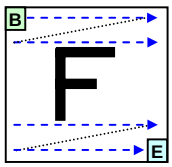
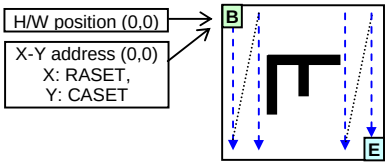
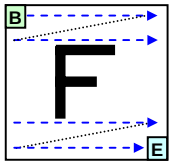
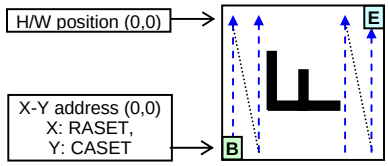
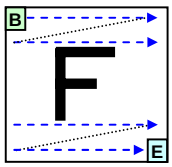
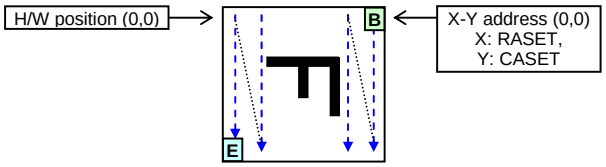
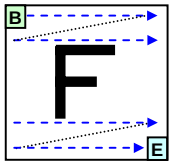
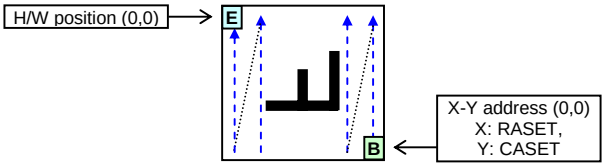
For flexibility in handling a wide variety of display architectures, the commands "CASET, RASET" and "MADCTL" (see section "6 INSTRUCTION DESCRIPTION"), define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. ***Fig. 5.2.4*** shows the available combinations of writing to the display RAM. When MX, MY and MV will be changed, the data must be rewritten to the display RAM.

For each image condition, the controls for the column and row counters apply as below:

Condition	Column Counter	Row Counter
When RAMWR/RAMRD command is accepted	Return to "Start Column (XS)"	Return to "Start Row (YS)"
Complete Pixel Read / Write action	Increment by 1	No change
The Column counter value is larger than "End Column (XE)"	Return to "Start Column (XS)"	Increment by 1
The Column counter value is larger than "End Column (XE)" and the Row counter value is larger than "End Row (YE)"	Return to "Start Column (XS)"	Return to "Start Row (YS)"

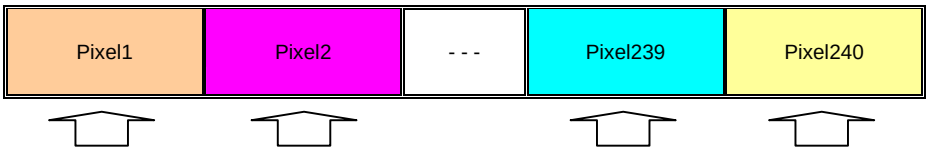
(where MY= 0)

Fig. 5.2.4 Frame Data Write Direction According to the MADCTR parameters (MV, MX and MY)

Display Data Direction	MADCTR Parameter			Image in the Host (MPU)	Image in the Driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

NOTE: MV=D5 parameter of MADCTL command, MX=D6 parameter of MADCTL command, MY=D7 parameter of MADCTL command

5.2.4 Memory Map

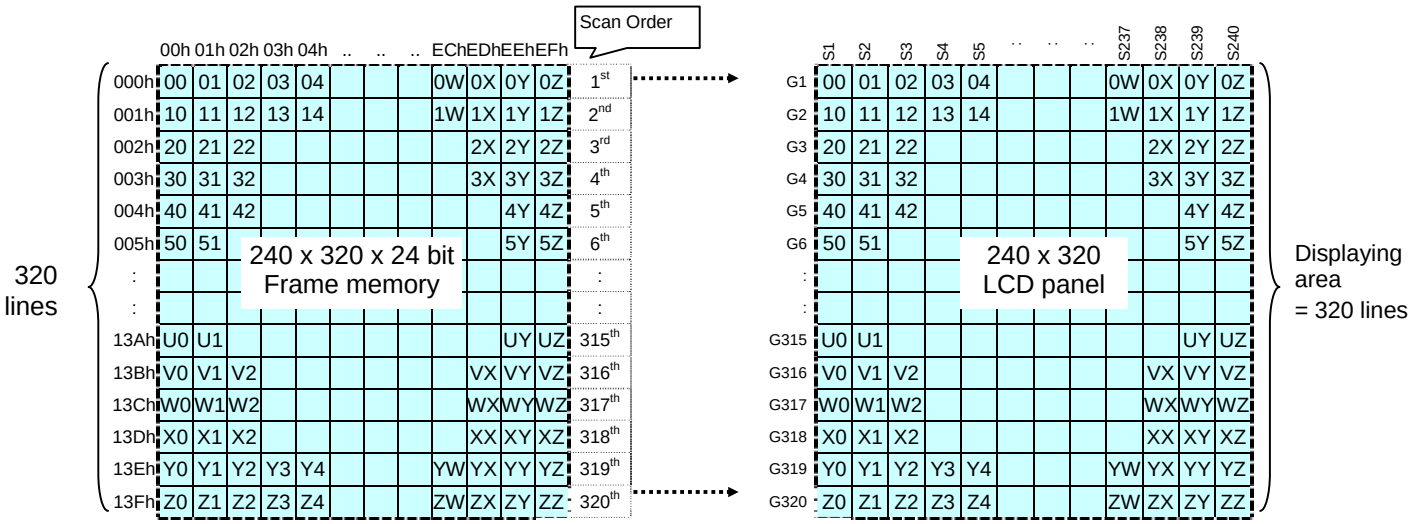


Source Out		S1	S2	S3	S4	S5	S6	- - -	S715	S716	S717	S718	S719	S720		
		RGB=0	RGB=1		RGB=0	RGB=1		RGB Order	RGB=0	RGB=1		RGB=0	RGB=1			
RA															SA	
MY=0	*MY=1*														*ML=0*	*ML=1*
0	319	R0$_{5-0}$	G0$_{5-0}$	B0$_{5-0}$	R1$_{5-0}$	G1$_{5-0}$	B1$_{5-0}$	- - -	R238$_{5-0}$	G238$_{5-0}$	B238$_{5-0}$	R239$_{5-0}$	G239$_{5-0}$	B239$_{5-0}$	0	319
1	318							- - -							1	318
2	317							- - -							2	317
3	316							- - -							3	316
4	315							- - -							4	315
5	314							- - -							5	314
6	313							- - -							6	313
7	312							- - -							7	312
8	311							- - -							8	311
9	310							- - -							9	310
10	309							- - -							10	309
11	308							- - -							11	308
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:
312	7							- - -							312	7
313	6							- - -							313	6
314	5							- - -							314	5
315	4							- - -							315	4
316	3							- - -							316	3
317	2							- - -							317	2
318	1							- - -							318	1
319	0							- - -				RN$_{5-0}$	GN$_{5-0}$	BN$_{5-0}$	319	0
CA	*MX=0*	0			1			- - -	238			239				
	MX=1	239			238			- - -	1			0				

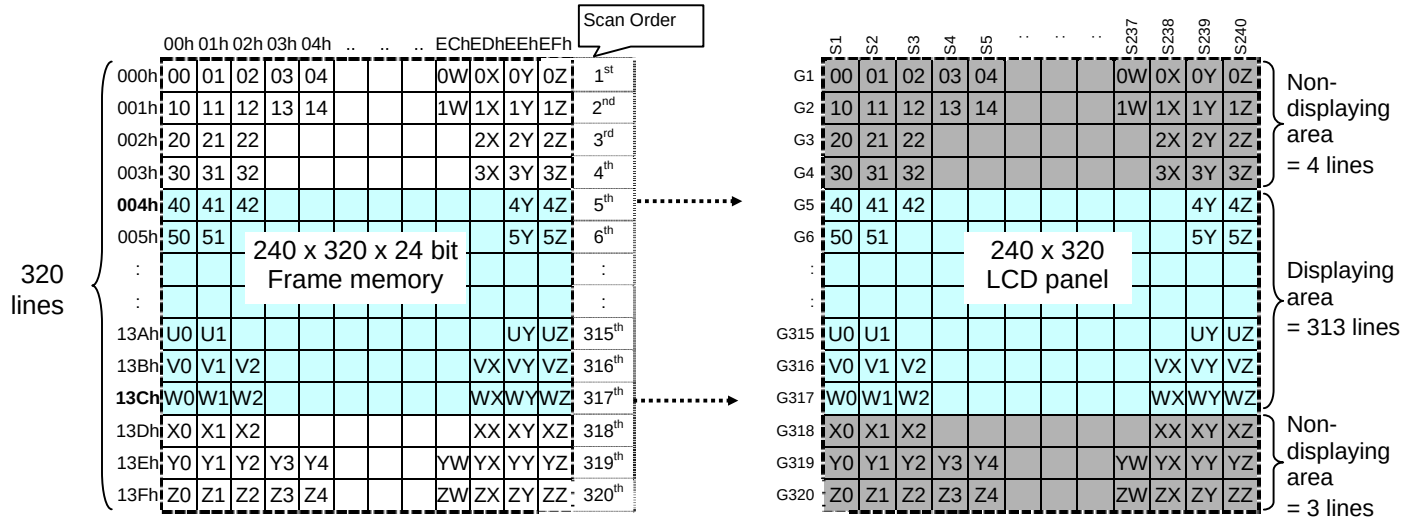
NOTE: RA = Row Address,
CA = Column Address,
SA = Scan Address,
MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTR command
MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTR command
ML = Scan direction parameter, D4 parameter of MADCTR command
RGB= Red, Green and Blue pixel position change, D3 parameter of MADCTR command

5.2.5 Normal Display On or Partial Mode On

In this mode, the content of the frame memory within an area where column pointer is 00h to 0EFh and page pointer is 00h to 13Fh is displayed.
To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).



Example2) Partial Display On: PSL [15:0] = 004h, PEL [15:0] = 13Ch, MADCTR (ML)=0

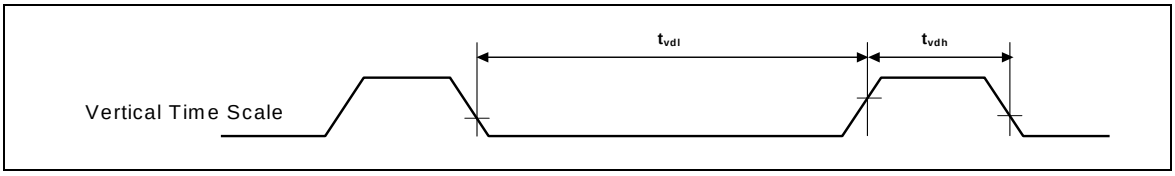


5.2.6 Tearing Effect Output Line

The Tearing Effect output line supplies a Panel synchronization signal to the MPU. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize DDRAM Writing when displaying video images.

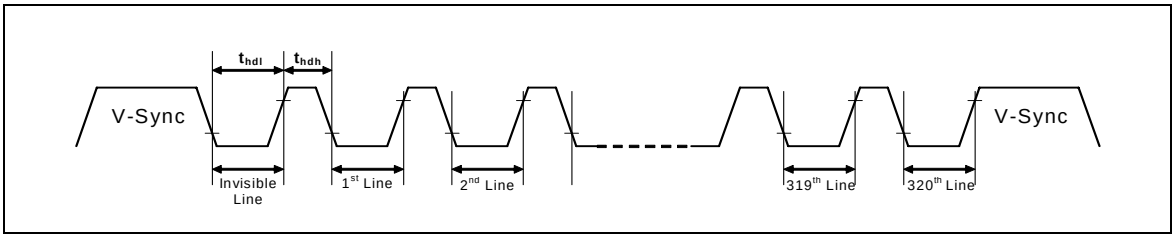
5.2.6.1 Tearing Effect Line Modes

Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:

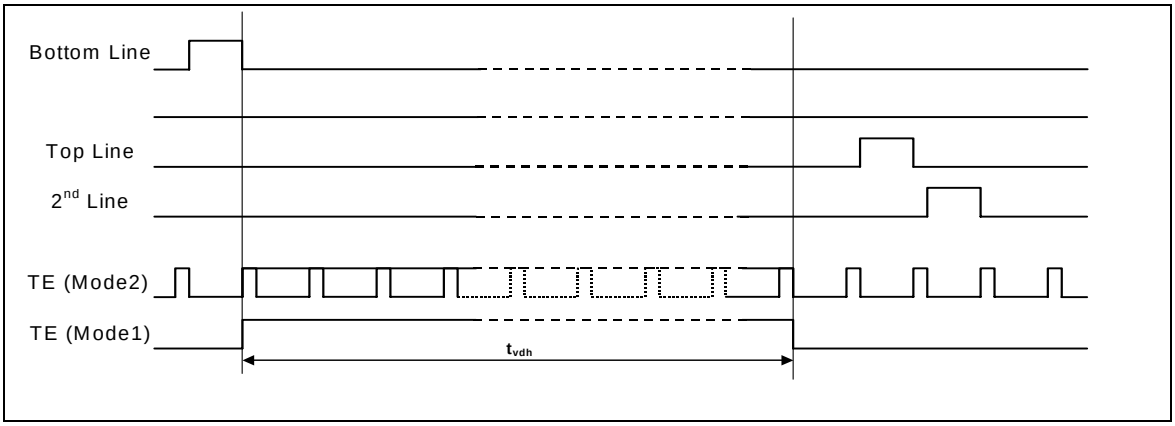


t_{vdh}= The LCD display is not updated from the DDRAM
t_{vdl} = The LCD display is updated from the DDRAM (except Invisible Line – see below)

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there are one V-sync and 320 H-sync pulses per field.



t_{hdh}= The LCD display is not updated from the Frame Memory
t_{hdl}= The LCD display is updated from the Frame Memory (except Invisible Line – see above)



Note: During Sleep In Mode, the Tearing Output Pin is active Low

5.2.6.2 Tearing Effect Line Timing

The Tearing Effect signal is described below:

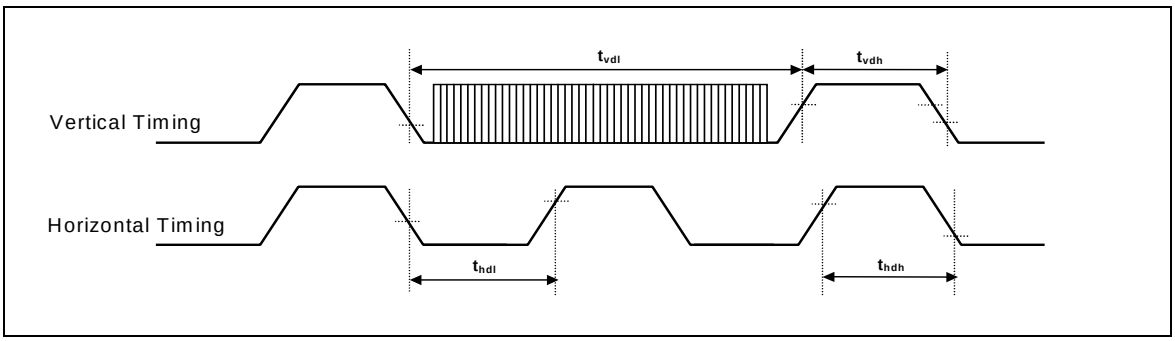


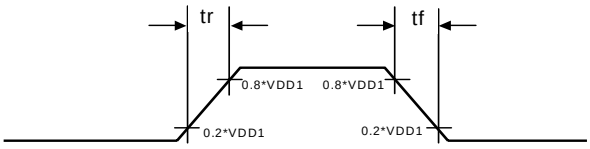
Table 5.2.19 AC characteristics of Tearing Effect Signal

Idle Mode Off (Frame Rate = 59Hz)

Symbol	Parameter	min	max	unit	description
t_{vdl}	Vertical Timing Low Duration	TBD	-	ms	
t_{vdh}	Vertical Timing High Duration	1000	-	μs	
t_{hdl}	Horizontal Timing Low Duration	TBD	-	μs	
t_{hdh}	Horizontal Timing High Duration	TBD	500	μs	

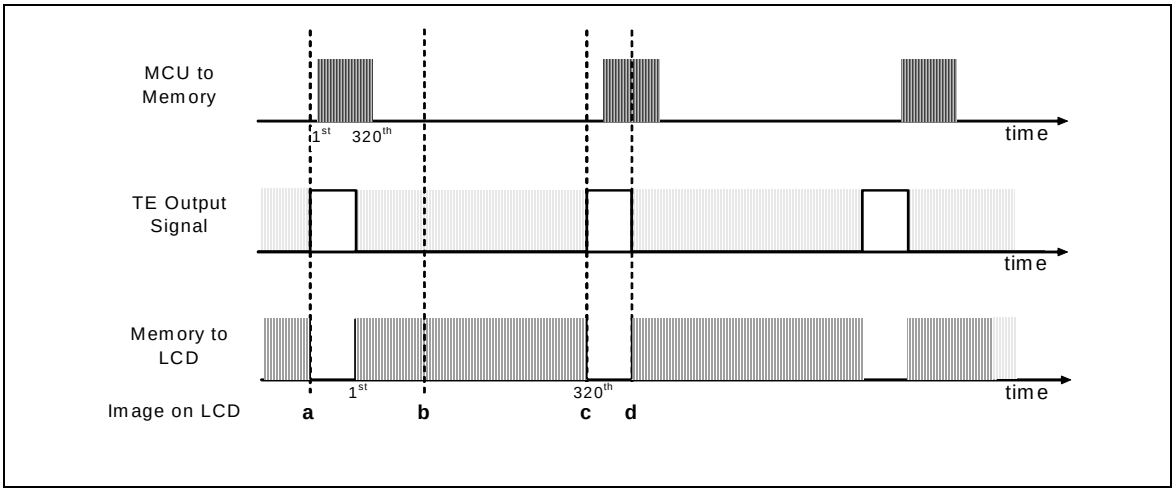
NOTE: The timings in Table 5.2.12 apply when MADCTL ML=0 and ML=1

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

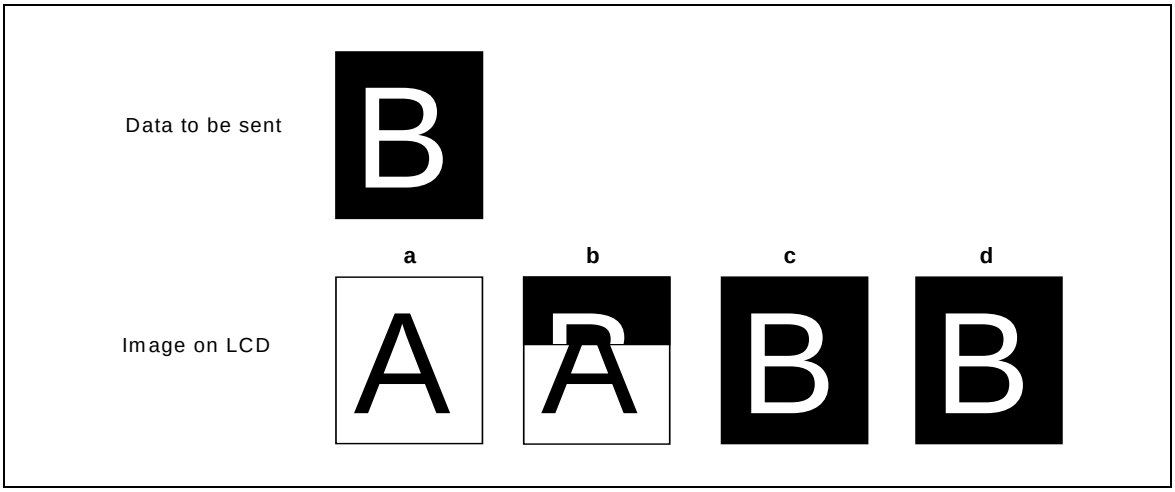


The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

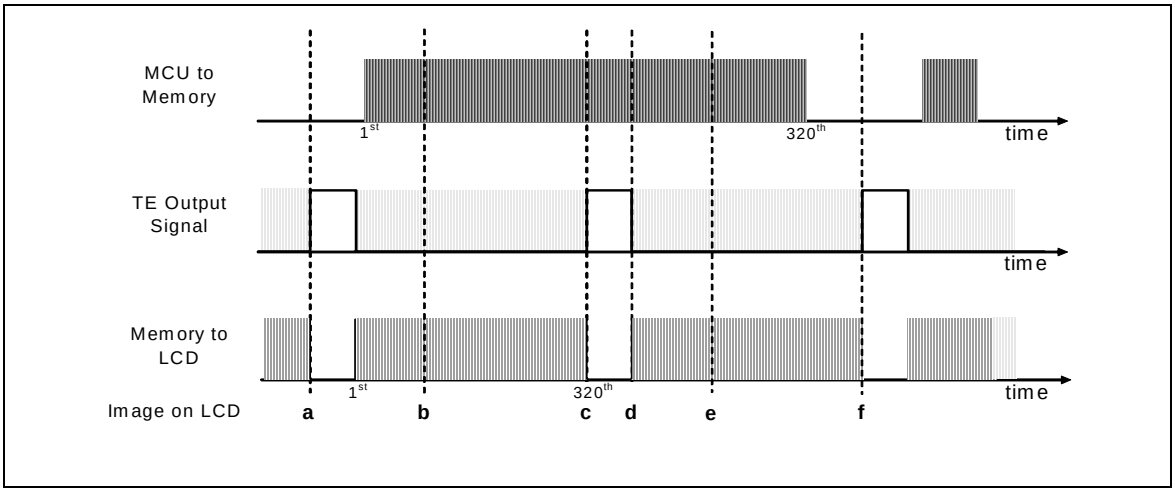
5.2.6.3 Example 1: MPU Write is faster than Panel Read.



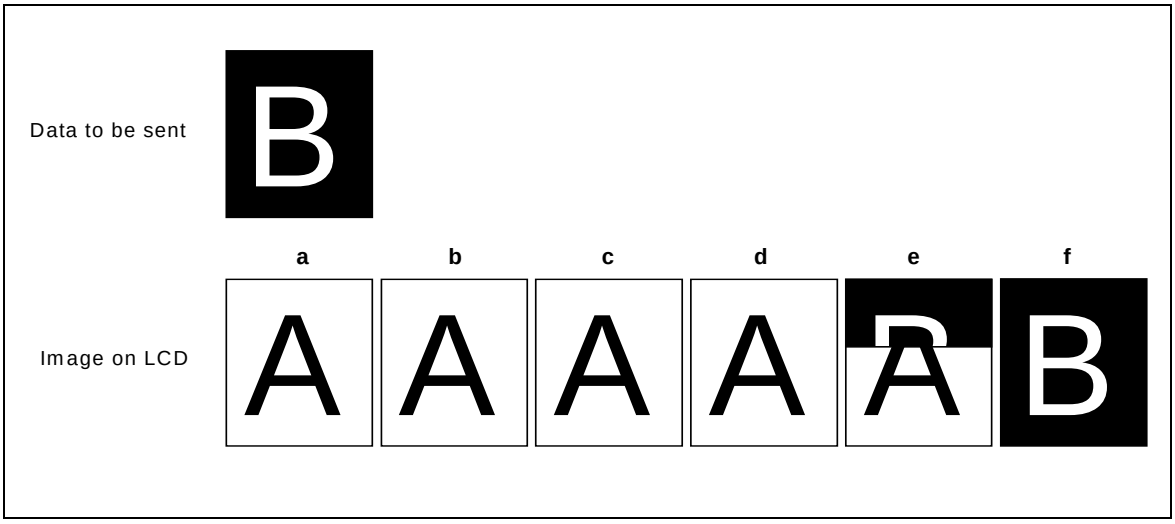
Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:



5.2.6.4 Example 2: MPU Write is slower than Panel Read.



The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the MPU to download the image behind the Panel Read pointer and to finish downloading during the subsequent Frame before the Read Pointer "catches" the MPU to Frame memory write position.



5.3 INSTRUCTION DECODER & REGISTER

The instruction decoder identifies command words arriving at the interface and routes the following data type bytes to their destination. The command set can be found in “6 INSTRUCTION DESCRIPTION” section.

5.4 SYSTEM CLOCK GENERATOR

The timing generator produces the various signals to drive the internal circuitry. Internal chip operation is not affected by operations on the data bus.

5.5 OSCILLATOR

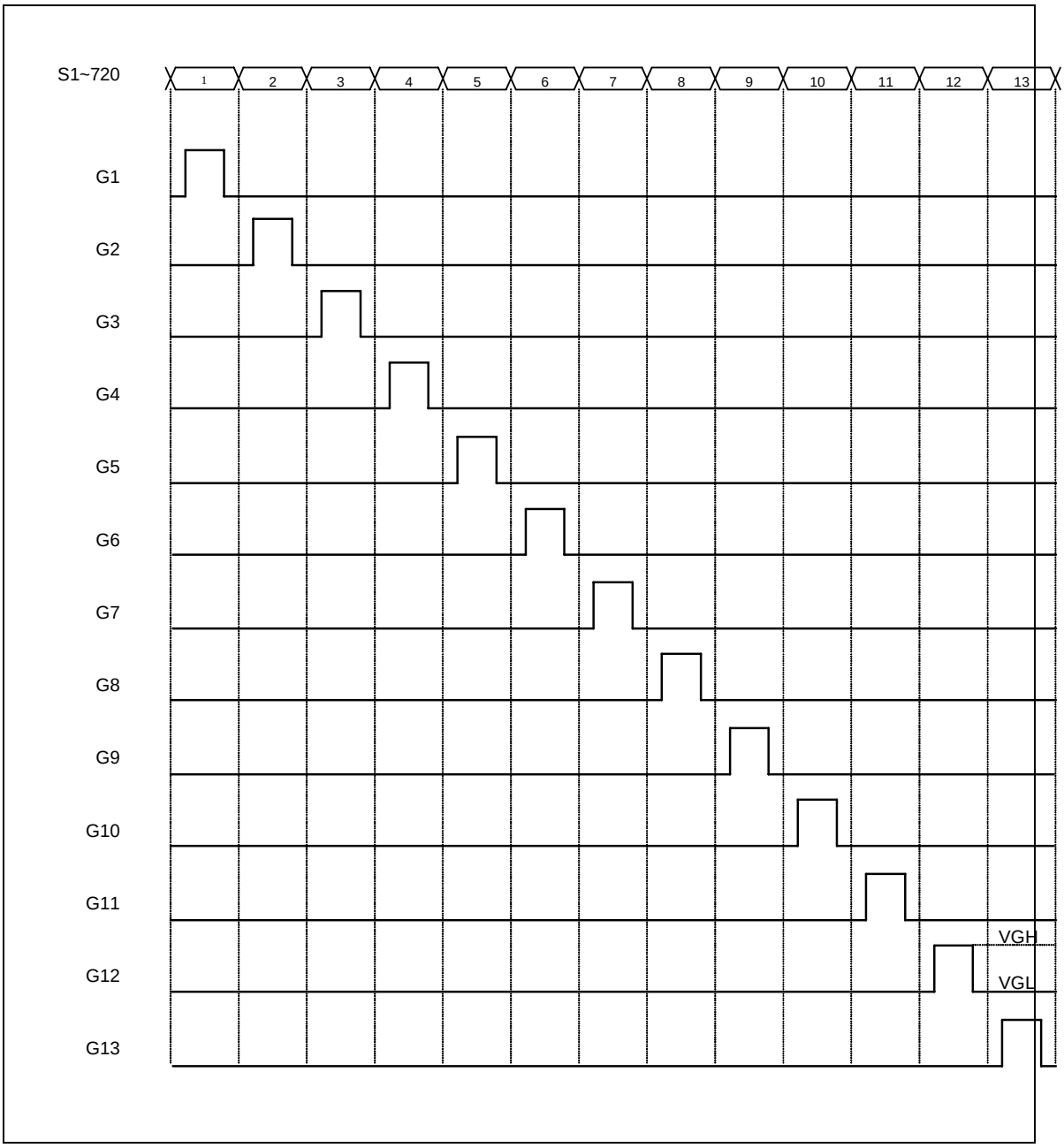
LDS285 has on-chip oscillator which does not require external components. This oscillator output signal is used for system clock generation for internal display operation

5.6 SOURCE DRIVER

The source driver block includes 240x3 source outputs (S1 to S720), which should be connected directly to the TFT-LCD. The source output signals are generated in the data processing block after the data is read out of the RAM and latched, which represent the simultaneous selected rows. When less then 720 sources are required the unused source outputs should be left open-circuit.

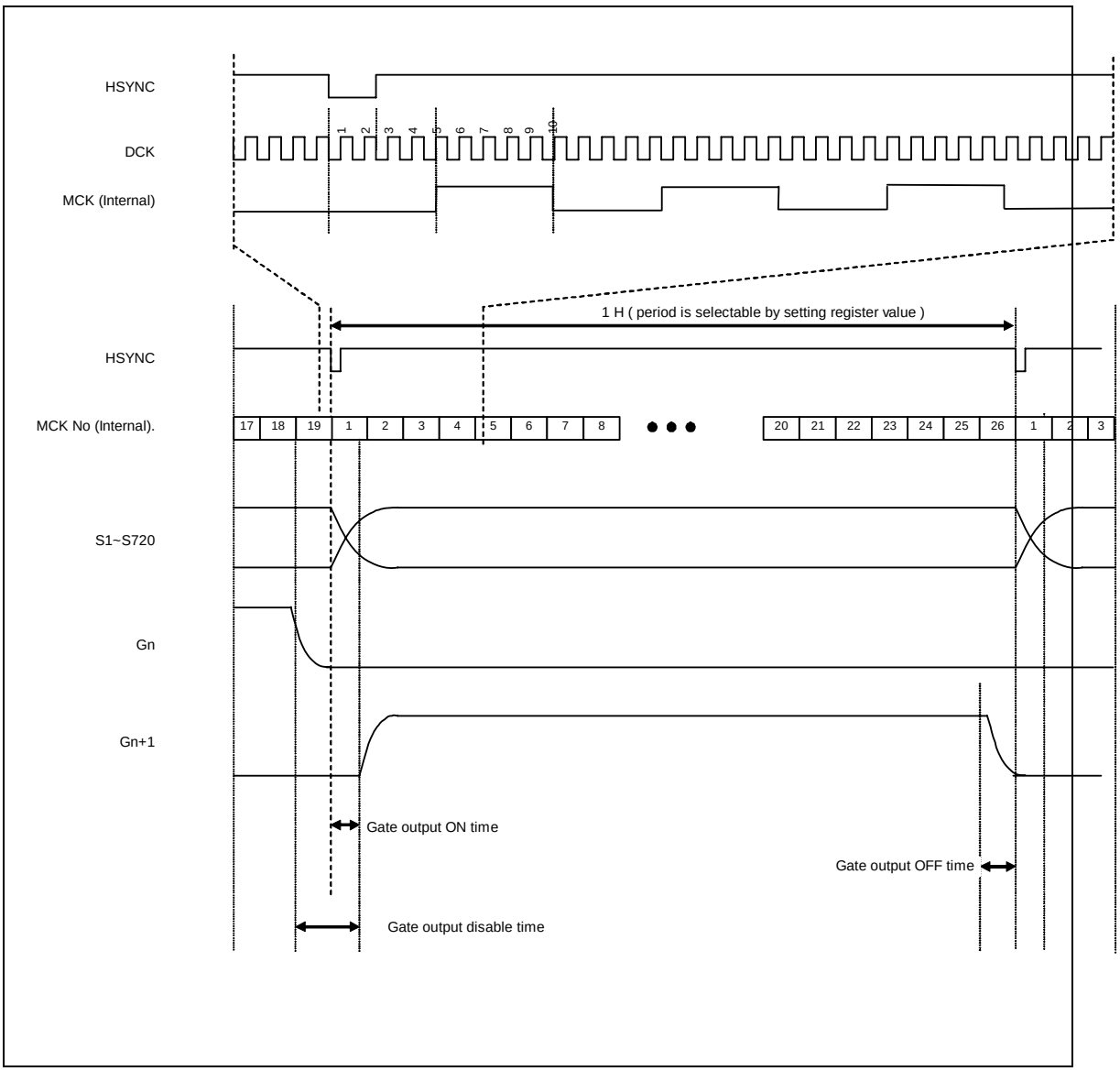
5.7 GATE DRIVER

The gate driver block includes 320 gate outputs (G1 to G320) which should be connected directly to the TFT-LCD.



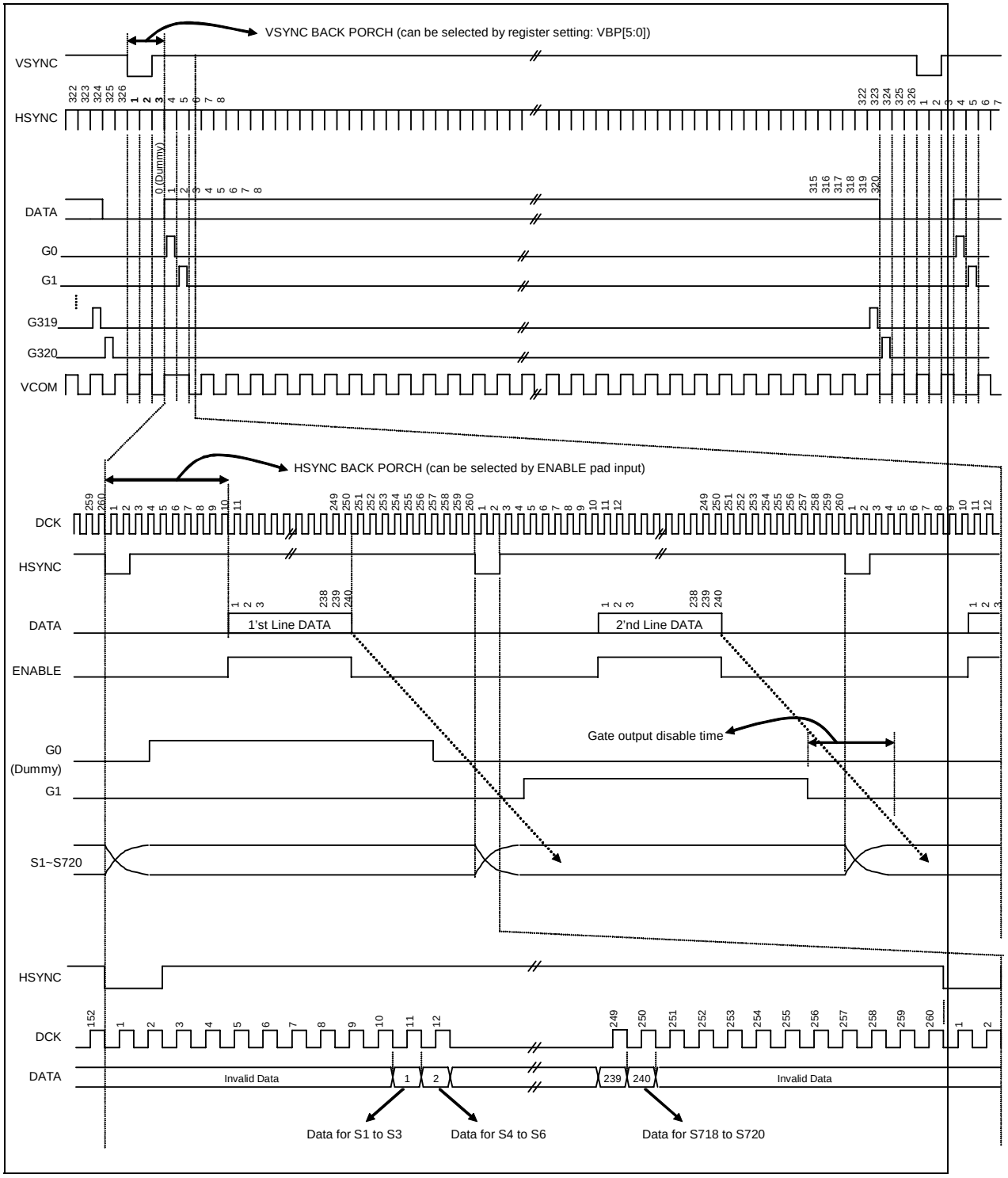
5.8 RGB INTERFACE TIMING DIAGRAM

5.8.1 Relationship between Input Signal and Output Signal (RGB I/F Mode 3)



5.8.2 Input / Output Timing Chart (G0->G320, S1->S720)

Horizontal valid data start time=10DCK, Vertical valid data start time=3HSYNC, 1 Line scan, Line inversion.



5.9 LCD POWER GENERATION CIRCUIT

5.9.1 LCD Power Generation Scheme

1. The boost voltage generated in LDS285 is shown as below. (Case=VS<4.2V)

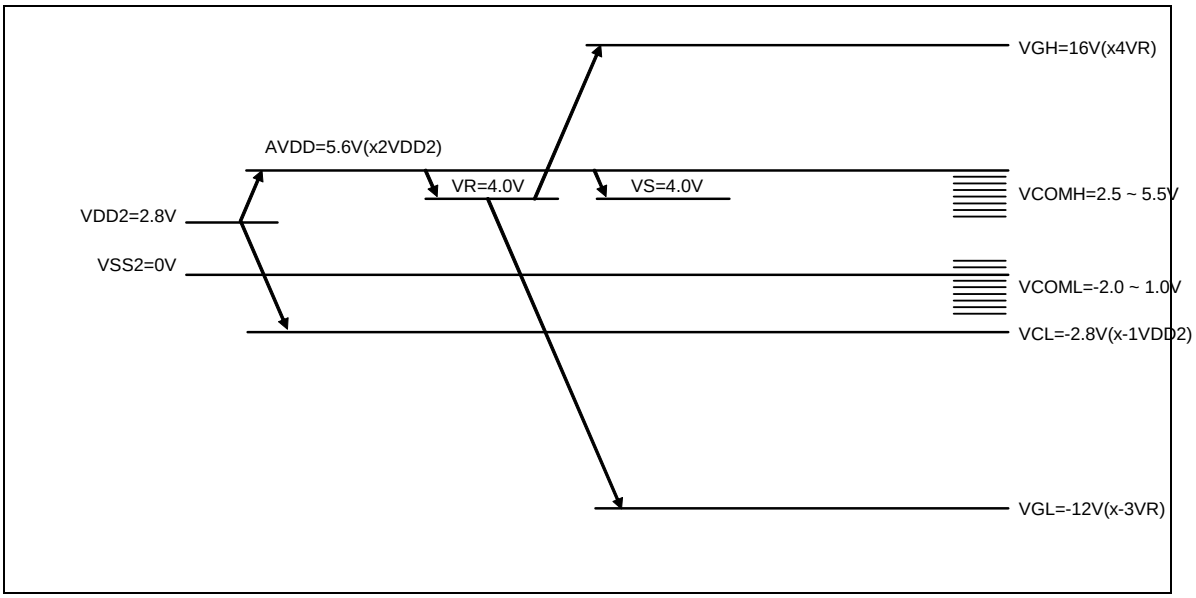


Fig. 5.9.1 LCD power generation scheme1

2. The boost voltage generated in LDS285 is shown as below. (Case=VS>4.2V)

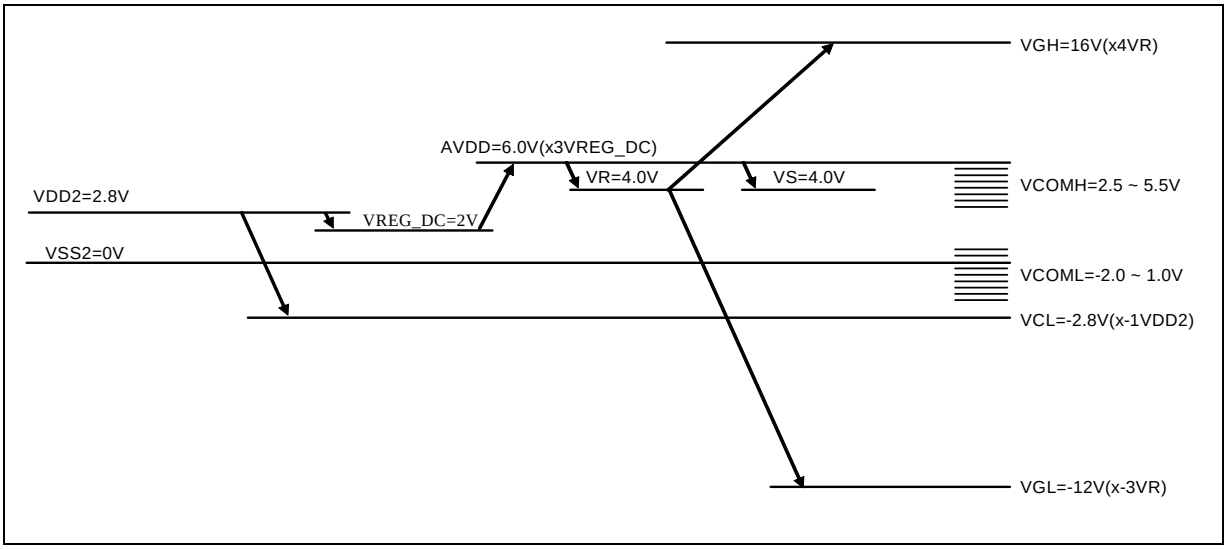


Fig. 5.9.2 LCD power generation scheme2(wide viewing angle)

5.9.2 Various Boosting Steps

The boost steps of each boosting voltage are selected according to how the external capacitors are connected. Different booster applications are shown as below.

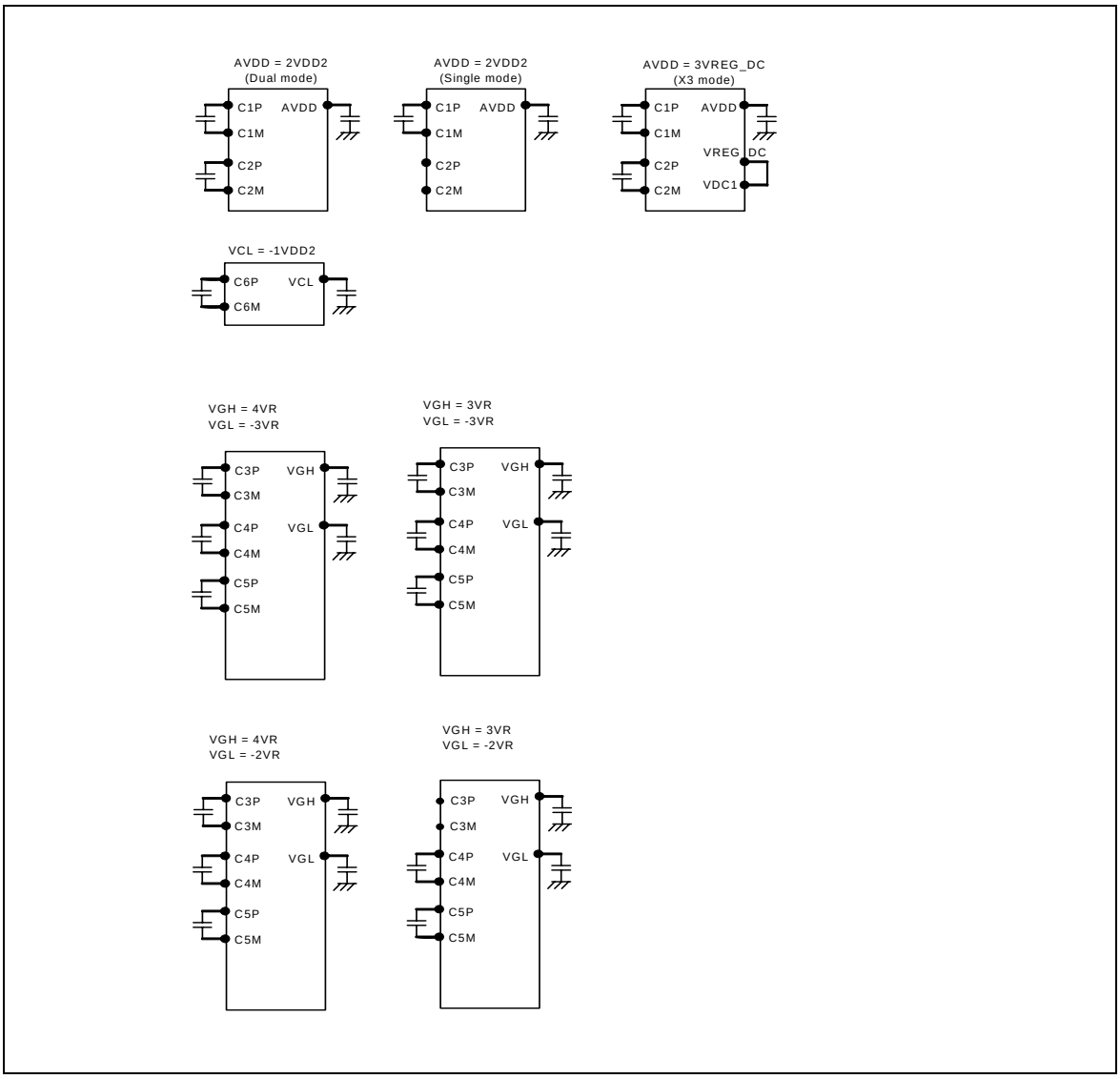


Fig. 5.9.3 Various boosting Step

5.9.3 Gray Voltage Generator

LDS285 supports 4 gamma curves. They can be selected by GAMSET command(26h).

5.9.3.1 Gamma Correction Curve Circuit

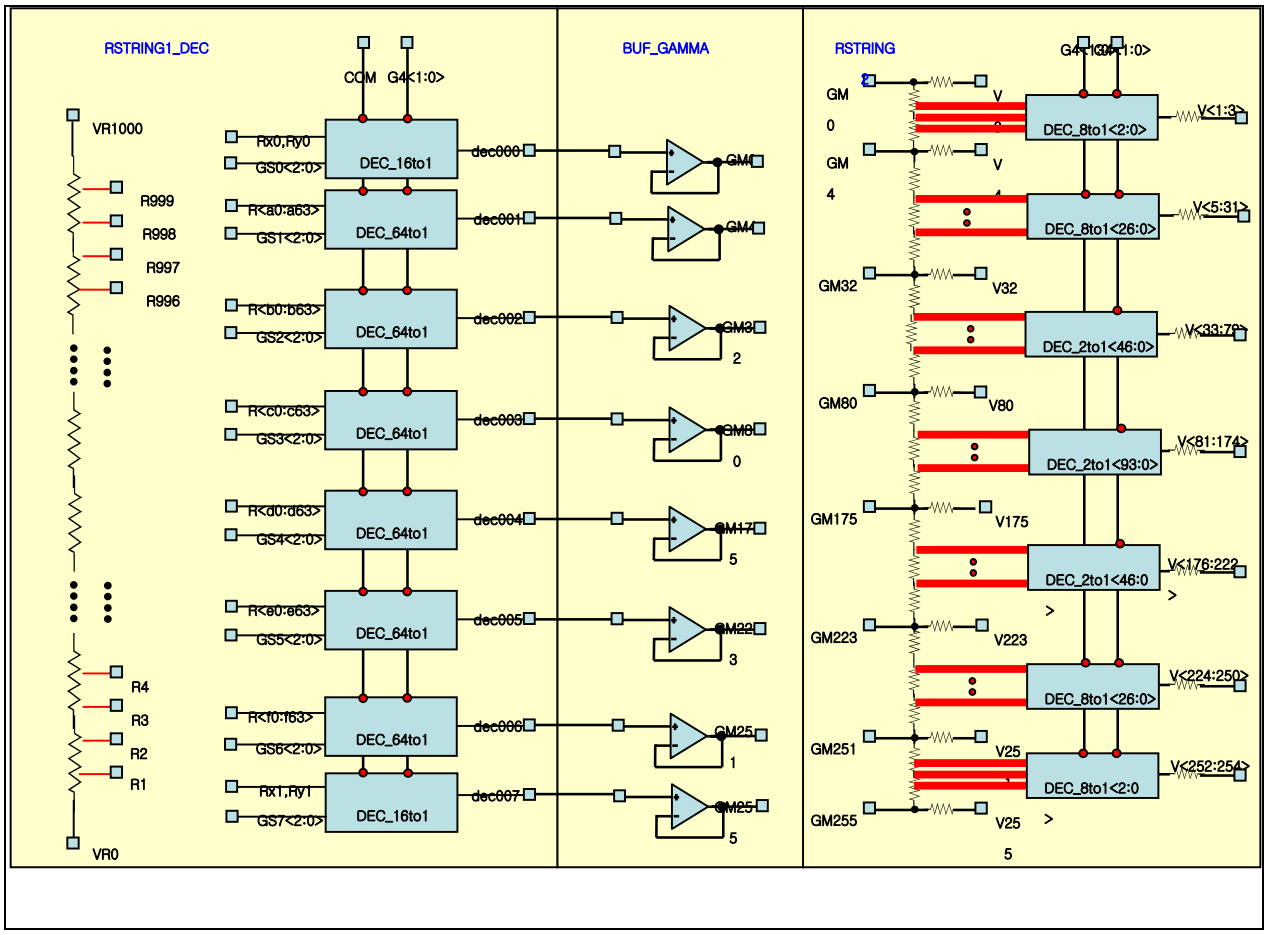


Fig. 5.9.4 Gamma Correction Curve cirsuit

5.9.3.2 Relationship between DDRAM Data and Output Voltages. (TBD)

Data (Hex)	Output Voltage when VS= V									
	VCOM = Low					VCOM = High				
	Gamma	1.0	1.8	2.2	2.5	Gamma	1.0	1.8	2.2	2.5
00	V0+					V0-				
01	V1+					V1-				
02	V2+					V2-				
03	V3+					V3-				
04	V4+					V4-				
05	V5+					V5-				
06	V6+					V6-				
07	V7+					V7-				
08	V8+					V8-				
09	V9+					V9-				
0A	V10+					V10-				
0B	V11+					V11-				
0C	V12+					V12-				
0D	V13+					V13-				
0E	V14+					V14-				
0F	V15+					V15-				
10	V16+					V16-				
11	V17+					V17-				
12	V18+					V18-				
13	V19+					V19-				
14	V20+					V20-				
15	V21+					V21-				
16	V22+					V22-				
17	V23+					V23-				
18	V24+					V24-				
19	V25+					V25-				
1A	V26+					V26-				
1B	V27+					V27-				
1C	V28+					V28-				
1D	V29+					V29-				
1E	V30+					V30-				
1F	V31+					V31-				
20	V32+					V32-				
21	V33+					V33-				
22	V34+					V34-				
23	V35+					V35-				
24	V36+					V36-				
25	V37+					V37-				
26	V38+					V38-				
27	V39+					V39-				
28	V40+					V40-				
29	V41+					V41-				
2A	V42+					V42-				
2B	V43+					V43-				
2C	V44+					V44-				
2D	V45+					V45-				
2E	V46+					V46-				
2F	V47+					V47-				
30	V48+					V48-				
31	V49+					V49-				
32	V50+					V50-				
33	V51+					V51-				
34	V52+					V52-				
35	V53+					V53-				
36	V54+					V54-				
37	V55+					V55-				
38	V56+					V56-				
39	V57+					V57-				
3A	V58+					V58-				
3B	V59+					V59-				
3C	V60+					V60-				
3D	V61+					V61-				
3E	V62+					V62-				
3F	V63+					V63-				
40	V64+					V64-				
41	V65+					V65-				
42	V66+					V66-				
43	V67+					V67-				
44	V68+					V68-				
45	V69+					V69-				
46	V70+					V70-				
47	V71+					V71-				

48	V72+					V72-				
49	V73+					V73-				
4A	V74+					V74-				
4B	V75+					V75-				
4C	V76+					V76-				
4D	V77+					V77-				
4E	V78+					V78-				
4F	V79+					V79-				
50	V80+					V80-				
51	V81+					V81-				
52	V82+					V82-				
53	V83+					V83-				
54	V84+					V84-				
55	V85+					V85-				
56	V86+					V86-				
57	V87+					V87-				
58	V88+					V88-				
59	V89+					V89-				
5A	V90+					V90-				
5B	V91+					V91-				
5C	V92+					V92-				
5D	V93+					V93-				
5E	V94+					V94-				
5F	V95+					V95-				
60	V96+					V96-				
61	V97+					V97-				
62	V98+					V98-				
63	V100+					V100-				
64	V101+					V101-				
65	V102+					V102-				
66	V103+					V103-				
67	V104+					V104-				
68	V105+					V105-				
69	V106+					V106-				
6A	V107+					V107-				
6B	V108+					V108-				
6C	V109+					V109-				
6D	V110+					V110-				
6E	V111+					V111-				
6F	V112+					V112-				
70	V113+					V113-				
71	V114+					V114-				
72	V115+					V115-				
73	V116+					V116-				
74	V117+					V117-				
75	V118+					V118-				
76	V119+					V119-				
77	V120+					V120-				
78	V121+					V121-				
79	V122+					V122-				
7A	V123+					V123-				
7B	V124+					V124-				
7C	V125+					V125-				
7D	V126+					V126-				
7E	V127+					V127-				
7F	V127+					V127-				
80	V128+					V128-				
81	V129+					V129-				
82	V130+					V130-				
83	V131+					V131-				
84	V132+					V132-				
85	V133+					V133-				
86	V134+					V134-				
87	V135+					V135-				
88	V136+					V136-				
89	V137+					V137-				
8A	V138+					V138-				
8B	V139+					V139-				
8C	V140+					V140-				
8D	V141+					V141-				
8E	V142+					V142-				
8F	V143+					V143-				
90	V144+					V144-				
91	V145+					V145-				
92	V146+					V146-				
93	V147+					V147-				
94	V148+					V148-				
95	V149+					V149				

96	V150+				2.097	V150-				
97	V151+				2.056	V151-				
98	V152+				2.015	V152-				
99	V153+				1.975	V153-				
9A	V154+				1.934	V154-				
9B	V155+				1.893	V155-				
9C	V156+				1.853	V156-				
9D	V157+				1.817	V157-				
9E	V158+				1.782	V158-				
9F	V159+				1.746	V159-				
A0	V160+				1.711	V160-				
A1	V161+				1.676	V161-				
A2	V162+				1.640	V162-				
A3	V163+				1.605	V163-				
A4	V164+				1.575	V164-				
A5	V165+				1.545	V165-				
A6	V166+				1.515	V166-				
A7	V167+				1.485	V167-				
A8	V168+				1.455	V168-				
A9	V169+				1.425	V169-				
AA	V170+				1.395	V170-				
AB	V171+				1.363	V171-				
AC	V172+				1.330	V172-				
AD	V173+				1.298	V173-				
AE	V174+				1.265	V174-				
AF	V175+				1.233	V175-				
B0	V176+				1.200	V176-				
B1	V177+				1.166	V177-				
B2	V178+				1.131	V178-				
B3	V179+				1.097	V179-				
B4	V180+				1.062	V180-				
B5	V181+				1.028	V181-				
B6	V182+				0.985	V182-				
B7	V183+				0.943	V183-				
B8	V184+				0.900	V184-				
B9	V185+				0.851	V185-				
BA	V186+				0.803	V186-				
BB	V187+				0.750	V187-				
BC	V188+				0.683	V188-				
BD	V189+				0.608	V189-				
BE	V190+				0.518	V190-				
BF	V191+				0.368	V191-				
C0	V192+				3.540	V192-				
C1	V193+				3.398	V193-				
C2	V194+				3.383	V194-				
C3	V195+				3.353	V195-				
C4	V196+				3.293	V196-				
C5	V197+				3.203	V197-				
C6	V198+				3.128	V198-				
C7	V199+				3.053	V199-				
C8	V200+				2.963	V200-				
C9	V201+				2.873	V201-				
CA	V202+				2.783	V202-				
CB	V203+				2.717	V203-				
CC	V204+				2.651	V204-				
CD	V205+				2.585	V205-				
CE	V206+				2.519	V206-				
CF	V207+				2.453	V207-				
D0	V208+				2.400	V208-				
D1	V209+				2.348	V209-				
D2	V210+				2.295	V210-				
D3	V211+				2.243	V211-				
D4	V212+				2.190	V212-				
D5	V213+				2.138	V213-				
D6	V214+				2.097	V214-				
D7	V215+				2.056	V215-				
D8	V216+				2.015	V216-				
D9	V217+				1.975	V217-				
DA	V218+				1.934	V218-				
DB	V219+				1.893	V219-				
DC	V220+				1.853	V220-				
DD	V221+				1.817	V221-				
DE	V222+				1.782	V222-				
DF	V223+				1.746	V223-				
E0	V224+				1.711	V224-				
E1	V225+				1.676	V225-				
E2	V226+				1.640	V226-				
E3	V227+				1.605	V227-				

E4	V228+					V228-				
E5	V229+					V229-				
E6	V230+					V230-				
E7	V231+					V231-				
E8	V232+					V232-				
E9	V233+					V233-				
EA	V234+					V234-				
EB	V235+					V235-				
EC	V236+					V236-				
ED	V237+					V237-				
EE	V238+					V238-				
EF	V239+					V239-				
F0	V240+					V240-				
F1	V241+					V241-				
F2	V242+					V242-				
F3	V243+					V243-				
F4	V244+					V244-				
F5	V245+					V245-				
F6	V246+					V246-				
F7	V247+					V247-				
F8	V248+					V248-				
F9	V249+					V249-				
FA	V250+					V250-				
FB	V251+					V251-				
FC	V252+					V252-				
FD	V253+					V253-				
FE	V254+					V254-				
FF	V255+					V255-				

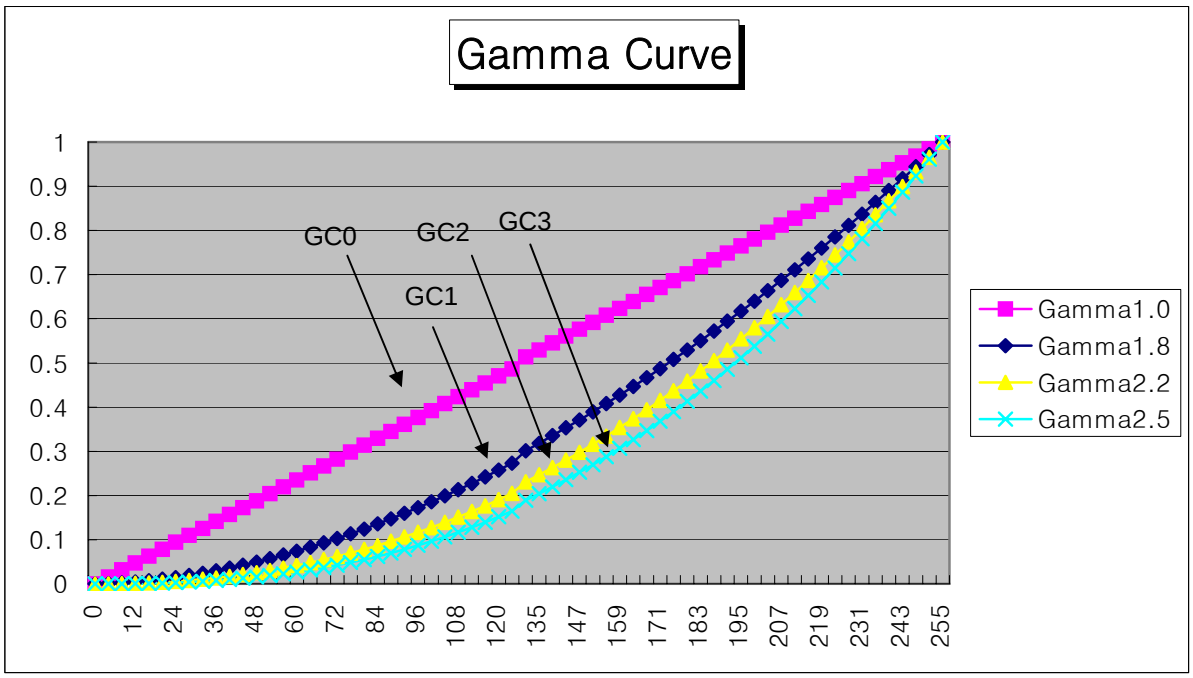


Fig. 5.9.5 Gamma Curve according to the GC0 to GC3 bit (TBD)

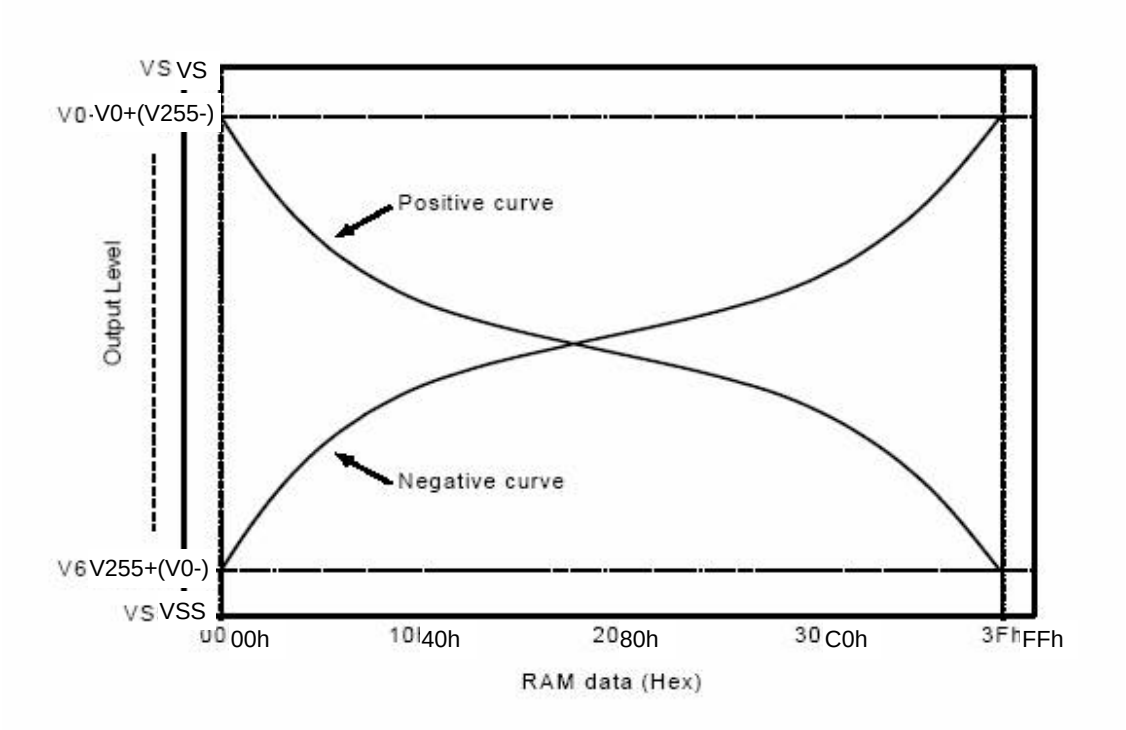


Fig. 5.9.6 Relationship between DDRAM data and output level

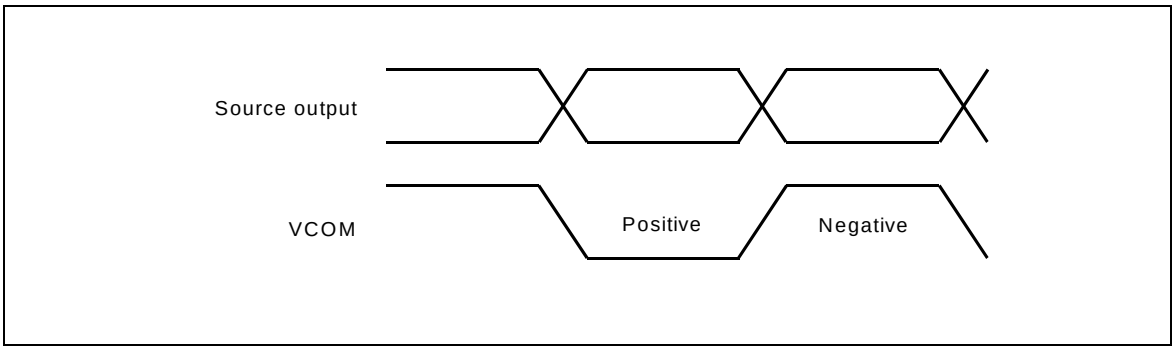


Fig. 5.9.7 Relationship between source output and VCOM

5.9.4 Temperature Compensation

The LDS285 has a built-in temperature compensation circuits. By the temperature compensation circuits, user can obtain a higher quality in the various temperature ranges.

5.10 POWER ON/OFF SEQUENCE

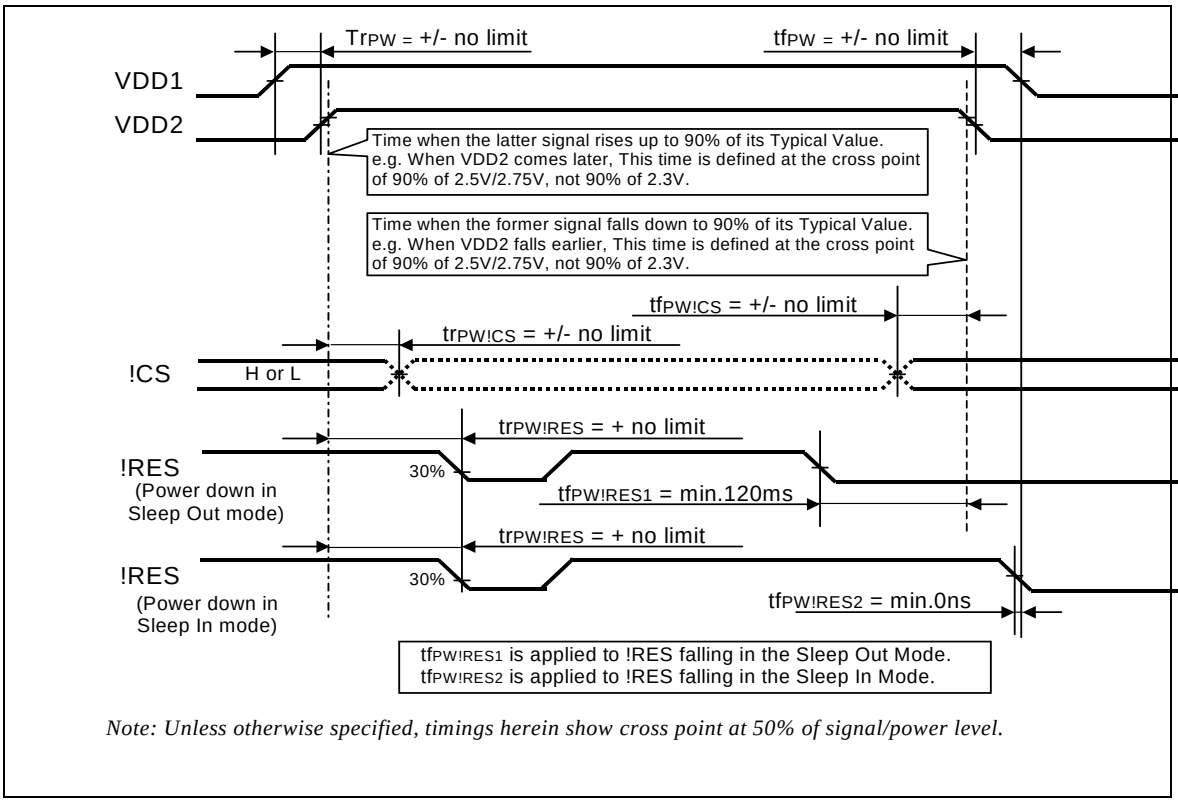
VDD1 and VDD2 can be applied in any order.
VDD2 and VDD1 can be powered down in any order.
During power off, if LCD is in the Sleep Out mode, VDD2 and VDD1 must be powered down minimum 120msec after RESB has been released.
During power off, if LCD is in the Sleep In mode, VDD1 or VDD2 can be powered down minimum 0msec after RESB has been released.
!SCE can be applied at any timing or can be permanently grounded. RESB has priority over !SCE.

There will be no damage to the display module if the power sequences are not met.
There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
There will be no abnormal visible effects on the display between ending the Power On Sequence and receiving Sleep Out command and between receiving Sleep In command and starting the Power Off Sequence.
If RESB line is not held stable by host during Power On Sequence as defined in Sections 5.10.21, and 5.10.2, then it will be necessary to apply a Hardware Reset (RESB) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below:

5.10.1 Case 1 – RESB line is held High or Unstable by Host at Power On

If RESB line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VDD2 and VDD1 have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

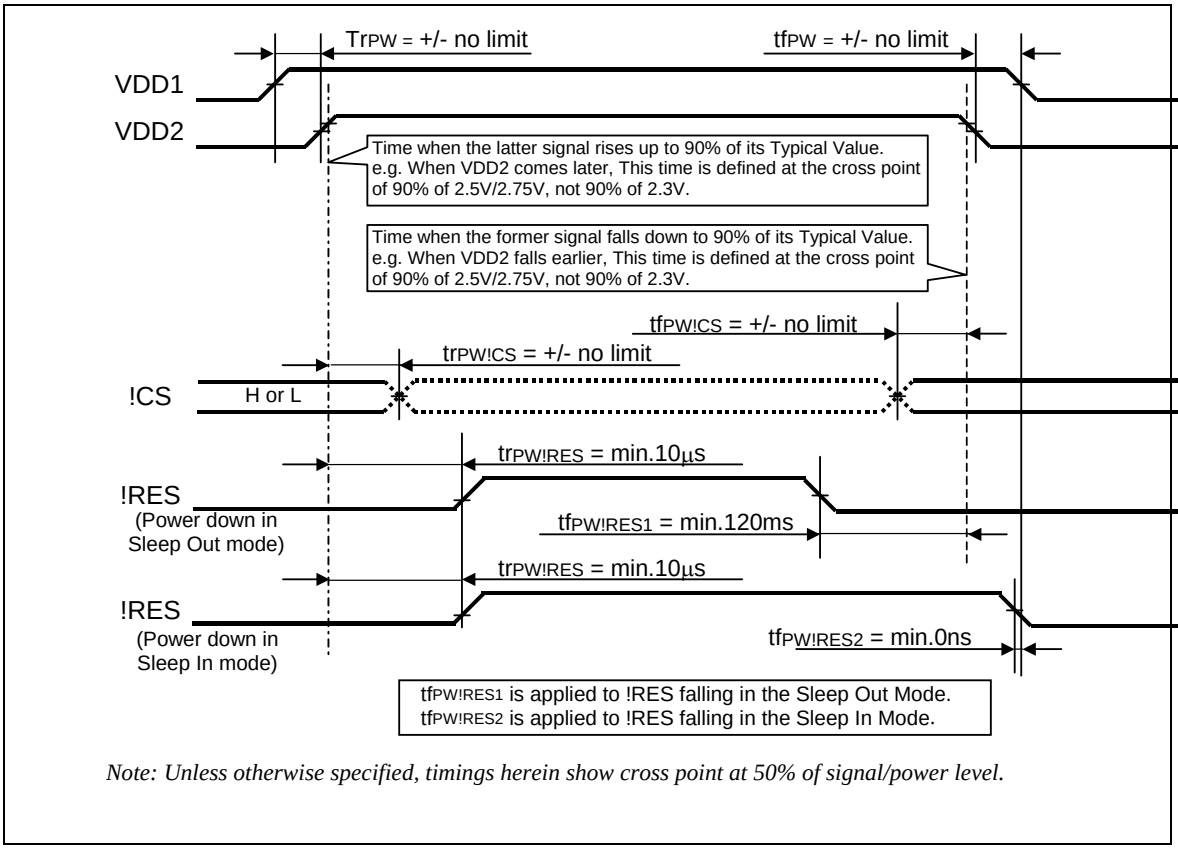


Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Fig. 5.10.1 RESB line is held high or unstable by Host at Power on

5.10.2 Case 2 – RESB line is held Low by host at Power On

If RESB line is held Low (and stable) by the host during Power On, then the RESB must be held low for minimum 10μsec after both VDD2 and VDD1 have been applied.



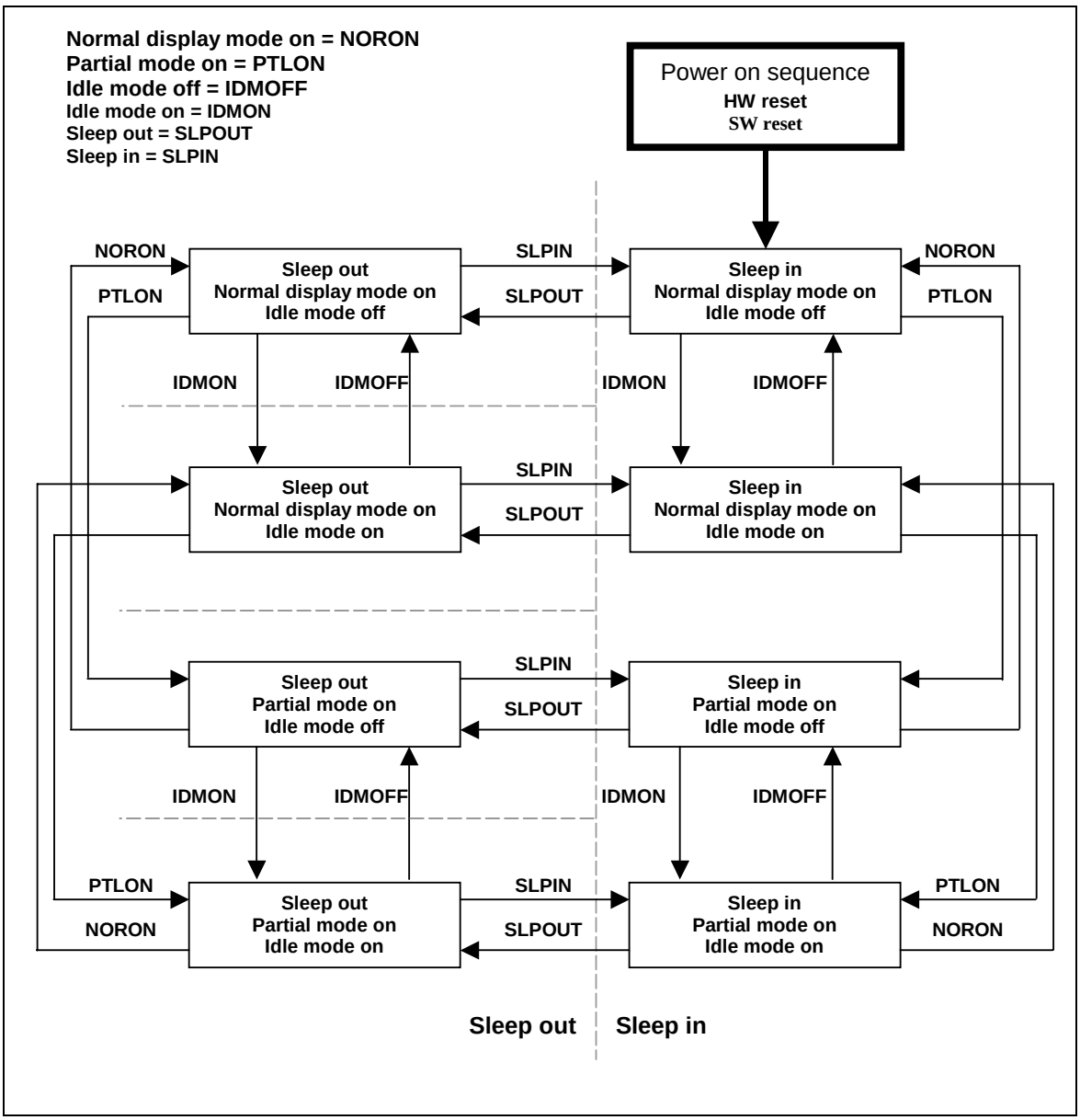
Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Fig. 5.10.2 RESB line is held low by Host at Power on

5.11 UNCONTROLLED POWER OFF

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off the display will go blank and there will not be any visible effects within 1 second on the display (blank display) and remains blank until "Power On Sequence" powers it up.

5.12 POWER FLOW CHART FOR DIFFERENT POWER MODES



Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

2: There is not any limitation, which is not specified by this spec, when there is changing from one power mode to another power mode

Fig. 5.12.1 Power flow char for different Power Modest

5.13 INPUT / OUTPUT PIN STATE

5.13.1 Output or Bi-directional (I/O) Pins

Output or Bi-directional pins	After Power On	After Hardware Reset	After Software Reset
TE	Low	Low	Low
D23 to D0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)
TEST1, TEST4	X	X	X

Note: There will be no output from D23-D0 during Power On/Off sequence, Hardware Reset and Software Reset.

5.13.2 Input Pins

Input pins	During Power On Process	After Power On	After Hardware Reset	After Software Reset	During Power Off Process
RESB	See Section 5.10	Input valid	Input valid	Input valid	See Section 5.10
CSB	Input invalid	Input valid	Input valid	Input valid	Input invalid
DC	Input invalid	Input valid	Input valid	Input valid	Input invalid
WRB	Input invalid	Input valid	Input valid	Input valid	Input invalid
RDB	Input invalid	Input valid	Input valid	Input valid	Input invalid
D23 to D0	Input invalid	Input valid	Input valid	Input valid	Input invalid
VSYNC, HSYNC , DCK, ENABLE, VD0	Input invalid	Input valid	Input valid	Input valid	Input invalid
SRGB, SINV, SMX,SMY, P68, BS2, BS1,BS0, TGS,EXTC,FRM,PSEL, OSC,TEST2, TEST3	Input invalid	Input valid	Input valid	Input valid	Input invalid

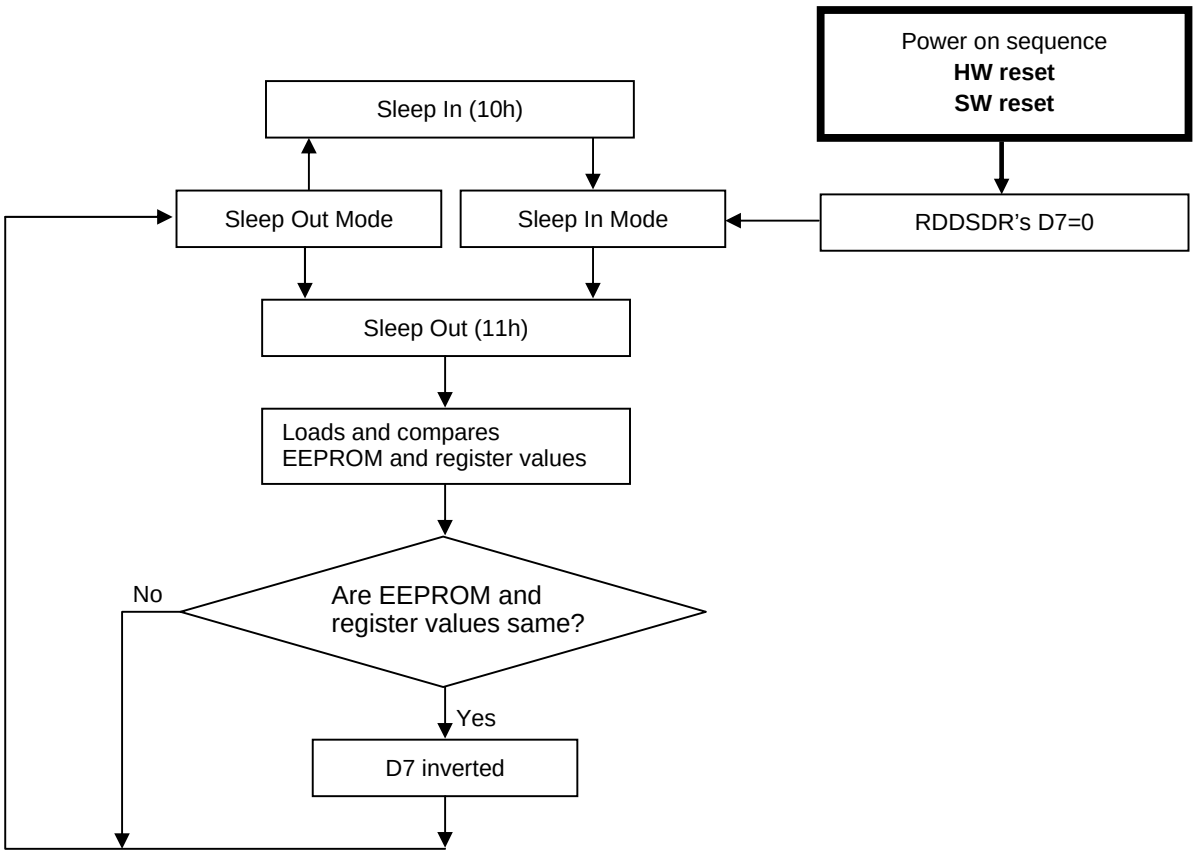
5.14 SLEEP OUT –COMMAND AND SELF-DIAGNOSTIC FUNCTIONS OF THE DISPLAY MODULE

5.14.1 Register loading Detection

Sleep Out-command (See section 6.1.13 “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EEPROM (or similar device) to registers of the display controller is working properly.

There are compared factory values of the EEPROM and register values of the display controller by the display controller. If those both values (EEPROM and register values) are same, there is inverted (=increased by 1) a bit, which is defined in command 6.1.11 “Read Display Self-Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (= increased by 1).

The flow chart for this internal function is following:



Note: There is not compared and loaded register values, which can be changed by user (00h to AFh and DAh to DDh), by the display module.

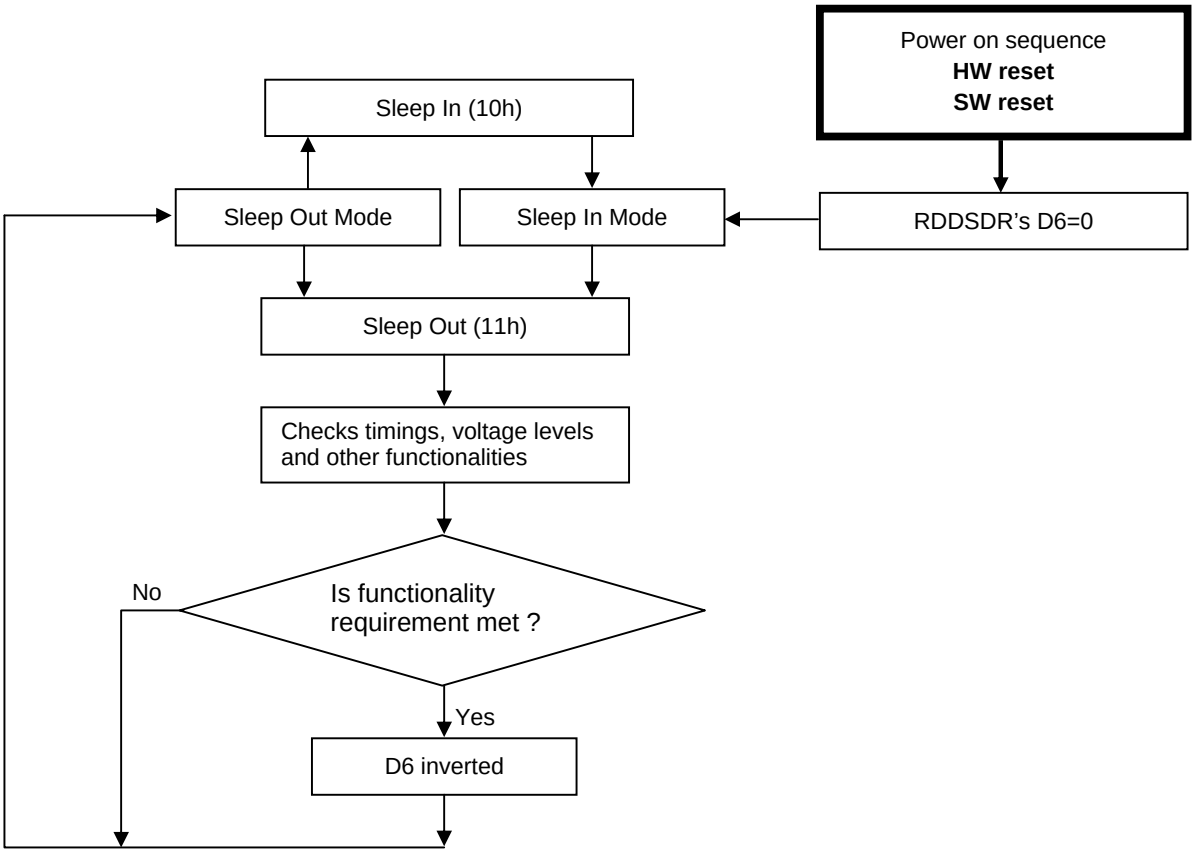
Fig. 5.14.1 Regist er loading Detection Flow chart

5.14.2 Functionality Detection

Sleep Out-command (See section 6.1.13 “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirement is met, there is inverted (= increased by 1) a bit, which defined in command 6.1.11 “Read Display Self- Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= increased by 1).

The flow chart for this internal function is following:



Note: It is needed 120msec after Sleep Out -command, when there is changing from Sleep In –mode to Sleep Out -mode, before it is possible to check if functionality requirements are met and a value of RDDSDR’s D6 is valid. Otherwise, there is 5msec delay for D6’s value, when Sleep Out –command is sent in Sleep Out -mode.

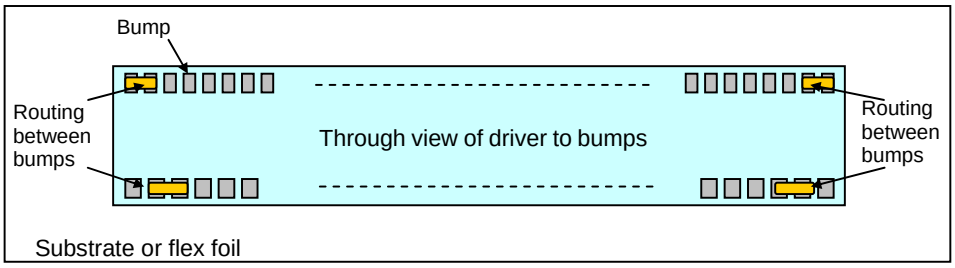
Fig. 5.14.2 Functionality Detection Flow chart

5.14.3 Chip Attachment Detection (optional)

Sleep Out-command (See section 6.1.13 “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if a chip or chips (e.g. driver, etc.) of the display module is/are attached to the circuit route of a flex foil or display glass ITO.

There is inverted (= increased by 1) a bit, which is defined in command 6.1.11 “Read Display Self- Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D5), if the chip or chips is/are attached to the circuit route of the flex or display glass. If this chip is or those chips are not attached to the circuit route of the flex or display glass, this bit (D5) is not inverted (= increased by 1).

The following figure is for reference purposes; how this chip attachment can be implemented e.g. there are connected together 2 bumps via route of ITO or the flex foil on 4 corners of the driver (chip).



The flow chart for this internal function is following:

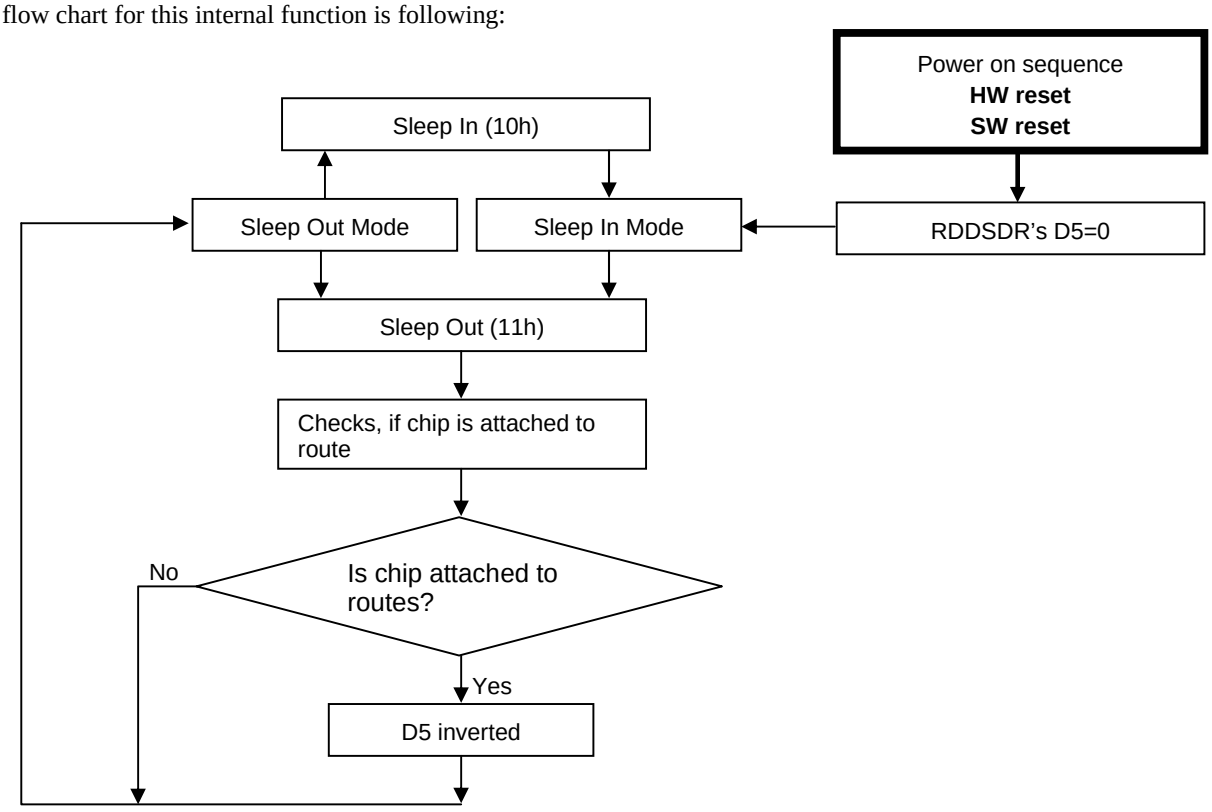


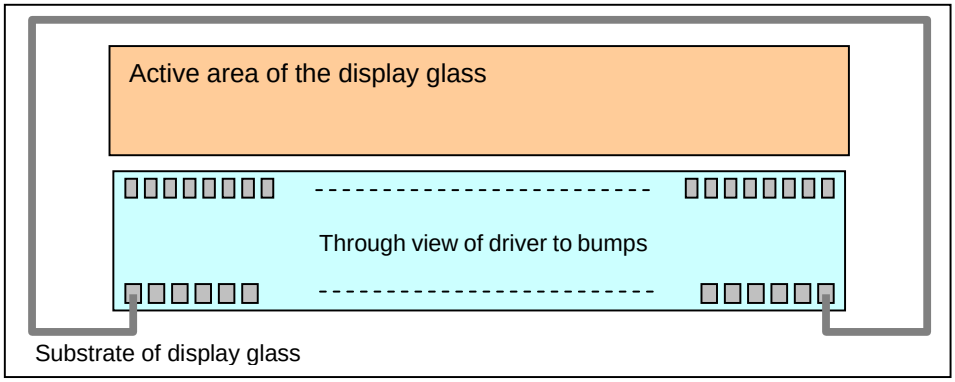
Fig. 5.14.3 Chip attachment Detection Flow chart

5.14.4 Display Glass Break Detection (optional)

Sleep Out-command (See section 6.1.12 “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display glass of the display module is broken or not.

There is inverted (= increased by 1) a bit, which is defined in command 6.1.11 “Read Display Self-Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D4), if the display glass is not broken. If this display glass is broken, this bit (D4) is not inverted (= increased by 1).

The following figure is a reference, how this glass break detection can be implemented e.g. there is connected together 2 bumps via route of ITO. This route of ITO is the nearest route of the edge of the display glass.



The flow chart for this internal function is following:

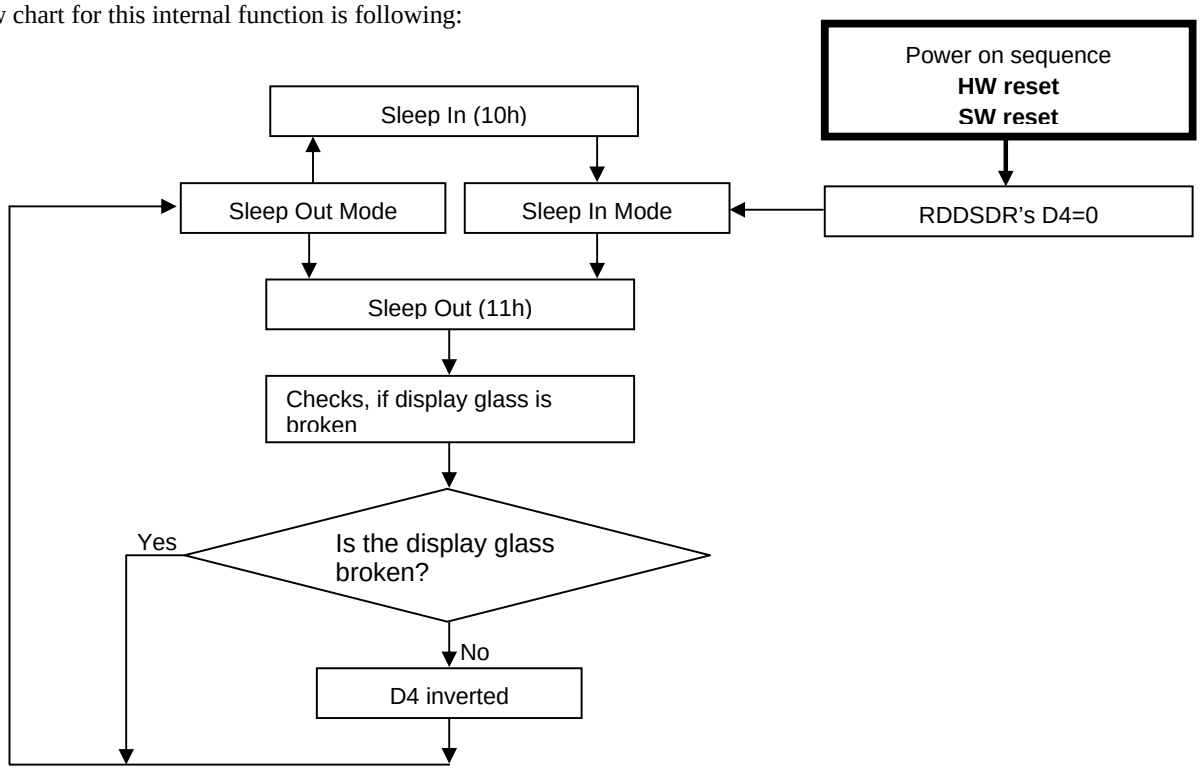


Fig. 5.14.4 Display Glass Break Detection Flow chart

6 ADAPTIVE BCAKLIGHT CONTROL AND LED DRIVER CONTROL

6.1 LABC (LIGHT ADAPTIVE BACKLIGHT CONTROL)

6.1.1 System Block Diagam with ALS (Ambient Light Sensor) and LDS285

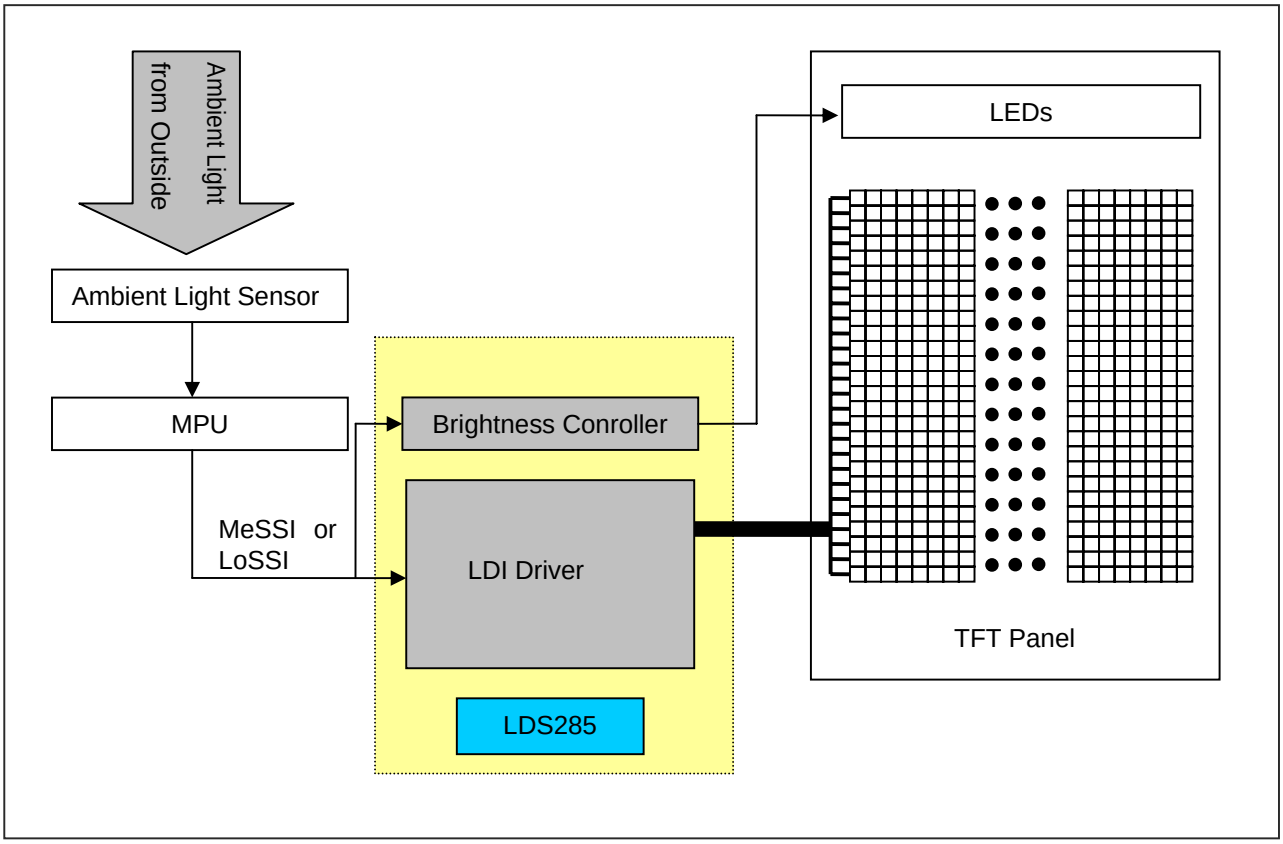


Fig. 6.1.1 System Block Diagram with ALS

The general block diagram of the ambient light and brightness control is illustrated in Fig 6.1.1. The information of the ambient light is sent to LDS285 and the Brightness Control in LDS285 deals with them if the user enables it.

The user can read ambient light information from LDS285 and control the brightness of LEDs in TFT Panel by writing the command to LDS285 manually. (See section 7.1.32 " Write Display Brightness (51h)").

6.1.2 LABC Function Flow

6.1.2.1 LABC contol from sleep out to sleep in

- Previous status before the sequence
  - Sleep in Mode
  - BCTRL = 0, BL = 0 in “Write CTRL Display(53h)”
- Command Sequence

Command : “Sleep out (11h)”
- Not working Brightness control
- Display backlight off

Command : “Write Display Brightness (51h)”

Parameter : DBV[7:0] : 216 (DBh: 85 % brightness)
- Not working Brightness control
- Display backlight off

Command : “Write CTRL Display (53h)”

Parameter : BCTRL = 1 : Brightness Control Block on
BL = 1 : Backlight Control on
- Display waits for V-sync
- Display starts brightness control from 0 % to 85 % after V-sync

Command : “Write Display Brightness (51h)”

Parameter : DBV[7:0] : 255 (DBh: 100 % brightness)
- Display waits for V-sync
- Display starts brightness control from 85 % to 100 % after V-sync

Command : “Write CTRL Display (53h)”

Parameter : BCTRL = 0 : Brightness Control Block off
BL = 0 : Backlight Control off
- Display waits for V-sync
- Display backlight off

Command : “Sleep in (10h)”

Following Fig 6.1.2 shows the brightness changes in the case of the above example..

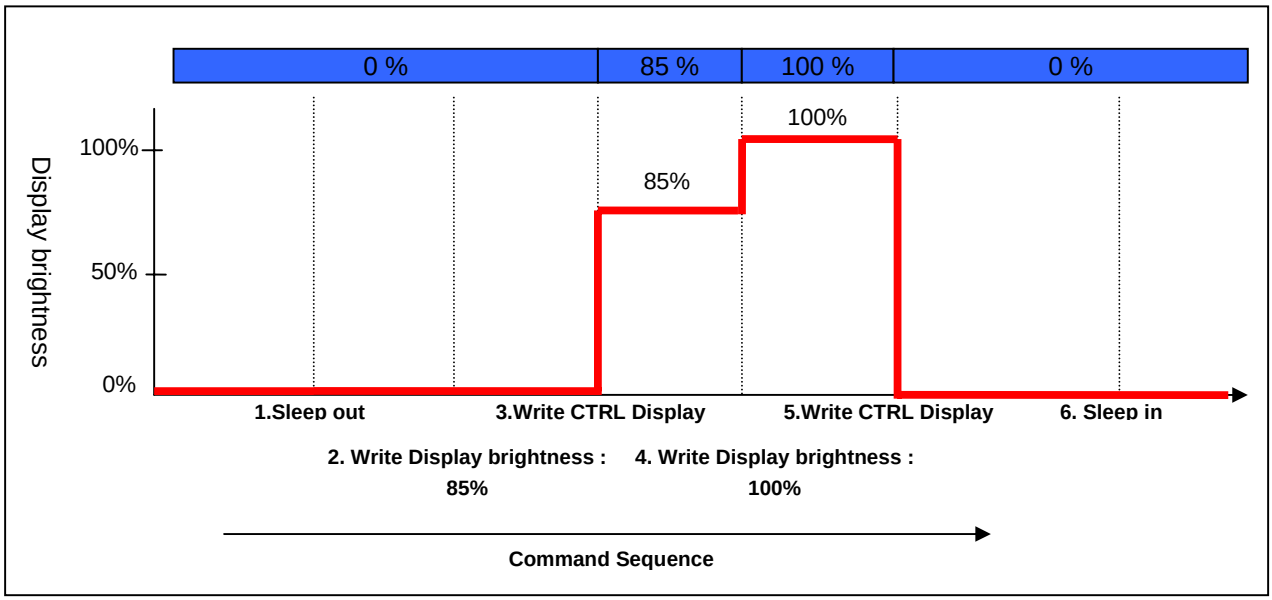


Fig. 6.1.2 LABC (Light Adaptive Brightness control) example

6.2 CABC (CONTENT ADAPTIVE BACKLIGHT CONTROL)

A Content Adaptive Brightness Control function can be used to reduce the power consumption of the luminance source. Content adaptation means that content grey level scale can be increased while simultaneously lowering brightness of the backlight to achieve the same perceived brightness. The adjusted grey level scale and thus the power consumption reduction depend on the content of the image.

The function and its different modes can be controlled. See “7.1.36 Write Content Adaptive Brightness Control (55h)” for more information.

Definition modes :

Off mode :

Content Adaptive Brightness Control functionality is totally off.

UI(User Interface) image mode :

Optimized for UI image. It is kept image quality as much as possible.

Target power consumption reduction ratio: 10% or less

SI(Still picture mode) :

Optimized for still picture. Some image quality degradation would be acceptable.

Target power consumption reduction ratio: more than 30 %

MI(Moving image mode) :

Optimized for moving image. It is focused on the biggest power reduction with image quality degradation. Target power consumption reduction ratio : more than 30 %

6.2.1 CABC Function Flow

Content Adaptive Brightness Control operates like below.

Display brightness is changed, according to the image contents. The following graph in Fig 6.2.1 mentions the case of displaying three different images.

- Image A : -20 % brightness reduction
- Image B : -30 % brightness reduction
- Image C : -10 % brightness reduction

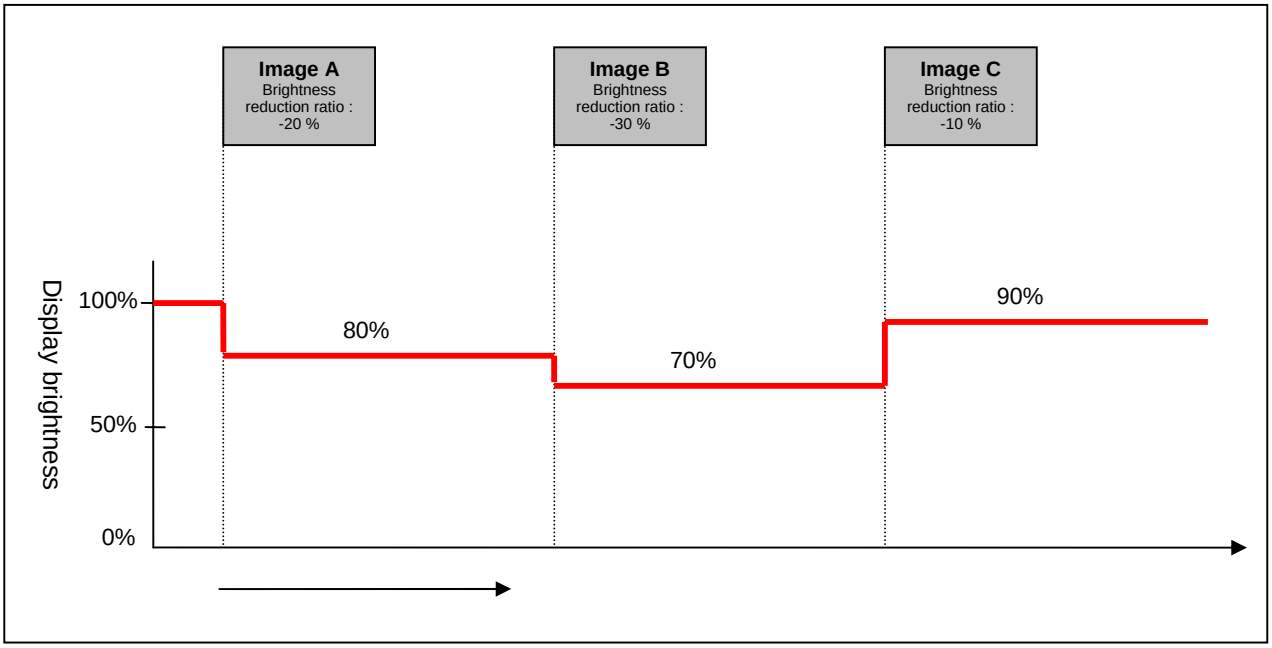


Fig. 6.2.1 CABC (Content Adaptive Brightness control) example)

6.3 CABC AND LABC

CABC and LABC can be "ON" simultaneously. Then the final Display Brightness is calculated with the following formula.

Display brightness = Brighness based on LABC * Brightness based on CABC

Table 6.3.1 Display Brightness ration when LABC and CABC are all "ON"

	LABC Brightness ratio	CABC Brightness ratio	Display Brightness ratio
Case1	85%	80%	68%
Case2	60%	70%	42%
Case3	85%	90%	76.5%

6.4 LED DRIVER CONTROL

LDS285 can change the brightness of LEDs in panel by controlling LED drivers if LABC or CABC is enabled (Refer to Section 6.1 LABC and 6.2 CABC).

LDS285 can support the two interfaces for two types of LED drivers, LED driver with pwm pulse contorl and LED driver with 1-wire digital interface (only for LDS8661), through the output LED_CNT.

6.4.1 LED Driver control with PWM pulse

LDS285 can calculate the backlight brightness level and send it to LED driver which is controlled by PWM pulse through the output LED_CNT.

Fig 6.4.1 is the basic timing diagram which is used in LDS285 to contol LED driver.

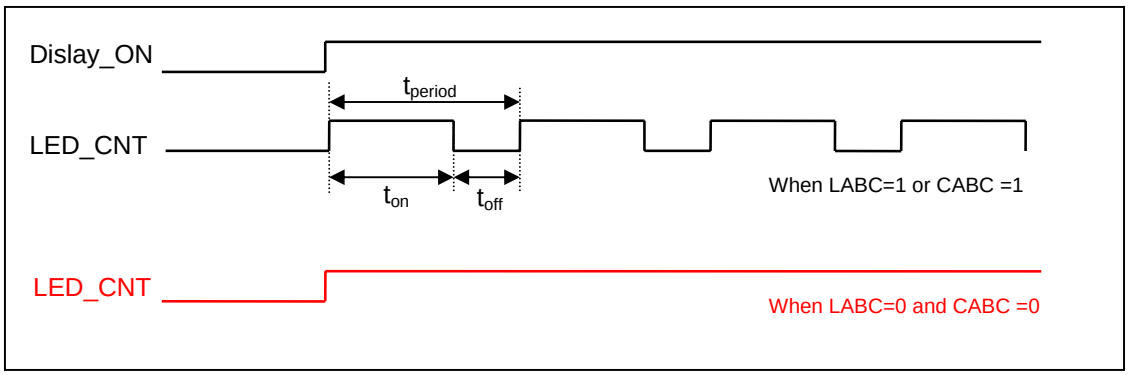


Fig. 6.4.1 PWM pulse timing on LED_CNT output

The period t_{period} of PWM pulse can be changed by the 3rd parameter PER[3:0] of the command "LEDCTRL(EFh)". (see the section 7.1.55 LEDCTRL)

The LED-on time t_{on} and the LED-off time t_{off} are decided by the backlight brightness level which is calculated with LABC or/and CABC in LDS285. If LABC is off and CABC is off, then LED_CNT is the same to Display-On signal.

Fig 6.4.2 shows the change of PWM pulse according to PER[3:0].

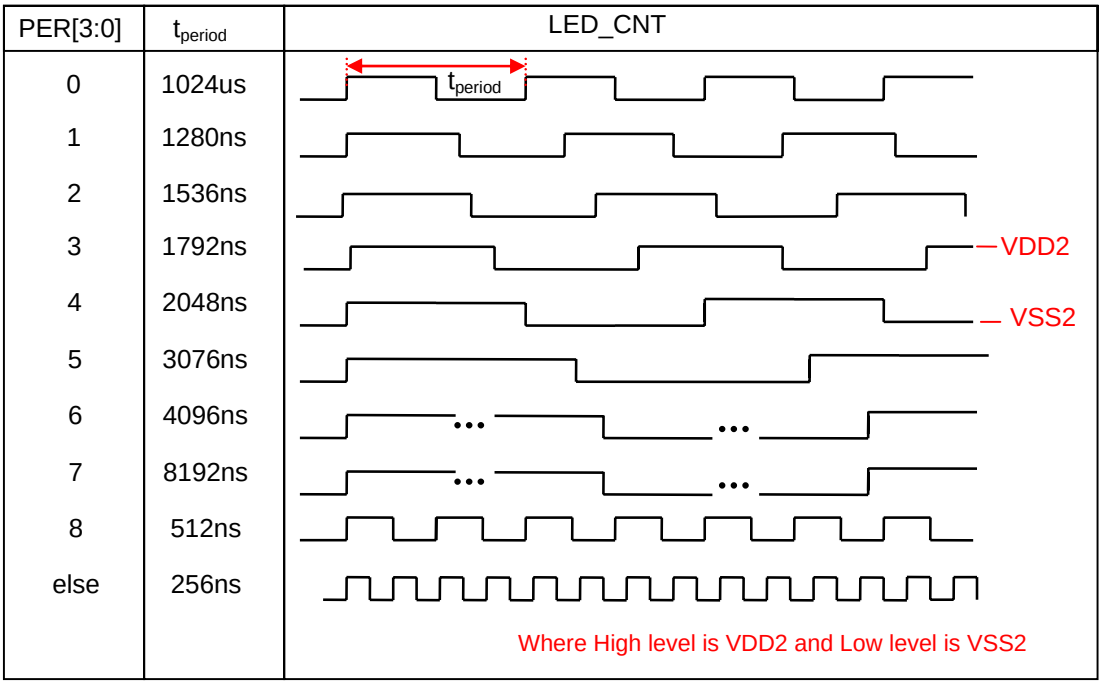


Fig. 6.4.2 PWM pulse timing according to PER[3:0]

Fig 6.4.3 shows the two examples of PWM pulse with LABC, CABC and PER[3:0]

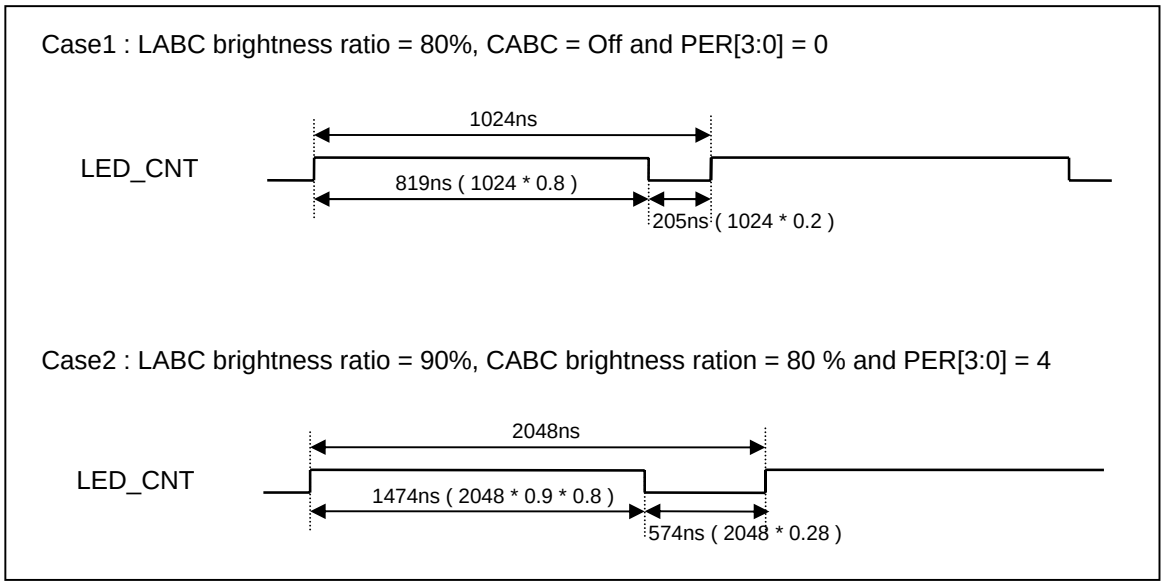


Fig. 6.4.3 PWM pulse examples with LABC, CABC and PER[3:0]

6.4.2 LED Driver control with 1-wire digital interface(only for LDS8861)

LDS285 can support only the LED driver LDS8861 with 1-wire digital interface.

Here we specify the interface between LDS285 and LDS8861 briefly. The LED_CNT output in LDS285 should be connected to EN/SET pin in LDS8816.

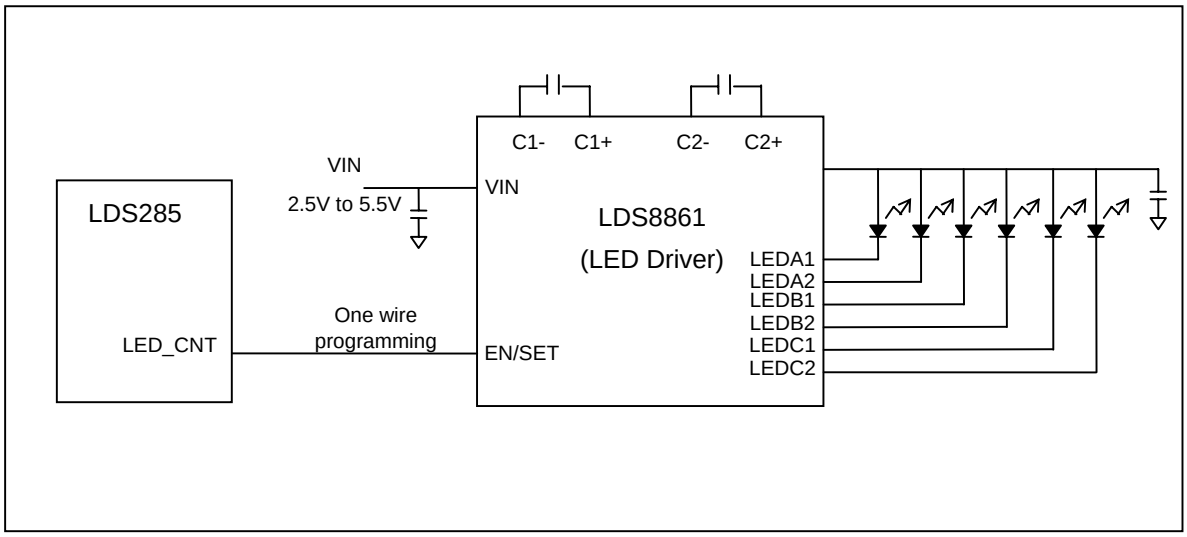


Fig. 6.4.4 Interconnection between LDS285 and LDS8861

LDS285 control LDS8861 through the one wire programming. The EN/SET logic input in LDS8861 operates as a chip enable and singla wire addressable interface for control and current setting of all LEDs.

LDS285 can write data to LDS8861 by programming the 2nd parameter of the command "LEDCTRL(EFh)". (see the section 7.1.55 LEDCTRL). The 2nd parameter of the command "LEDCTRL(EFh)" consists of ADDR[2:0] and DB[3:0].

The user can change the status of LDS8861 by changing the 2nd parameter of the command "LEDCTRL(EFh)".

Fig.6.4.5 shows the timing specification of EN/SET in LDS8861 and LDS285 drives the LED_CNT output meeting the timing specification of EN/SET in LDS8861.

If you need more detailed specification, please refer to "the Specification of LDS8861 (6-Channel Fractional Charge Pump LED Driver in 3x3 TQFN).

symbol	Name	Conditions	Min	Typ	Max	Units
T_{SETUP}	EN/SET setup from shutdown		10			us
T_{LO}	EN/SET program low time		0.2		100	us
T_{HI}	EN/SET program high time		0.2		100	us
T_{OFF}	EN/SET low time to shutdown		1.5			ms
$T_{DATADELAY}$	EN/SET Delay to DATA		500		1000	us
$T_{RESETDELAY}$	EN/SET Delay High to ADDRESS		2			ms

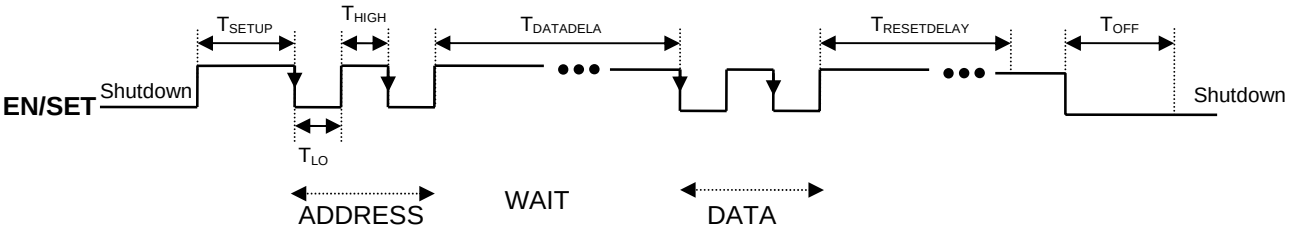


Fig. 6.4.5 EN/SET timing specification in LDS8861

7 INSTRUCTION DESCRIPTION

7.1 INSTRUCTION CODE

7.1.1 Instruction Code Table

Table 7.1.1 Instruction Code

"-": Don't care

Instruction	Refer	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
NOP	7.1.2	0	↑	1	-	0	0	0	0	0	0	0	0	**(00h)**	No Operation
SWRESET	7.1.3	0	↑	1	-	0	0	0	0	0	0	0	1	**(01h)**	Software reset
RDDID	7.1.4	0	↑	1	-	0	0	0	0	0	1	0	0	**(04h)**	Read Display ID
		1	1	↑	-	-	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-	ID1 read
		1	1	↑	-	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-	ID2 read
		1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-	ID3 read
RDDST	7.1.5	0	↑	1	-	0	0	0	0	1	0	0	1	**(09h)**	Read Display Status
		1	1	↑	-	-	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	-	ST31	ST30	ST29	ST28	ST27	ST26	ST25	ST24	-	-
		1	1	↑	-	ST23	ST22	ST21	ST20	ST19	ST18	ST17	ST16	-	-
		1	1	↑	-	ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8	-	-
		1	1	↑	-	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0	-	-
RDDPM	7.1.6	0	↑	1	-	0	0	0	0	1	0	1	0	**(0Ah)**	Read Display Power Mode
		1	1	↑	-	-	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	-	D7	D6	D5	D4	D3	D2	D1	D0	-	-
RDDMADCTR	7.1.7	0	↑	1	-	0	0	0	0	1	0	1	1	**(0Bh)**	Read Display MADCTR
		1	1	↑	-	-	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	-	D7	D6	D5	D4	D3	D2	D1	D0	-	-
RDDCOLMOD	7.1.8	0	↑	1	-	0	0	0	0	1	1	0	0	**(0Ch)**	Read Display Pixel Format
		1	1	↑	-	-	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	-	D7	D6	D5	D4	D3	D2	D1	D0	-	-
RDDIM	7.1.9	0	↑	1	-	0	0	0	0	1	1	0	1	**(0Dh)**	Read Display Image Mode
		1	1	↑	-	-	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	-	D7	D6	D5	D4	D3	D2	D1	D0	-	-
RDDSM	7.1.10	0	↑	1	-	0	0	0	0	1	1	1	0	**(0Eh)**	Read Display Signal Mode
		1	1	↑	-	-	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	-	D7	D6	D5	D4	D3	D2	D1	D0	-	-
RDDSDR	7.1.11	0	↑	1	-	0	0	0	0	1	1	1	1	**(0Fh)**	Read Display Self-diagnostic result
		1	1	↑	-	-	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	-	D7	D6	D5	D4	D3	D2	D1	D0	-	-
SLPIN	7.1.12	0	↑	1	-	0	0	0	1	0	0	0	0	**(10h)**	Sleep in & booster off
SLPOUT	7.1.13	0	↑	1	-	0	0	0	1	0	0	0	1	**(11h)**	Sleep out & booster on
PTLON	7.1.14	0	↑	1	-	0	0	0	1	0	0	1	0	**(12h)**	Partial mode on
NORON	7.1.15	0	↑	1	-	0	0	0	1	0	0	1	1	**(13h)**	Partial off (Normal)
INVOFF	7.1.16	0	↑	1	-	0	0	1	0	0	0	0	0	**(20h)**	Display inversion off (normal)
INVON	7.1.17	0	↑	1	-	0	0	1	0	0	0	0	1	**(21h)**	Display inversion on
GAMSET	7.1.18	0	↑	1	-	0	0	1	0	0	1	1	0	**(26h)**	Gamma curve select
		1	↑	**1**	-	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	-	-
DISPOFF	7.1.19	0	↑	1	-	0	0	1	0	1	0	0	0	**(28h)**	Display off
DISPON	7.1.20	0	↑	1	-	0	0	1	0	1	0	0	1	**(29h)**	Display on
CASET	7.1.21	0	↑	1	-	0	0	1	0	1	0	1	0	**(2Ah)**	Column address set
		1	↑	1	-	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	-	X address start: 0 ≤ XS ≤ EFh :MV=0
		1	↑	1	-	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	-	X address start: 0 ≤ XS ≤ 13Fh :MV=1
		1	↑	1	-	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	**-**	X address end: XS ≤ XE ≤ EFh :MV=0
		1	↑	1	-	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	**-**	X address end: XS ≤ XE ≤ 13Fh :MV=1

Table 7.1.2 Instruction Code (Continued)

"-":Don't care

Instruction	Refer	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
RASET	7.1.22	0	↑	1	-	0	0	1	0	1	0	1	1	**(2Bh)**	Row address set
		1	↑	1	-	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	-	Y address start: 0 ≤ YS ≤ 13Fh :MV=0
		1	↑	1	-	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	-	Y address start: 0 ≤ YS ≤ EFh :MV=1
		1	↑	1	-	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	**-**	Y address end: YS ≤ YE ≤ 13Fh :MV=0
		1	↑	1	-	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	**-**	Y address end: YS ≤ YE ≤ EFh :MV=1
RAMWR	7.1.23	0	↑	1	-	0	0	1	0	1	1	0	0	**(2Ch)**	Memory write
		1	↑	1	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	-	Write data
RAMRD	7.1.24	0	↑	1	-	0	0	1	0	1	1	1	0	**(2Eh)**	Memory read
		1	1	↑	-	-	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	-	Read data
PTLAR	7.1.25	0	↑	1	-	0	0	1	1	0	0	0	0	**(30h)**	Partial start/end address set
		1	↑	1	-	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8	-	Partial start address (0,1,2 , …,319)
		1	↑	1	-	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	-	
		1	↑	1	-	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8	**-**	Partial end address (0,1,2 , …, 319)
		1	↑	1	-	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	**-**	
TEOFF	7.1.26	0	↑	1	-	0	0	1	1	0	1	0	0	**(34h)**	Tearing effect line off
TEON	7.1.27	0	↑	1	-	0	0	1	1	0	1	0	1	**(35h)**	Tearing effect mode set & on
		1	↑	1	-	-	-	-	-	-	-	-	M	**-**	M="0": Mode1, M="1": Mode2
MADCTR	7.1.28	0	↑	1	-	0	0	1	1	0	1	1	0	**(36h)**	Memory data access control
		1	↑	1	-	MY	MX	MV	ML	RGB	-	-	-	-	-
IDMOFF	7.1.29	0	↑	1	-	0	0	1	1	1	0	0	0	**(38h)**	Idle mode off
IDMON	7.1.30	0	↑	1	-	0	0	1	1	1	0	0	1	**(39h)**	Idle mode on
COLMOD	7.1.31	0	↑	1	-	0	0	1	1	1	0	1	0	**(3Ah)**	Interface pixel format
		1	↑	1	-	-	RP2	RP1	RP0	-	P2	P1	P0	-	Interface format
WRDISBV	7.1.32	0	↑	1	-	0	1	0	1	0	0	0	1	**(51h)**	Write Display Brightness
		1	↑	1	-	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0		Write Data
RDDISBV	7.1.33	0	↑	1	-	0	1	0	1	0	0	1	0	**(52h)**	Read Display Brightness value
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0		Read parameter
WRCTRLD	7.1.34	0	↑	1	-	0	1	0	1	0	0	1	1	**(53h)**	Write Control Display
		1	↑	1	-	-	-	BCTRL	-	-	BL	-	-	-	Write Data
RDCTRLD	7.1.35	0	↑	1	-	0	1	0	1	0	1	0	0	**(54h)**	Read Control Display
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	-	-	BCTRL	-	-	BL	-	-		Read parameter
WRCABC	7.1.36	0	↑	1	-	0	1	0	1	0	1	0	1	**(55h)**	Wrtie Content Adaptive Brightness
		1	↑	1	-	-	-					C1	C0	-	Write Data
RDCABC	7.1.37	0	↑	1	-	0	1	0	1	0	1	1	0	**(56h)**	Read Content Adaptive Brightness
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	-	-					C1	C0		Read parameter
RDID1	7.1.38	0	↑	1	-	1	1	0	1	1	0	1	0	**(DAh)**	Read ID1
		1	1	↑	-	-	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-	Read parameter
RDID2	7.1.39	0	↑	1	-	1	1	0	1	1	0	1	1	**(DBh)**	Read ID2
		1	1	↑	-	-	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	-	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-	Read parameter
RDID3	7.1.40	0	↑	1	-	1	1	0	1	1	1	0	0	**(DCh)**	Read ID3
		1	1	↑	-	-	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-	Read parameter

Table 7.1.3 Instruction Code (Extended code set)

"-": Don't Care

Instruction	Refer	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
IFMODE	7.1.41	0	↑	1	-	1	0	1	1	0	0	0	0	**(B0h)**	Set display interface mode
		1	↑	1	-	-	-	-	-	**-**	**-**	IF1	IF0	-	Data transfer mode set
		1	↑	1	-	-	-	DW	-	DP	EP	HSP	VSP	-	RGB I/F data width & Clock polarity set
DISCLK	7.1.42	0	↑	1	-	1	0	1	1	0	0	0	1	**(B1h)**	Display clock set
		1	↑	1	-	HA7	HA 6	HA 5	HA 4	HA 3	HA 2	HA 1	HA 0	-	Number of clocks during 1H (full-color)
		1	↑	1	-	-	-	BPA5	BPA4	BPA3	BPA2	BPA1	BPA0	-	Number of vertical back porches (full-color)
		1	↑	1	-	-	-	FPA5	FPA4	FPA3	FPA2	FPA1	FPA0	-	Number of vertical front porches (full-color)
		1	↑	1	-	HB7	HB 6	HB 5	HB 4	HB 3	HB 2	HB 1	HB 0	-	Number of clocks during 1H (8-color)
		1	↑	1	-	-	-	BPB5	BPB4	BPB3	BPB2	BPB1	BPB0	-	Number of vertical back porches (8-color)
		1	↑	1	-	-	-	FPB5	FPB4	FPB3	FPB2	FPB1	FPB0	-	Number of vertical front porches (8-color)
INVCTR	7.1.43	0	↑	1	-	1	0	1	1	0	0	1	0	**(B2h)**	Display inversion control
		1	↑	1	-	0	0	0	0	-	NLA2	NLA1	NLA0	-	Line inversion (full color)
		1	↑	1	-	0	0	0	0	-	NLB2	NLB1	NLB0	-	Line inversion (8-color)
REGCTR	7.1.44	0	↑	1	-	1	1	0	0	0	0	0	0	**(C0h)**	Regulator control
		1	↑	1	-	-	VR2	VR1	VR0	-	VS2	VS1	VS0	-	VR/VS regulator output voltage control
VCOMCTR	7.1.45	0	↑	1	-	1	1	0	0	0	0	0	1	**(C1h)**	VCOML/VCOMH voltage control
		1	↑	1	-	-	-	VCLC5	VCLC4	VCLC3	VCLC2	VCLC1	VCLC0	**-**	-2.5V ~ +0.5V (50mV step)
		1	↑	1	-	-	-	VCHC5	VCHC4	VCHC3	VCHC2	VCHC1	VCHC0	**-**	+2.5V ~ +5.5V (50mV step)
GAMCTR1	7.1.46	0	↑	1	-	1	1	0	0	1	0	0	0	**(C8h)**	Set gamma correction characteristics
		1	↑	1	-	-	-	GS102	GS101	GS100	GS112	GS111	GS110	-	Gamma adjustment .
		1	↑	1	-	-	-	GS122	GS121	GS120	GS132	GS131	GS130	-	Gamma adjustment .
		1	↑	1	-	-	-	GS142	GS141	GS140	GS152	GS151	GS150	-	Gamma adjustment .
		1	↑	1	-	-	-	GS162	GS161	GS160	GS172	GS171	GS170	-	Gamma adjustment .
GAMCTR2	7.1.47	0	↑	1	-	1	1	0	0	1	0	0	1	**(C9h)**	Set gamma correction characteristics
		1	↑	1	-	-	-	GS202	GS201	GS200	GS212	GS211	GS210	-	Gamma adjustment .
		1	↑	1	-	-	-	GS222	GS221	GS220	GS232	GS231	GS230	-	Gamma adjustment .
		1	↑	1	-	-	-	GS242	GS241	GS240	GS252	GS251	GS250	-	Gamma adjustment .
		1	↑	1	-	-	-	GS262	GS261	GS260	GS272	GS271	GS270	-	Gamma adjustment .
GAMCTR3	7.1.48	0	↑	1	-	1	1	0	0	1	0	1	0	**(CAh)**	Set gamma correction characteristics
		1	↑	1	-	-	-	GS302	GS301	GS300	GS312	GS311	GS310	-	Gamma adjustment .
		1	↑	1	-	-	-	GS322	GS321	GS320	GS332	GS331	GS330	-	Gamma adjustment .
		1	↑	1	-	-	-	GS342	GS341	GS340	GS352	GS351	GS350	-	Gamma adjustment .
		1	↑	1	-	-	-	GS362	GS361	GS360	GS372	GS371	GS370	-	Gamma adjustment .
GAMCTR4	7.1.49	0	↑	1	-	1	1	0	0	1	0	1	1	**(CBh)**	Set gamma correction characteristics
		1	↑	1	-	-	-	GS402	GS401	GS400	GS412	GS411	GS410	-	Gamma adjustment .
		1	↑	1	-	-	-	GS422	GS421	GS420	GS432	GS431	GS430	-	Gamma adjustment .
		1	↑	1	-	-	-	GS442	GS441	GS440	GS452	GS451	GS450	-	Gamma adjustment .
		1	↑	1	-	-	-	GS462	GS461	GS460	GS472	GS471	GS470	-	Gamma adjustment .

Table 7.1.4 Instruction Code (Extended code set, continued)

"-": Don't Care

Instruction	Refer	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
EPPGMDB	7.1.50	0	↑	1	-	1	1	0	1	0	0	0	0	**(D0h)**	Write ID2,VCOM Offset for EEPROM program
		1	↑	1	-	-	-	-	-	-	VCOF82	VCOF81	VCOF80	-	VCOM middle voltage trimming in 8color
		1	↑	1		-	-	VCOF5	VCOF4	VCOF3	VCOF2	VCOF1	VCOF0		VCOM middle voltage trimming
		1	↑	1		ID26	ID25	ID24	ID23	ID22	ID21	ID20	db_sel		Just ID2 [6:0] are stored in EEPROM
EPERASE	7.1.51	0	↑	1	-	1	1	0	1	0	0	0	1	**(D1h)**	EEPROM erase
EPPROG	7.1.52	0	↑	1	-	1	1	0	1	0	0	1	0	**(D2h)**	EEPROM program
EPRDVRF	7.1.53	0	↑	1	-	1	1	0	1	0	0	1	1	**(D3h)**	EEPROM read, verify register set
						0	0	0	0	READ	PGMVF	ERVF	0		macro read , program verify,Erase verify
RDVCOF	7.1.54	0	↑	1	-	1	1	0	1	1	0	0	1	**(D9h)**	VCOM offset bits read
		1	1	↑	-	-	-	-	-	-	-	-	-	**-**	Dummy Read
		1	1	↑	-	-	-	RVCOF5	RVCOF4	RVCOF3	RVCOF2	RVCOF1	RVCOF0	-	Read Parameter
		1	1	↑							RVCOF82	RVCOF81	RVCOF80		Read Parameter
LEDCTRL	7.1.55	0	↑	1	-	1	1	1	0	1	1	1	1	**(EFh)**	Write LED control value
		1	↑	1									TYPE	**-**	LED driver type
		1	↑	1		0	ADR2	ADR1	ADR0	DB3	DB2	DB1	DB0	**-**	Control value for LDS8861
		1	↑	1		0	PER3	PER2	PER1	PER0	STEP2	STEP1	STEP0	**-**	Contorl value for PWM output

NOTE:

1) After the H/W reset by RESB pin or S/W reset by SWRESET command, each internal register becomes default state (Refer "RESET TABLE" section)

2) Before command D1(EPER) , supply 22V to the ME_CMP for EEPROM Erase .

3) Before command D2(EPPGM), supply 8.5V to the ME_CMP for EEPROM Program .

4) To use extended code set,

the TGS pad should be connected to VSS. Extended code set is just used for module test. If TGS pad is not connected to VSS, all the extended code set will be ignored and regarded as NOP (00h) command.

5) Undefined commands are treated as NOP (00 h) command.

6) Commands 10h, 12h, 13h, 20h, 21h, 26h, 28h, 29h, 30h, 33h, 36h (ML parameter only), 37h, 38h and 39h are updated during V-sync when Module is in Sleep Out Mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately. Read status (09h), Read Display Power Mode ($0A_H$), Read Display MADCTL ($0B_H$), Read Display Pixel Format ($0C_H$), Read Display Image Mode ($0D_H$), Read Display Signal Mode ($0E_H$) and Read Display Self Diagnostic Result ($0F_H$) of these commands of these commands is updated immediately both in Sleep In mode and Sleep Out mode.

7.1.2 NOP (00h)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
NOP	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)
Parameter	No Parameter												

NOTE: "-" Don't care

Description	This command is empty command. It does not have effect on the display module. However it can be used to terminate DDRAM data write or read as described in RAMWR (Memory Write), RAMRD (Memory Read) and parameter write commands.
Restriction	-
Register Availability	Status: Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes
Default	Status: Default Value Power On Sequence: N/A S/W Reset: N/A H/W Reset: N/A
Flow Chart	-

7.1.3 SWRESET: Software Reset (01h)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SWRESET	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)
Parameter	No Parameter												

NOTE: "-" Don't care

Description

When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values and all source & gate outputs are set to VSS (display off). (See default tables in each command description)

Note: The DDRAM contents are not affected by this command.

Restriction

It will be necessary to wait 5msec before sending new command following software reset.

The display module loads all display supplier's factory default values to the registers during 5msec.

If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep Out command.

Software Reset command cannot be sent during Sleep Out sequence.

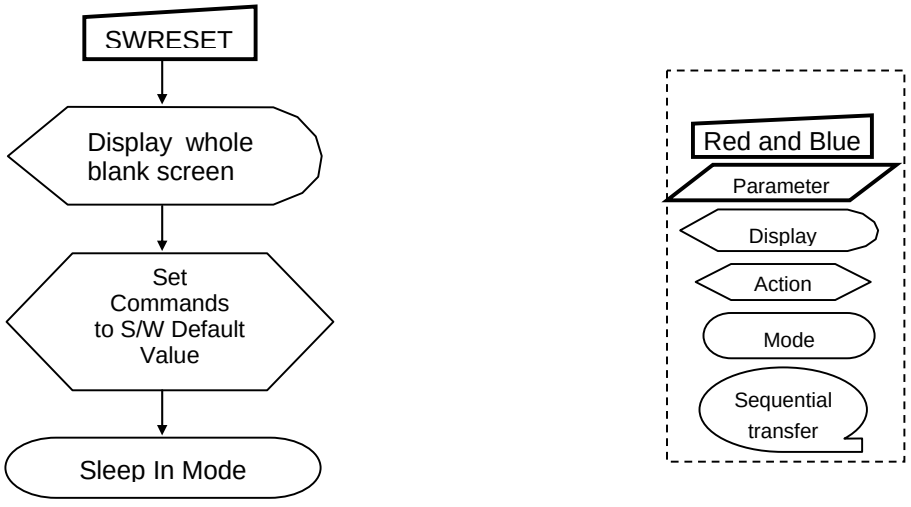
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart



7.1.4 RDDID: Read Display ID (04h)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDID	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)
Dummy Read	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-
3rd parameter	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-
4th parameter	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-

NOTE: "-" Don't care

Description

This read byte returns 24-bit display identification information.
The 1st parameter is dummy data
The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID.
The 3rd parameter (ID27 to ID20): LCD module/driver version ID
The 4th parameter (ID37 to UD30): LCD module/driver ID.
NOTE: Commands RDID1/2/3(DAh, DBh, DCh) read data correspond to the parameters 2,3,4 of the command 04h, respectively.

Restriction

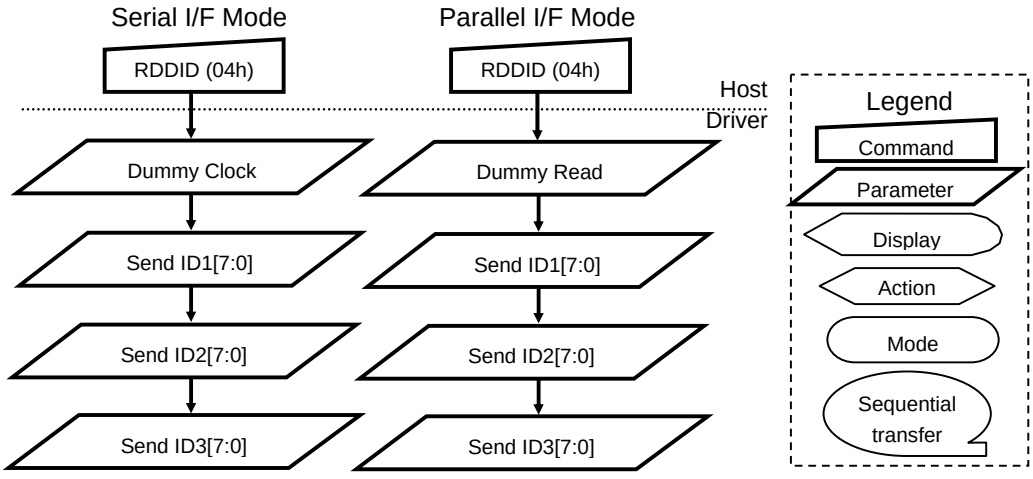
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	ID1	ID2	ID3
Power On Sequence	Not Fixed	Not Fixed	Not Fixed
S/W Reset	Not Fixed	Not Fixed	Not Fixed
H/W Reset	Not Fixed	Not Fixed	Not Fixed

Flow Chart



7.1.5 RDDST: Read Display Status (09h)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDST	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)
Dummy Read	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	ST31	ST30	ST29	ST28	ST27	ST26	ST25	ST24	-
3rd parameter	1	1	↑	-	ST23	ST22	ST21	ST20	ST19	ST18	ST17	ST16	-
4th parameter	1	1	↑	-	ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8	-
5th parameter	1	1	↑	-	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0	-

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
ST31	Booster Voltage Status	"1"=Booster on, "0"=off
ST30	Row Address Order (MY)	"1"=Decrement, "0"=Increment
ST29	Column Address Order (MX)	"1"=Decrement, "0"=Increment
ST28	Row/Column Exchange (MV)	"1"= Row/column exchange (MV=1) "0"= Normal (MV=0)
ST27	Scan Address Order (ML)	"1"=Decrement, "0"=Increment
ST26	RGB/BGR Order (RGB)	"1"=BGR, "0"=RGB
ST25	Not Used	"0"
ST24	Not Used	"0"
ST23	Not Used	"0"
ST22 ST21 ST20	Interface Colour Pixel Format Definition	"110" = 18-bit / pixel (666 mode) "111" = 24-bit / pixel (888 mode)
ST19	Idle Mode On/Off	"1" = On, "0" = Off
ST18	Partial Mode On/Off	"1" = On, "0" = Off
ST17	Sleep In/Out	"1" = Out, "0" = In
ST16	Display Normal Mode On/Off	"1" = Normal Display, "0" = Partial Display
ST15	Vertical Scrolling Status	"1" = Scroll on, "0" = Scroll off
ST14	Not Used	"0"
ST13	Inversion Status	"1" = On, "0" = Off
ST12	All Pixels On (Not Used)	"0"
ST11	All Pixels Off (Not Used)	"0"
ST10	Display On/Off	"1" = On, "0" = Off
ST9	Tearing effect line on/off	"1" = On, "0" = Off
ST8 ST7 ST6	Gamma Curve Selection	"000" = GC0, "001" = GC1, "010" = GC2, "011" = GC3 "100"~"111":Not used
ST5	Tearing effect line mode	"0" = mode1, "1" = mode2
ST4	Not Used	"0"
ST3	Not Used	"0"
ST2	Not Used	"0"
ST1	Not Used	"0"
ST0	Not Used	"0"

Restriction

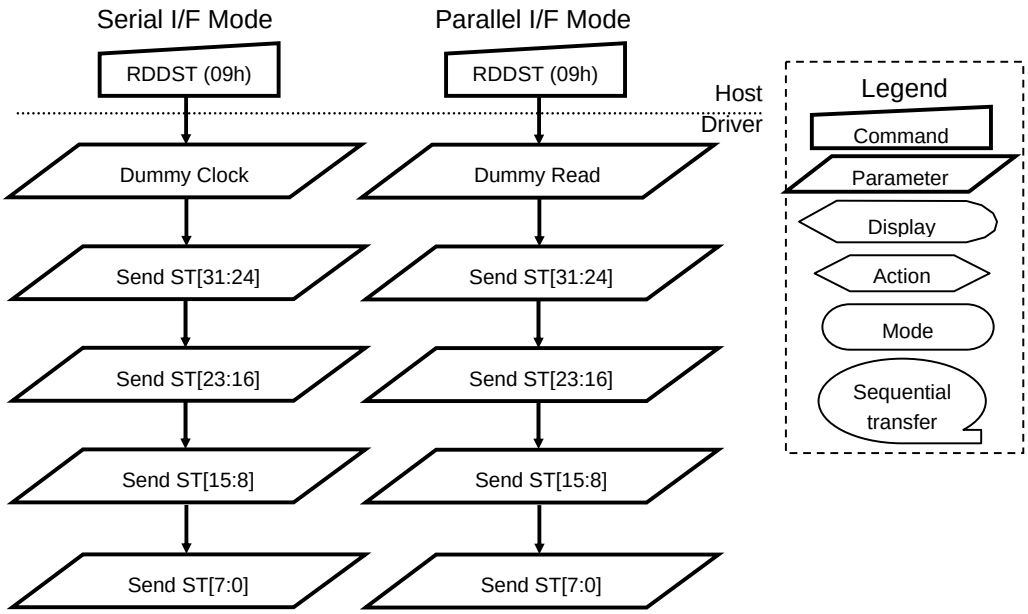
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (ST31 to ST0):
Power On Sequence	0000 0000_0111 0001_0000 0000_0000 0000
S/W Reset	0xxx xx00_0xxx 0001_0000 0000_0000 0000
H/W Reset	0000 0000_0111 0001_0000 0000_0000 0000

Flow Chart



7.1.6 RDDPM: Read Display Power Mode (0Ah)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDPM	0	↑	1	-	0	0	0	0	1	0	1	0	(0Ah)
Dummy Read	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	D7	D6	D5	D4	D3	D2	D1	D0	-

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Booster Voltage Status	"1"=Booster on, "0"=Booster off
D6	Idle Mode On/Off	"1" = Idle Mode On, "0" = Idle Mode Off
D5	Partial Mode On/Off	"1" = Partial Mode On, "0" = Partial Mode Off
D4	Sleep In/Out	"1" = Sleep Out, "0" = Sleep In
D3	Display Normal Mode On/Off	"1" = Normal Display, "0" = Partial Display
D2	Display On/Off	"1" = Display On, "0" = Display Off
D1	Not Used	"0"
D0	Not Used	"0"

Restriction

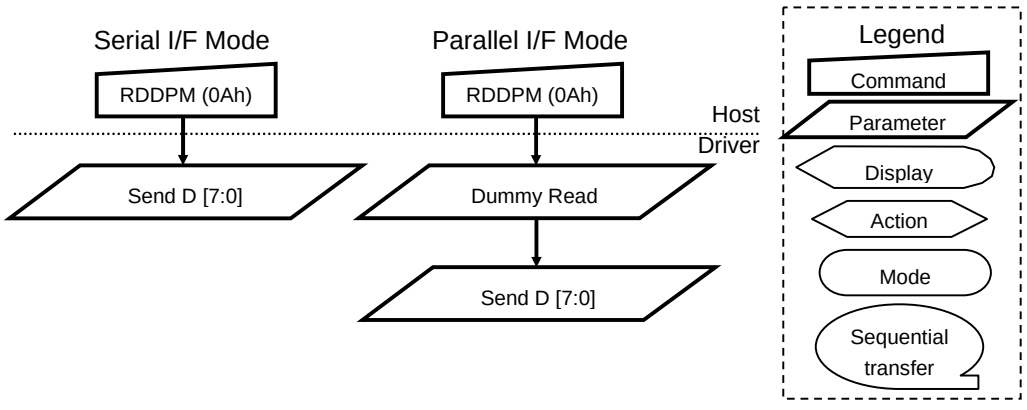
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_1000 (08h)
S/W Reset	0000_1000 (08h)
H/W Reset	0000_1000 (08h)

Flow Chart



7.1.7 RDDMADCTR: Read Display MADCTR (0Bh)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDMADCTR	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)
Dummy Read	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	D7	D6	D5	D4	D3	D2	D1	D0	-

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Row Address Order	"1"=Decrement, "0"=Increment
D6	Column Address Order	"1"=Decrement, "0"=Increment
D5	Row/Column Order (MV)	"1"= Row/column exchange (MV=1) "0"= Normal (MV=0)
D4	Scan Address Order	"1"=Decrement, "0"=Increment
D3	RGB/BGR Order	"1"=BGR, "0"=RGB
D2	Not Used	"0"
D1	Not Used	"0"
D0	Not Used	"0"

Restriction

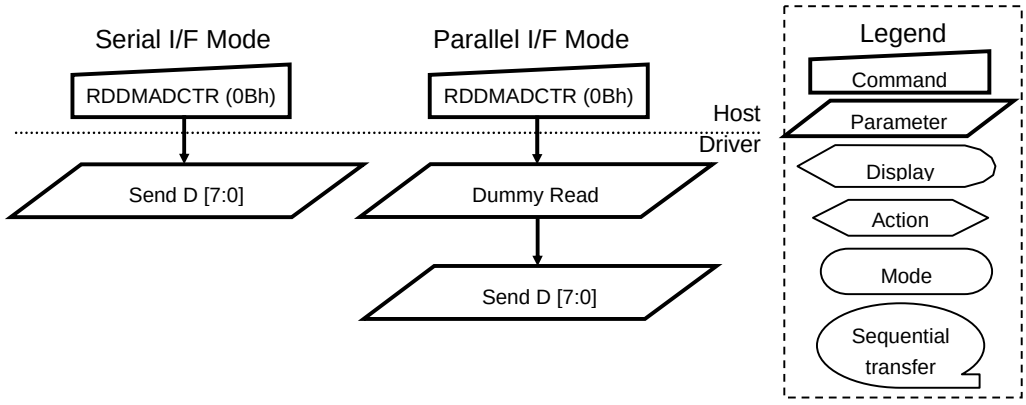
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	No change
H/W Reset	0000_0000 (00h)

Flow Chart



7.1.8 RDDCOLMOD: Read Display Pixel Format (0Ch)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDCOLMOD	0	↑	1	-	0	0	0	0	1	1	0	0	(0Ch)
Dummy Read	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	D7	D6	D5	D4	D3	D2	D1	D0	-

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	RGB Interface Color Format	"0" (Not Used)
D6		"0" (Not Used)
D5		"0" (Not Used)
D4		"0" (Not Used)
D3	Control Interface Color Format	"0"
D2		"111"=24 bit/pixel "011"=12 bit/pixel "101"=16 bit/pixel "110"=18 bit/pixel
D1		
D0		

Restriction

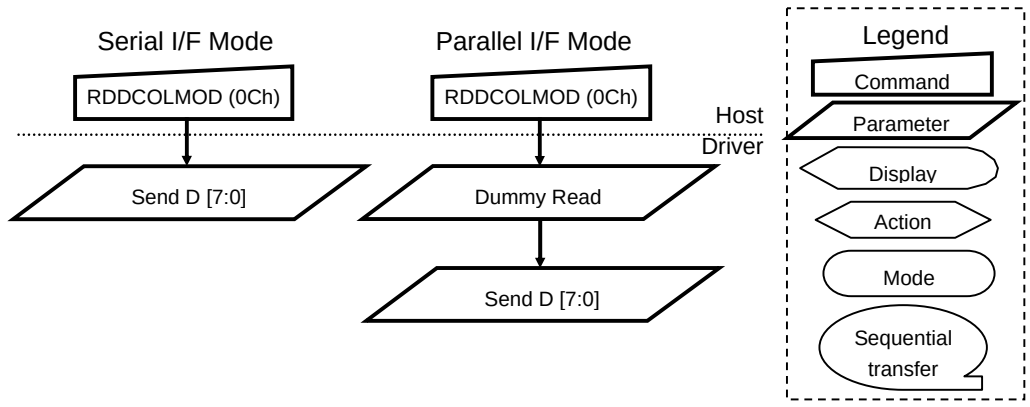
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000_0111 (24 bit/pixel)
S/W Reset	No Change
H/W Reset	0000_0111 (24 bit/pixel)

Flow Chart



7.1.9 RDDIM: Read Display Image Mode (0Dh)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDIM	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)
Dummy Read	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	D7	D6	D5	D4	D3	D2	D1	D0	-

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Vertical Scrolling On/Off	"0" (Not used)
D6	Horizontal Scrolling On/Off	"0" (Not used)
D5	Inversion On/Off	"1" = Inversion is On, "0" = Inversion is Off
D4	All Pixels On	"0" (Not used)
D3	All Pixels Off	"0" (Not used)
D2	Gamma Curve Selection	"000" = GC0, "001" = GC1 "010" = GC2, "011" = GC3 "100" to "111" = Not defined
D1		
D0		

Restriction

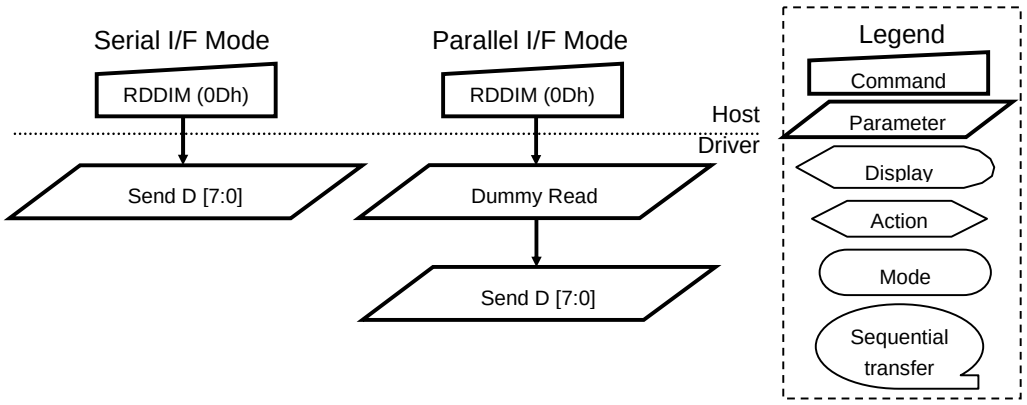
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	0000_0000 (00h)
H/W Reset	0000_0000 (00h)

Flow Chart



7.1.10 RDDSM: Read Display Signal Mode (0Eh)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDSM	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)
Dummy Read	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	D7	D6	D5	D4	D3	D2	D1	D0	-

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Tearing Effect Line On/Off	"1" = On, "0" = Off
D6	Tearing effect line mode	"0" = mode1, "1" = mode2
D5	Horizontal Sync. (RGB I/F) On/Off	"0"
D4	Vertical Sync. (RGB I/F) On/Off	"0"
D3	Pixel Clock (DCK, RGB I/F) On/Off	"0"
D2	Data Enable (ENABLE, RGB I/F) On/Off	"0"
D1	Not Used	"0"
D0	Not Used	"0"

Restriction

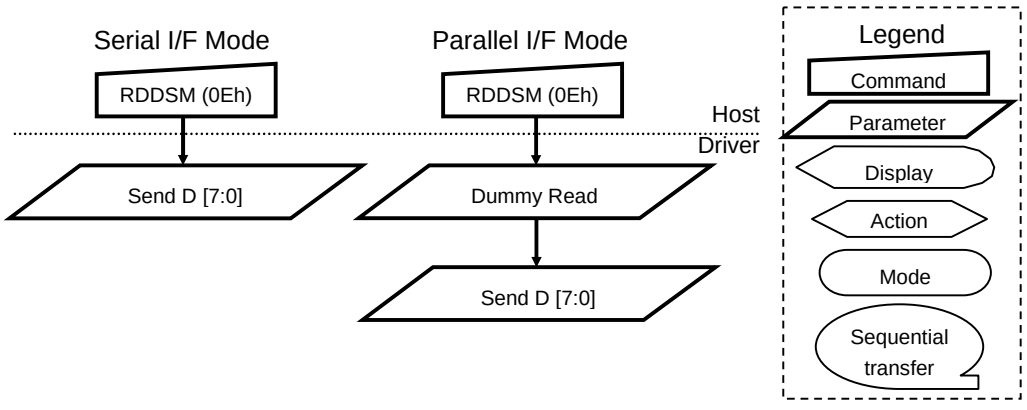
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	0000_0000 (00h)
H/W Reset	0000_0000 (00h)

Flow Chart



7.1.11 RDDSDR: Read Display Self-Diagnostic Result (0Fh)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDSDR	0	↑	1	-	0	0	0	0	1	1	1	1	(0Fh)
Dummy Read	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	D7	D6	D5	D4	D3	D2	D1	D0	-

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Register Loading Detection	refer section 5.14
D6	Functionality Detection	
D5	Chip Attachment Detection	
D4	Display Glass Break Detection	
D3	Not Used	"0"
D2	Not Used	"0"
D1	Not Used	"0"
D0	Not Used	"0"

Restriction

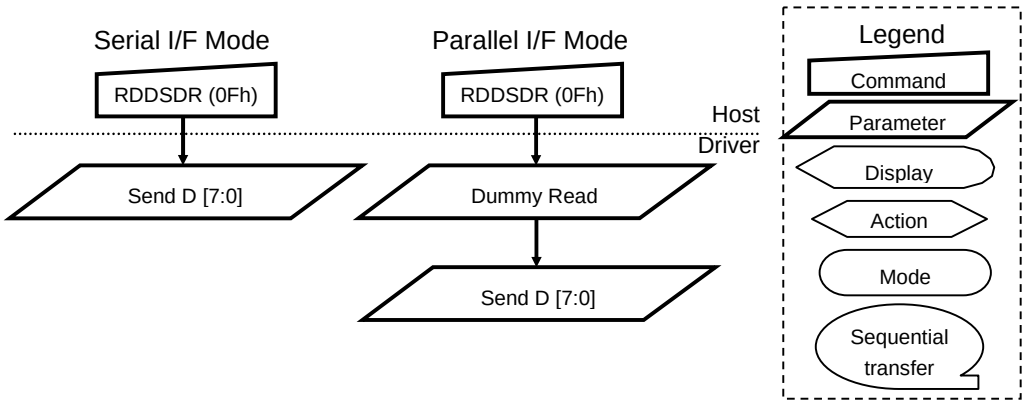
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000_0000 (00h)
S/W Reset	0000_0000 (00h)
H/W Reset	0000_0000 (00h)

Flow Chart



7.1.12 SLPIN: Sleep In (10h)

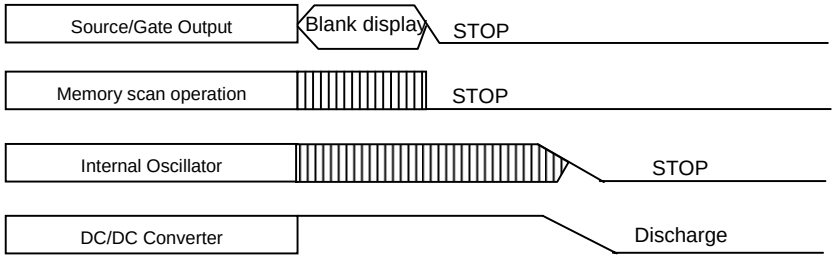
Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SLPIN	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)
Parameter	No Parameter												

NOTE: "-" Don't care

Description

This command causes the LCD module to enter the minimum power consumption mode.

In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped.



MPU interface and memory are still working and the memory keeps its contents

Restriction

This command has no effect when module is already in sleep in mode. Sleep In Mode can only be exit by the Sleep Out Command (11h).

It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.

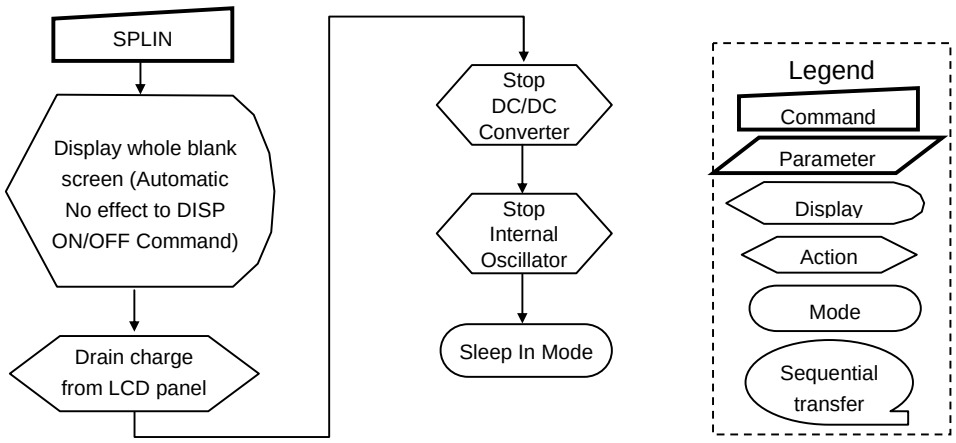
It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep in mode
S/W Reset	Sleep in mode
H/W Reset	Sleep in mode

Flow Chart	It takes about 120 msec to get into Sleep In mode (booster off state) after SLPIN command issued. The results of booster off can be check by RDDST (09h) command Bit31. 

7.1.13 SLPOUT: Sleep Out (11h)

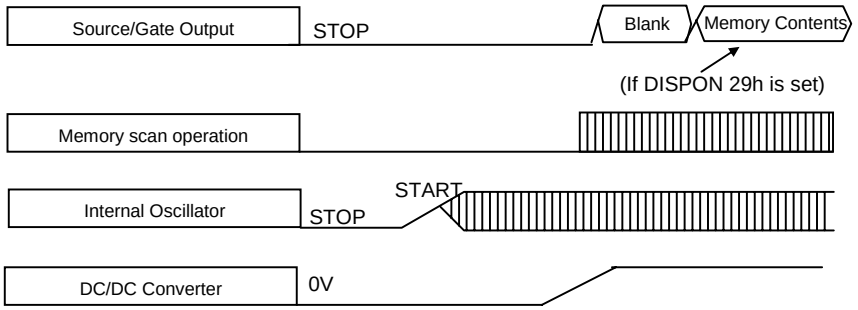
Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SLPOUT	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)
Parameter	No Parameter												

NOTE: "-" Don't care

Description

This command turns off sleep mode.

In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started.



Restriction

This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be exit by the Sleep In Command (10h).

It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to be stabilized.

LDS285 loads all default values of extended and test command to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if those default and register values are same when this load is done and then the LDS285 is already Sleep Out –mode.

LDS285 is doing self-diagnostic functions during this 5msec. See also section 5.14.

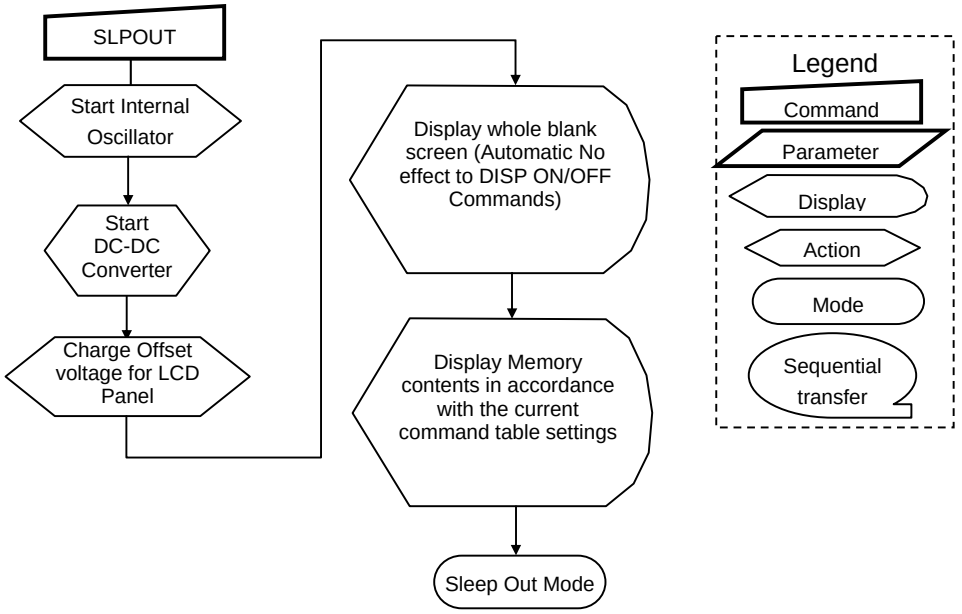
It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep in mode
S/W Reset	Sleep in mode
H/W Reset	Sleep in mode

Flow Chart	It takes 120msec to become Sleep Out mode (booster on mode) after SLPOUT command issued. The results of booster on can be checked by RDDST (09h) command Bit31. 

7.1.14 PTLON: Partial Display Mode On (12h)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PTLON	0	↑	1	-	0	0	0	1	0	0	1	0	(12h)
Parameter	No Parameter												

NOTE: "-" Don't care

Description	This command turns on Partial mode. The partial mode window is described by the Partial Area command (30_H) To leave Partial mode, the Normal Display Mode On command (13H) should be written. There is no abnormal visual effect during mode change between Normal mode On <-> Partial mode On.
Restriction	This command has no effect when Partial mode is active.
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes
Default	Status / Default Value Power On Sequence: Normal Mode On S/W Reset: Normal Mode On H/W Reset: Normal Mode On
Flow Chart	See Partial Area (30h)

7.1.15 NORON: Normal Display Mode On (13h)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
NORON	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)
Parameter	No Parameter												

NOTE: "-" Don't care

Description	This command returns the display to normal mode. Normal display mode on means Partial mode off. There is no abnormal visual effect during mode change from Normal mode On <-> Partial mode On.
Restriction	This command has no effect when Normal Display mode is active.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Normal Mode On
S/W Reset	Normal Mode On
H/W Reset	Normal Mode On

Flow Chart	See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command

7.1.16 INVOFF: Display Inversion Off (20h)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
INVOFF	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)
Parameter	No Parameter												

NOTE: "-" Don't care

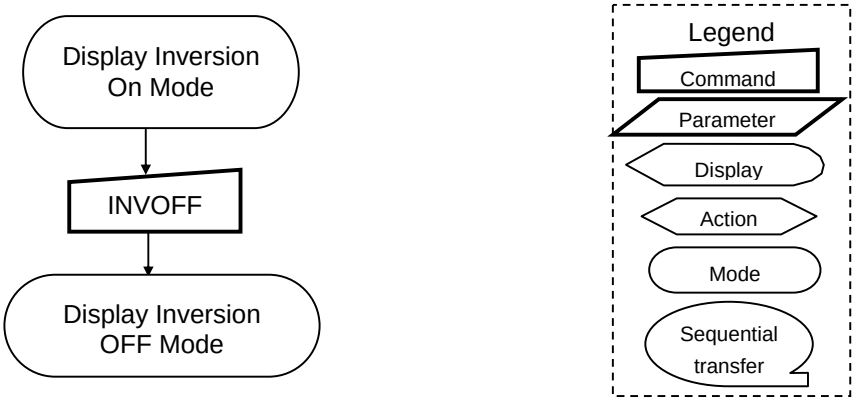
Description	This command is used to recover from display inversion mode. This command makes no change of contents of frame memory. This command does not change any other status.
Restriction	This command has no effect when module is already inversion off mode.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion off
S/W Reset	Display Inversion off
H/W Reset	Display Inversion off

Flow Chart



7.1.17 INVON: Display Inversion On (21h)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
INVON	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)
Parameter	No Parameter												

NOTE: "-" Don't care

Description

This command is used to enter into display inversion mode

This command makes no change of contents of frame memory. Every bit is inverted form the frame memory to the display.

This command does not change any other status.

Restriction

This command has no effect when module is already Inversion On mode.

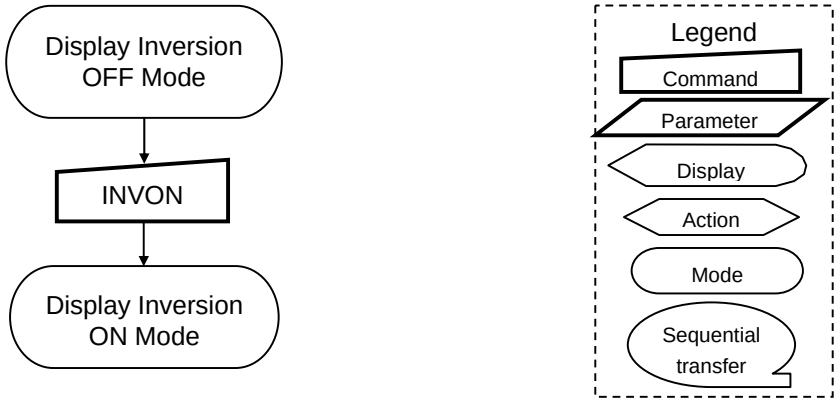
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion off
S/W Reset	Display Inversion off
H/W Reset	Display Inversion off

Flow Chart



7.1.18 GAMSET: Gamma Set (26h)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
INVON	0	↑	1	-	0	0	1	0	0	1	0	1	(26h)
Parameter	1	↑	1	-	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	-

NOTE: "-" Don't care

Description

This command is used to select the desired Gamma curve for the current display. A maximum of 4 curves can be selected. The curves are defined in Fig 5.9.3 The curve is selected by setting the appropriate bit in the parameter as described in the Table.

GC [7:0]	Parameter	Curve Selected
01h	GC0	Gamma Curve 1
02h	GC1	Gamma Curve 2
04h	GC2	Gamma Curve 3
08h	GC3	Gamma Curve 4

Note: All other values are undefined.

Restriction

Values of GC [7:0] not shown in table above are invalid and will not change the current selected Gamma curve until valid is received.

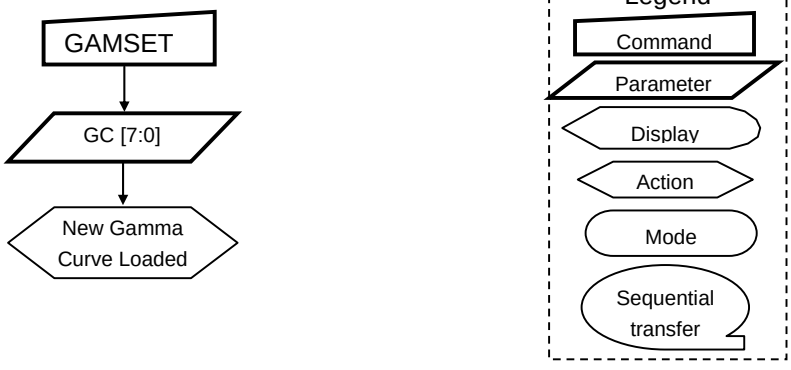
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	01h
S/W Reset	01h
H/W Reset	01h

Flow Chart



7.1.19 DISPOFF: Display Off (28h)

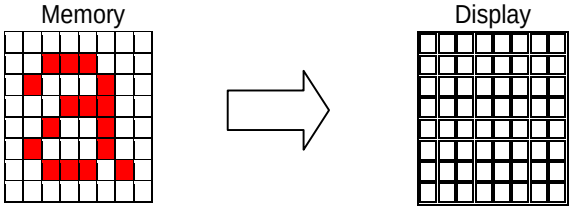
Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DISPOFF	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)
Parameter	No Parameter												

NOTE: "-" Don't care

Description

This command is used to enter into DISPLAY OFF mode. In this mode, the output from DDRAM is disabled and blank page is inserted for two frames.
This command makes no change of contents of DDRAM.
This command does not change any other status.
There will be no abnormal visible effect on the display.
Exit from this command by Display On (29h)

(Example)



Restriction

This command has no effect when module is already in Display Off mode.

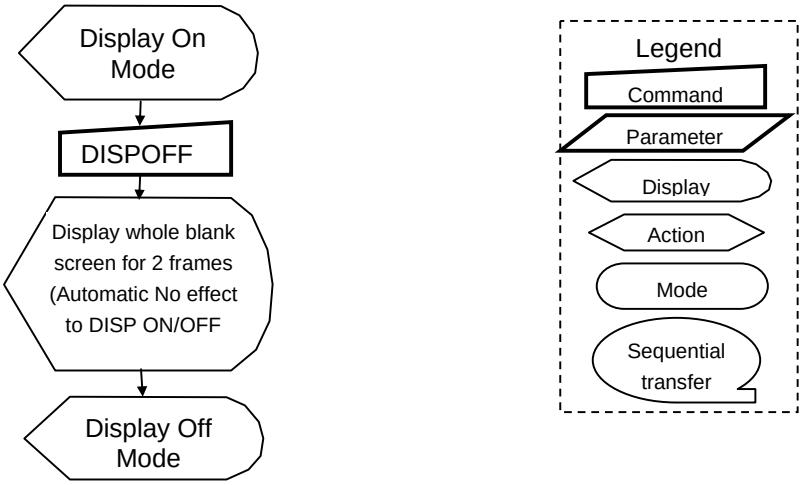
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

Flow Chart



7.1.20 DISPON: Display On (29h)

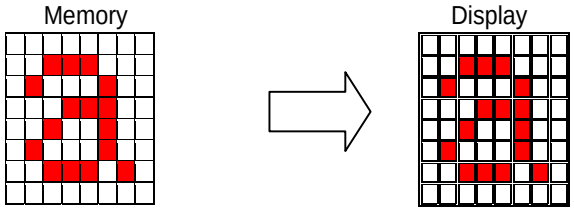
Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DISPON	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)
Parameter	No Parameter												

NOTE: "-" Don't care

Description

This command is used to recover from DISPLAY OFF mode. Output from the DDRAM is enabled.
This command makes no change of contents of DDRAM.
This command does not change any other status.

(Example)



Restriction

This command has no effect when module is already in Display On mode.

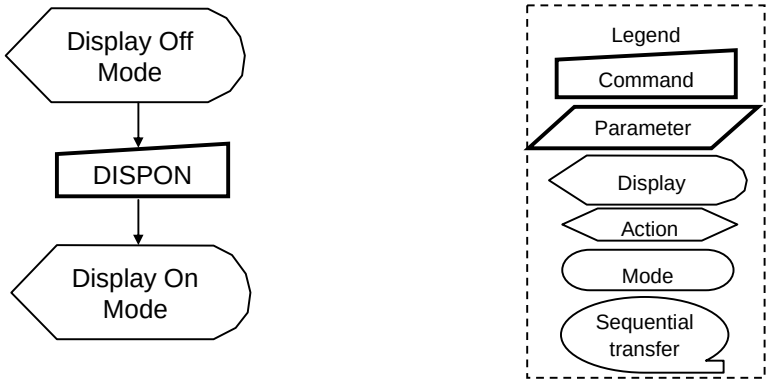
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

Flow Chart



7.1.21 CASET: Column Address Set (2Ah)

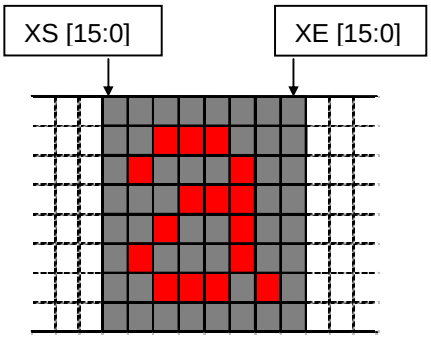
Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
CASET	0	↑	1	-	0	0	1	0	1	0	1	0	(2Ah)
1st Parameter	1	↑	1	-	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	-
2nd Parameter	1	↑	1	-	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	-
3rd Parameter	1	↑	1	-	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	-
4th Parameter	1	↑	1	-	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	-

NOTE: "-" Don't care

Description

This command is used to define area of DDRAM where MPU can access.
This command makes no change on the other driver status.
The value of XS [15:0] and XE [15:0] are referred when RAMWR command comes.
Each value represents one column line in the DDRAM.

(Example)



Restriction

XS [15:0] always must be equal to or less than XE [15:0]
When XS [15:0] or XE [15:0] is greater than maximum address like below, data of out of range will be ignored.
(Parameter range: 0 ≤ XS [15:0] ≤ XE [15:0] ≤ 239 (00EFh)): MV="0"
(Parameter range: 0 ≤ XS [15:0] ≤ XE [15:0] ≤ 319 (013Fh)): MV="1"
(about MV register, refer section 6.1.30 (Row / Column exchange))

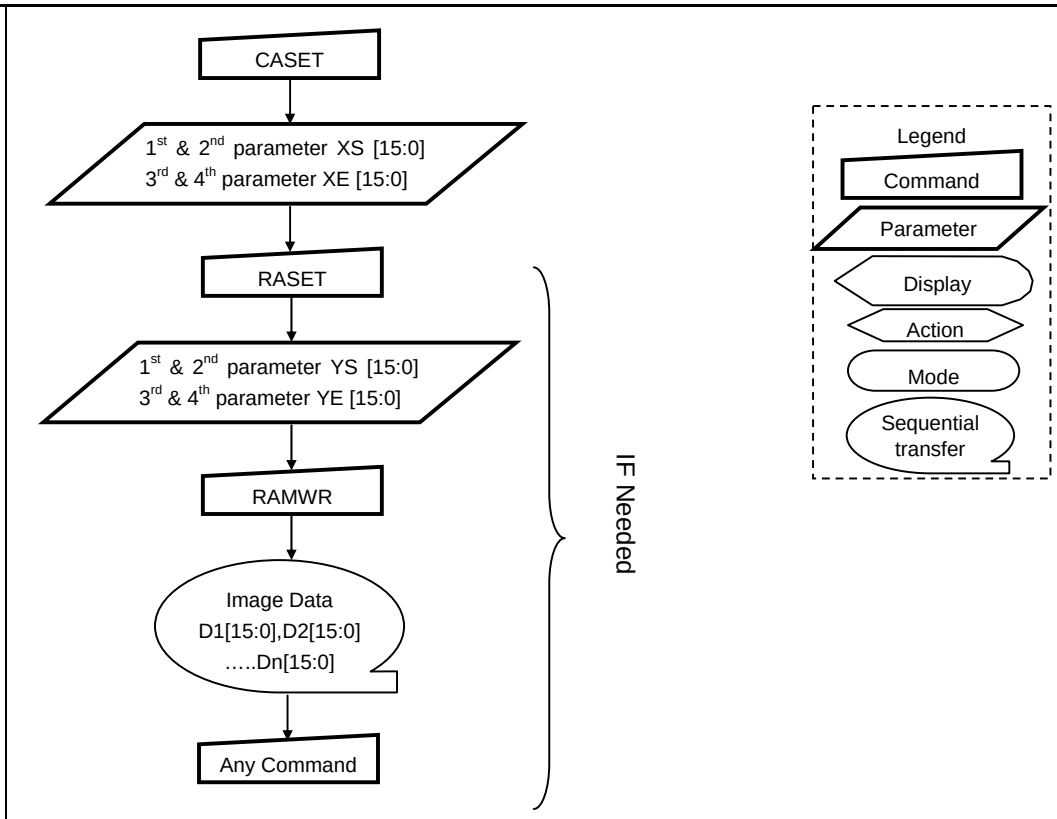
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	XS [15:0]	XE [15:0] (MV=0)	XE [15:0] (MV=1)
Power On Sequence	0000h	00EFh(239d)	
S/W Reset	0000h	00EFh(239d)	013Fh(319d)
H/W Reset	0000h	00EFh(239d)	

Flow Chart


CASET
1st & 2nd parameter XS [15:0]
3rd & 4th parameter XE [15:0]
RASET
1st & 2nd parameter YS [15:0]
3rd & 4th parameter YE [15:0]
RAMWR
Image Data
D1[15:0],D2[15:0]
…..Dn[15:0]
Any Command
IF Needed
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

7.1.22 RASET: Row Address Set (2Bh)

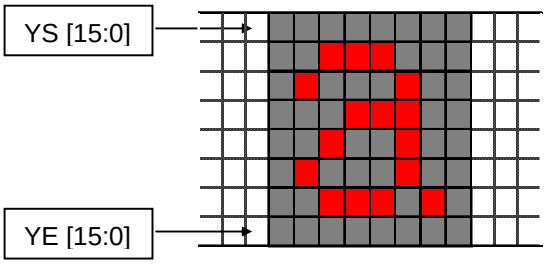
Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RASET	0	↑	1	-	0	0	1	0	1	0	1	1	(2Bh)
1st Parameter	1	↑	1	-	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	-
2nd Parameter	1	↑	1	-	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	-
3rd Parameter	1	↑	1	-	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	-
4th Parameter	1	↑	1	-	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	-

NOTE: "-" Don't care

Description

This command is used to define area of DDRAM where MPU can access.
This command makes no change on the other driver status.
The value of YS [15:0] and YE [15:0] are referred when RAMWR command comes.
Each value represents one column line in the DDRAM.

(Example)



Restriction

YS [15:0] always must be equal to or less than YE [15:0]
When YS [15:0] or YE [15:0] are greater than maximum row address like below, data of out of range will be ignored.
(Parameter range: 0 ≤ YS [15:0] ≤ YE [15:0] ≤ 319 (013Fh)): MV="0"
(Parameter range: 0 ≤ YS [15:0] ≤ YE [15:0] ≤ 239 (00EFh)): MV="1"
(about MV register, refer section 6.1.30 (Row / Column exchange))

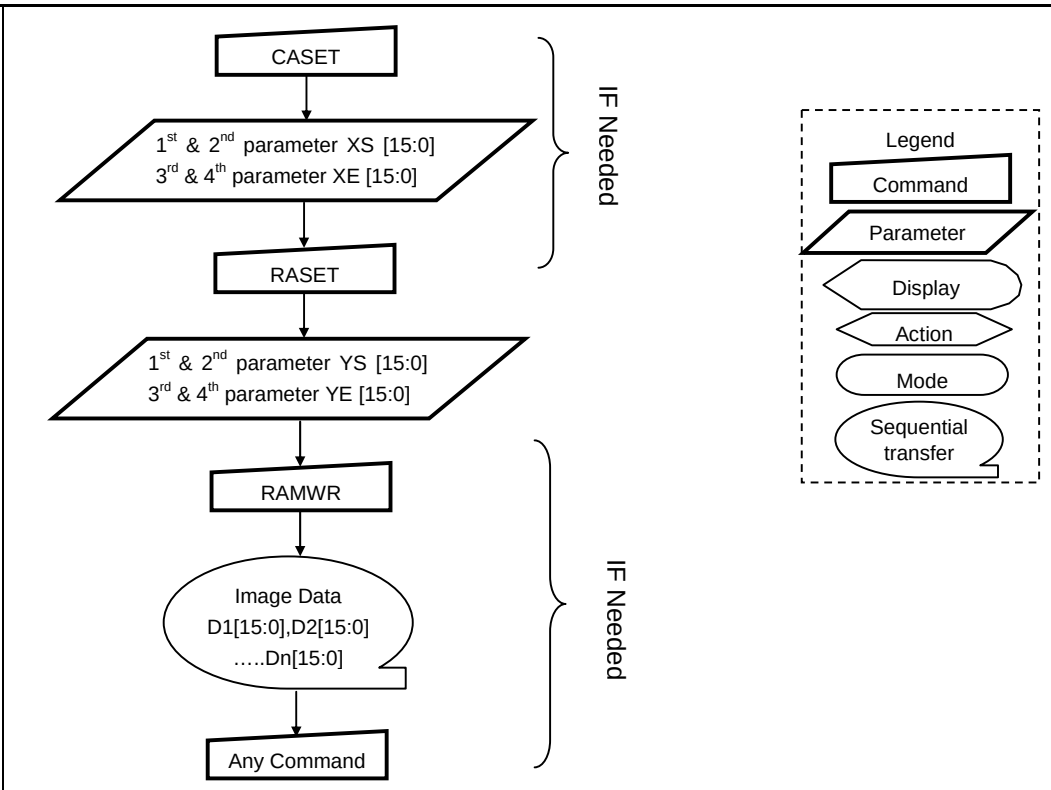
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	YS [15:0]	YE [15:0] (MV=0)	YE [15:0] (MV=1)
Power On Sequence	0000h	013Fh(319d)	
S/W Reset	0000h	013Fh(319d)	00EFh (239d)
H/W Reset	0000h	013Fh(319d)	

Flow Chart


CASET
1st & 2nd parameter XS [15:0]
3rd & 4th parameter XE [15:0]
RASET
1st & 2nd parameter YS [15:0]
3rd & 4th parameter YE [15:0]
RAMWR
Image Data
D1[15:0],D2[15:0]
…..Dn[15:0]
Any Command
IF Needed
IF Needed
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

7.1.23 RAMWR: Memory Write (2Ch)

Inst / Para	DC	WRB	RDB	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RAMWR	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)
Data write	1	↑	1	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	-
:	:	:	:	:	:	:	:	:	:	:	:	:	:
Data write	1	↑	1	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	-

NOTE: "-" Don't care

Description

This command is used to transfer data MPU to DDRAM.
This command makes no change to the other driver status.
When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions.
The Start Column/Start Row positions are different in accordance with MADCTR setting. (See 5.2.3)
Then D [15:0] is stored in DDRAM and the column register and the row register increment as in ***Fig 5.2.4***.
Sending any other command can stop Frame Write.

Restriction

In all color modes, there is no restriction on length of parameters.

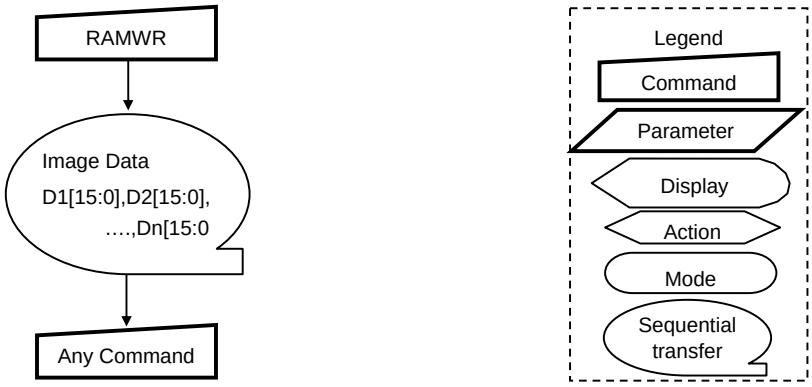
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart



7.1.24 RAMRD: Memory Read (2Eh)

Inst / Para	DC	WRB	RDB	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RAMRD	0	↑	1	-	0	0	1	0	1	1	1	0	(2Eh)
Dummy read	1	1	↑	-	-	-	-	-	-	-	-	-	-
Data read	1	1	↑	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	-
:	:	:	:	:	:	:	:	:	:	:	:	:	:
Data read	1	1	↑	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	-

NOTE: "-" Don't care

Description

This command is used to transfer data from DDRAM to MPU.
This command makes no change to the other driver status.
When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions.
The Start Column/Start Row positions are different in accordance with MADCTR setting.
(See section 5.2.3)
Then D[15:0] is read back from the DDRAM and the column register and the row register increment as in Fig. 5.2.4.
Frame Read can be canceled by sending any other command.

Restriction

In all color modes, there is no restriction on length of parameters.
Note – Memory Read is only possible via the Parallel Interface.

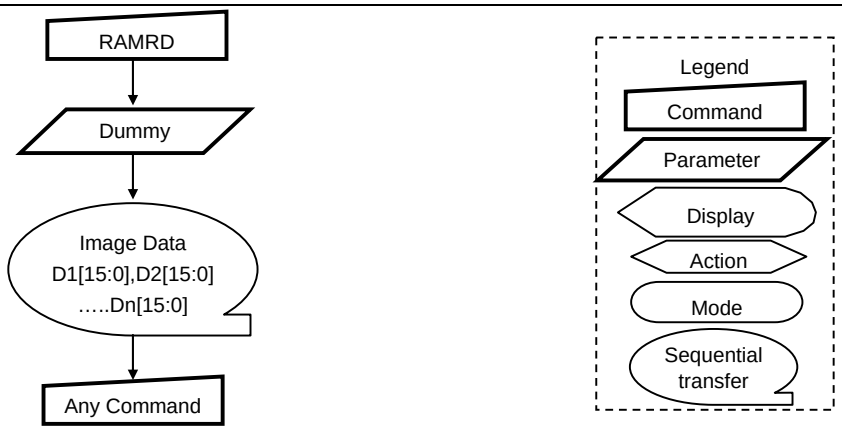
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart



7.1.25 PTLAR: Partial Area (30h)

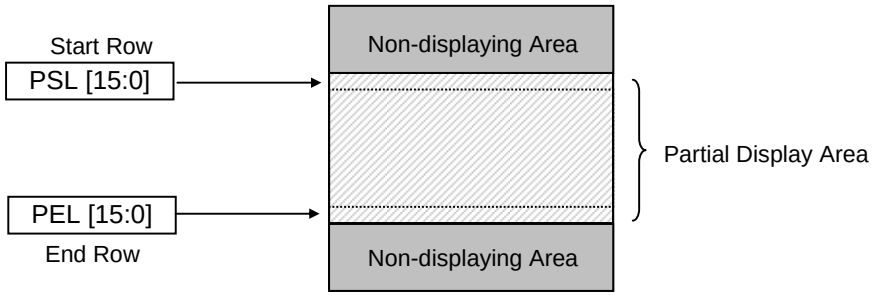
Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PTLAR	0	↑	1	-	0	0	1	1	0	0	0	0	(30h)
1st parameter	1	↑	1	-	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8	-
2nd parameter	1	↑	1	-	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	-
3rd parameter	1	↑	1	-	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8	-
4th parameter	1	↑	1	-	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	-

NOTE: "-" Don't care

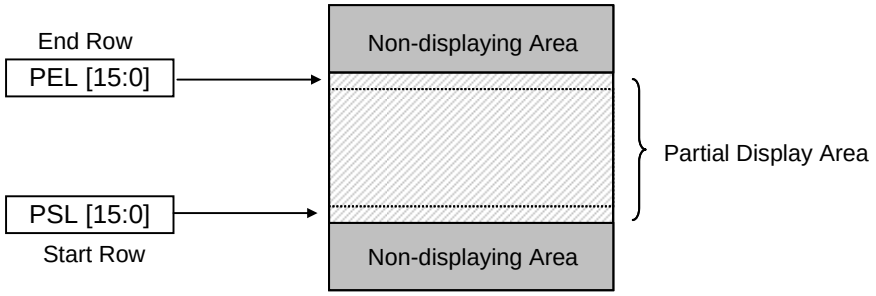
Description

This command defines the partial mode's display area. There are 4 parameters associated with this command, the first defines the Start Row (PSL) and the second the End Row (PEL), as illustrated in the figures below. PSL and PEL refer to the DDRAM row address counter.

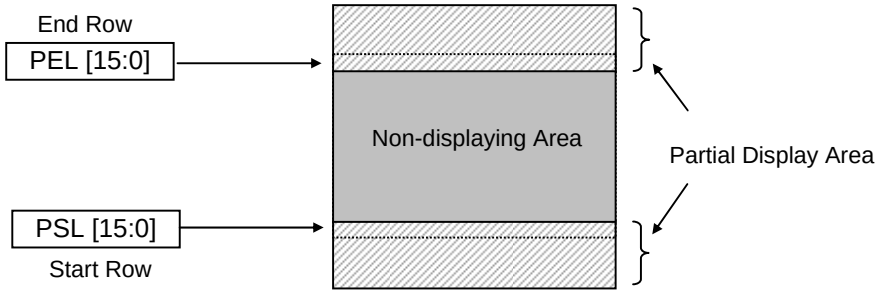
If End Row > Start Row when MADCTL ML=0:



If End Row > Start Row when MADCTL ML=1:



If End Row < Start Row when MADCTL ML=0:



If End Row = Start Row then the Partial Area will be one row deep.

Restriction

PSL[15:0] and PEL[15:0] should have below range

(Parameter range: 0 ≤ PSL[15:0], PEL[15:0] ≤ 319 (013Fh))

Register Availability

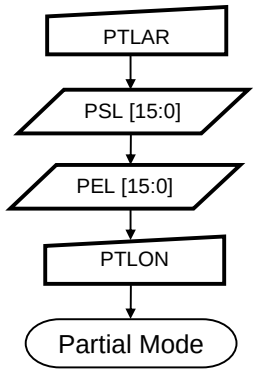
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

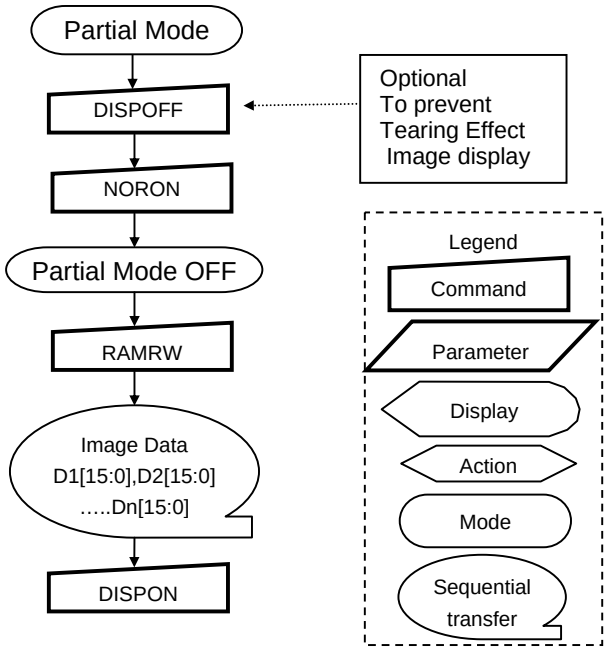
Status	Default Value	
	PSL [15:0]	PEL [15:0]
Power On Sequence	0000h	013Fh
S/W Reset	0000h	013Fh
H/W Reset	0000h	013Fh

Flow Chart

1. To Enter Partial Mode



2. To Exit Partial Mode



7.1.26 TEOFF: Tearing Effect Line OFF (34h)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEOFF	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)
Parameter	No Parameter												

NOTE: "-" Don't care

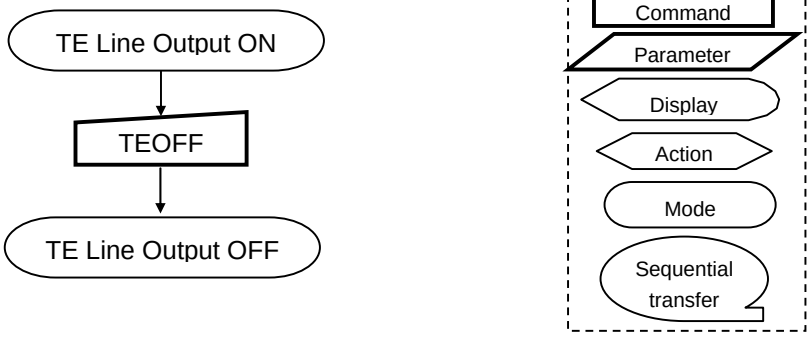
Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.
Restriction	This command has no effect when Tearing Effect output is already OFF.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Off
S/W Reset	Off
H/W Reset	Off

Flow Chart



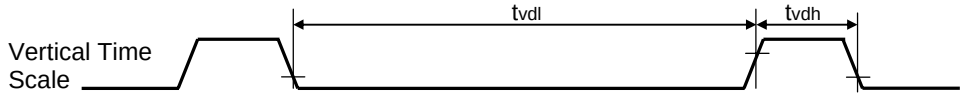
7.1.27 TEON: Tearing Effect Line ON (35h)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEON	0	↑	1	-	0	0	1	1	0	1	0	1	(35h)
Parameter	1	↑	1	-	-	-	-	-	-	-	-	M	-

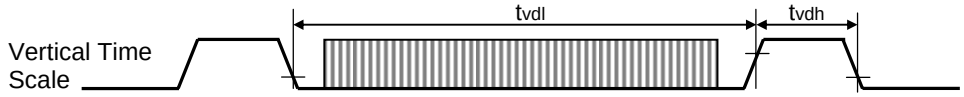
NOTE: "-" Don't care

Description

This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTR bit ML.
The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line. ("-"=Don't Care).
When M=0: The Tearing Effect Output line consists of V-Blanking information only.



When M=1: The Tearing Effect Output line consists of both V-Blanking and H-Blinking information.



See Section 5.2.7 for more information.
Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction

This command has no effect when Tearing Effect output is already OFF.

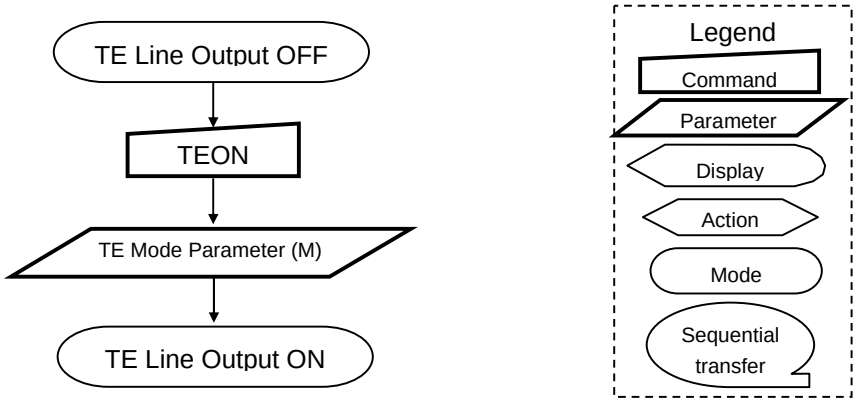
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Tearing effect off & M=0
S/W Reset	Tearing effect off & M=0
H/W Reset	Tearing effect off & M=0

Flow Chart



7.1.28 MADCTR: Memory Data Access Control (36h)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
MADCTR	0	↑	1	-	0	0	1	1	0	1	1	0	(36h)
Parameter	1	↑	1	-	MY	MX	MV	ML	RGB	-	-	-	-

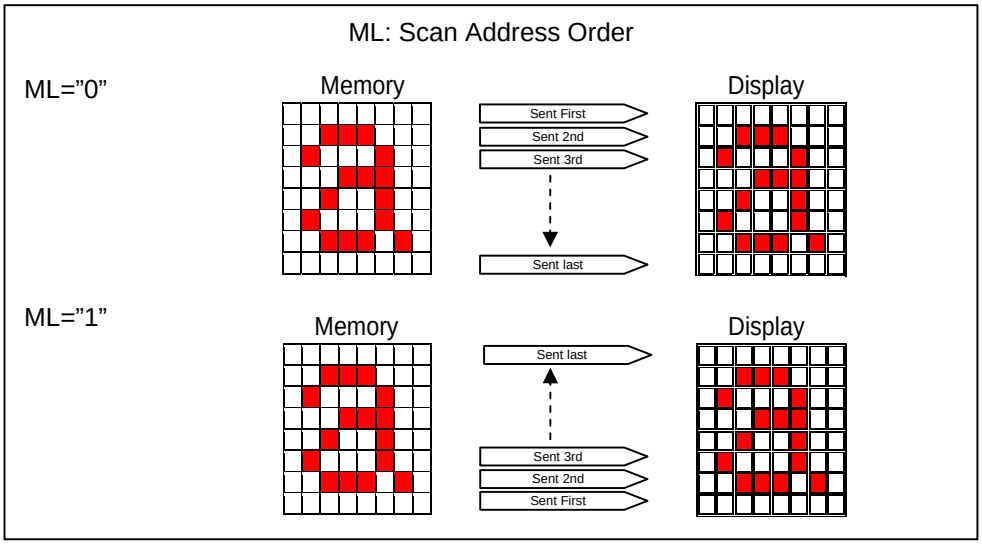
NOTE: "-" Don't care

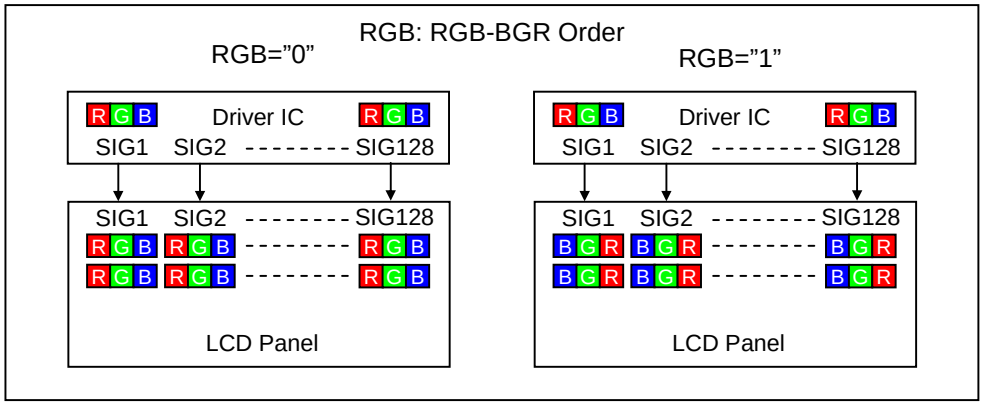
Description

This command defines read/write scanning direction of DDRAM.
This command makes no change on the other driver status.

Bit Assignment

Bit	NAME	DESCRIPTION
MY	ROW ADDRESS ORDER	These 3bits controls MPU to memory write/read direction. (See Section 5.2.3)
MX	COLUMN ADDRESS ORDER	
MV	ROW/COLUMN EXCHANGE	
ML	SCAN ADDRESS ORDER	LCD refresh direction control
RGB	RGB-BGR ORDER	Color selector switch control. DDRAM must be updated after the RGB bit change. (0=RGB color filter panel, 1=BGR color filter panel)





Restriction

D2, D1 and D0 of the 1st parameter are set to '000'internally.

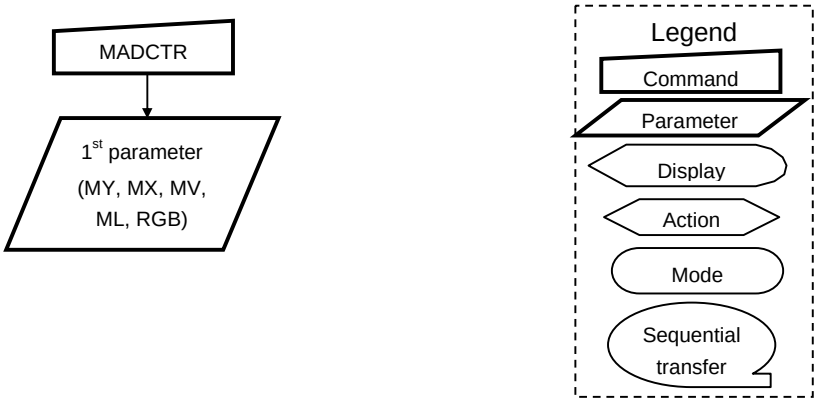
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	MY=0,MX=0,MV=0,ML=0,RGB=0
S/W Reset	No Change
H/W Reset	MY=0,MX=0,MV=0,ML=0,RGB=0

Flow Chart



7.1.29 IDMOFF: Idle Mode Off (38h)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)
Parameter	No Parameter												

NOTE: "-" Don't care

Description

This command is used to recover from Idle mode on.
There will be no abnormal visible effect on the display mode change transition.
In the idle off mode,

1. LCD can display maximum 4k, 65k, 262k or 16M-colors.
2. Normal frame frequency is applied.

Restriction

This command has no effect when module is already in idle off mode.

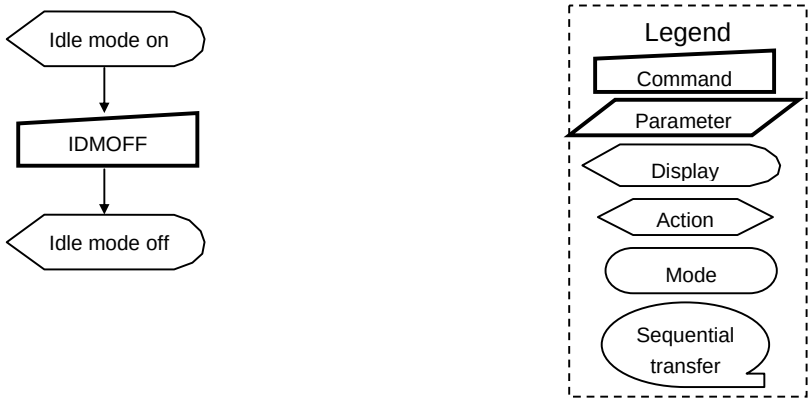
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off
H/W Reset	Idle Mode Off

Flow Chart



7.1.30 IDMON: Idle Mode On (39h)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
IDMON	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)
Parameter	No Parameter												

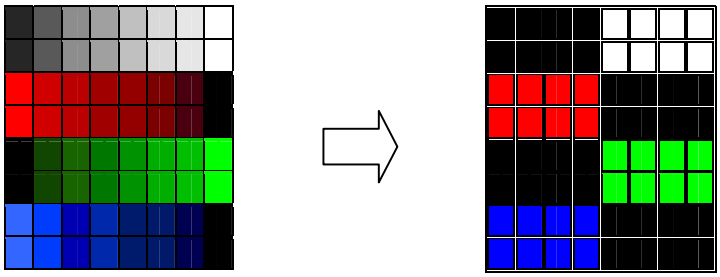
NOTE: "-" Don't care

Description

This command is used to enter into Idle mode on.
There will be no abnormal visible effect on the display mode change transition.
In the idle on mode,
1. Color expression is reduced. The primary and the secondary colors using MSB of each R,G and B in the DDRAM, 8 color depth data is displayed.
2. 8-Color mode frame frequency is applied.
3. Exit from IDMON by Idle Mode Off (38h) command

(Example)

Memory Display



"X": don't care

Color	$R_7 R_6 R_5 R_4 R_3 R_2 R_1 R_0$	$G_7 G_6 G_5 G_4 G_3 G_2 G_1 G_0$	$B_7 B_6 B_5 B_4 B_3 B_2 B_1 B_0$
Black	0XXXXXXX	0XXXXXXX	0XXXXXXX
Blue	0XXXXXXX	0XXXXXXX	1XXXXXXX
Red	1XXXXXXX	0XXXXXXX	0XXXXXXX
Magenta	1XXXXXXX	0XXXXXXX	1XXXXXXX
Green	0XXXXXXX	1XXXXXXX	0XXXXXXX
Cyan	0XXXXXXX	1XXXXXXX	1XXXXXXX
Yellow	1XXXXXXX	1XXXXXXX	0XXXXXXX
White	1XXXXXXX	1XXXXXXX	1XXXXXXX

Restriction

This command has no effect when module is already in idle on mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off
H/W Reset	Idle Mode Off

Flow Chart	

Idle mode off
IDMON
Idle mode on
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

7.1.31 COLMOD: Interface Pixel Format (3Ah)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
COLMOD	0	↑	1	-	0	0	1	1	1	0	1	0	(3Ah)
Parameter	1	↑	1	-	-	RP2	RP1	RP0	-	P2	P1	P0	-

NOTE: "-" Don't care

Description

This command is used to define the format of RGB picture data, which is to be transferred via the MPU(P2-0) & RGB(RP2-0) Interface. The formats are shown in the table:

Interface Pixel Format	P2(RP2)	P1(RP1)	P0(RP0)
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
Not Defined	0	1	1
Not Defined	1	0	0
Not Defined	1	0	1
18Bit/Pixel	1	1	0
24Bit/Pixel	1	1	1

NOTE: In 18 Bit/Pixel mode, the LSB Expansion is applied to transfer data into the DDRAM.

Restriction

There is no visible effect until the DDRAM is written to.

Register Availability

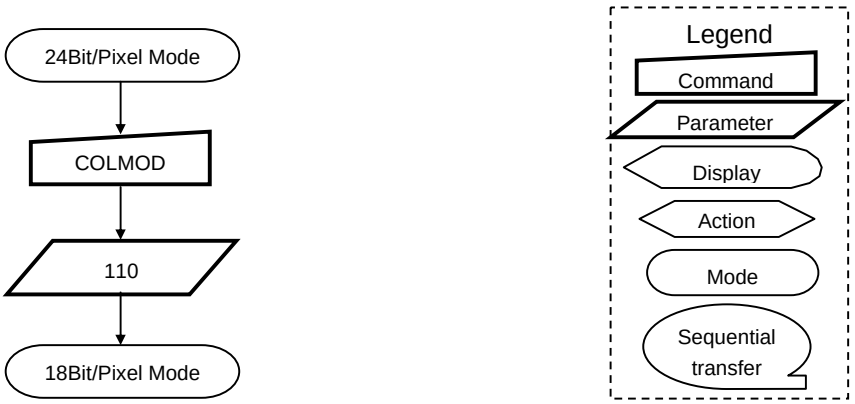
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default
Power On Sequence	24Bit/Pixel
S/W Reset	No Change
H/W Reset	24Bit/Pixel

Flow Chart

Example:



7.1.32 WRDISBV : Write Display Brightness (51h)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
WRDISBV	0	↑	1	-	0	1	0	1	0	0	0	1	(51h)
Parameter	1	↑	1	-	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	-

NOTE: "-" Don't care

Description

This command is used to adjust then brightness value of the display.

It should be checked what the relationship between this written value and output brightness of the display is. This relationship is defined on the display module specification.

00h value means the lowest brightness and FFh value means the highest brightness.

Restriction

The display supplier cannot use this command for tuning(e.g. factory tuning. Etc), because this command is only for Nokia.

Register Availability

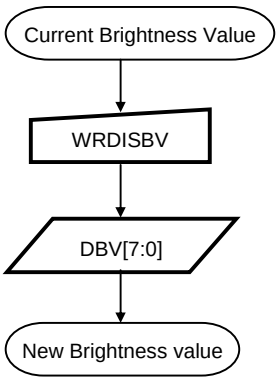
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

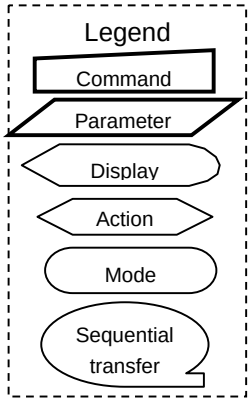
Default

Status	Default
Power On Sequence	FFh
S/W Reset	FFh
H/W Reset	FFh

Flow Chart

Example:





7.1.33 RDDISBV : Read Display Brightness (52h)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDDISBV	0	↑	1	-	0	1	0	1	0	0	1	0	(52h)
Dummy read	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	-

NOTE: "-" Don't care

Description

This command returns the brightness value of the display.

It should be checked what the relationship between this written value and output brightness of the display is. This relationship is defined on the display module specification.

00h value means the lowest brightness and FFh value means the highest brightness.

Restriction

Register Availability

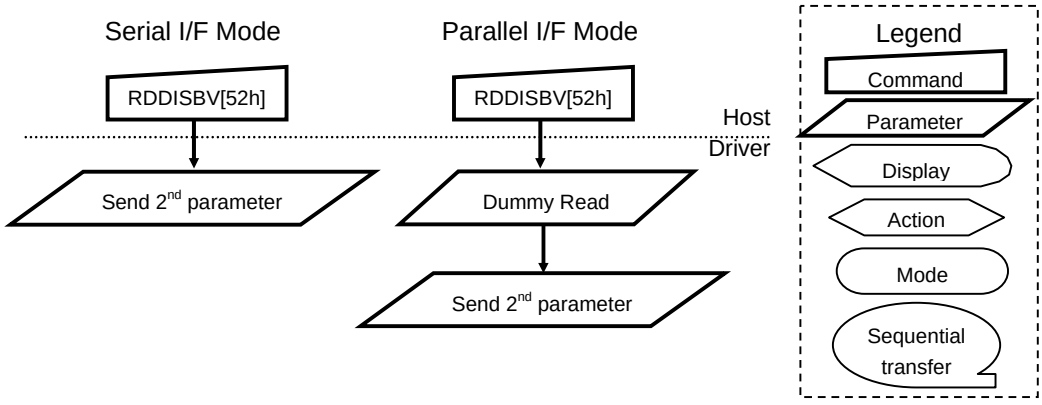
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default
Power On Sequence	FFh
S/W Reset	FFh
H/W Reset	FFh

Flow Chart

Example:



7.1.34 WRCTRLD: Write CTRL Display (53h)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
WRCTRLD	0	↑	1	-	0	1	0	1	0	0	1	1	(53h)
Parameter	1	↑	1	-	-	-	BCTRL	-	-	BL	-	-	-

NOTE: "-" Don't care

Description

This command is used to control brightness setting.

BCTRL : Brightness Controll Block On/Off. This bit is always used to switch brightness for display .
"0" = Off (Brightness registers are 00h)
"1" = On (Brightness registers are active)

BL : Backlight Control On/Off
"0" = Off (Completely turn off backlight circuit : Control Lines must be low.)
"1" = On

Restriction

The display supplier cannot use this command for tuning(e.g. factory tuning. Etc), because this command is of only for Nokia.

Register Availability

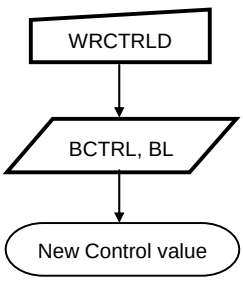
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

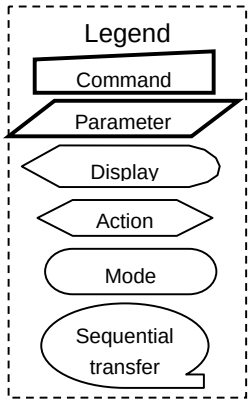
Default

Status	Default
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart

Example:





7.1.35 RDCTRLD : Read CTRL Value Display (54h)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDCTRLD	0	↑	1	-	0	1	0	1	0	1	0	0	(54h)
Dummy read	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	-	-	BCTRL	-	-	BL	-	-	-

NOTE: "-" Don't care

Description

This command returns the brightness control value. (See Chapter 7.1.34 WRCTRLD)

BCTRL : Brightness Controll Block On/Off. This bit is always used to switch brightness for display .
"0" = Off (Brightness registers are 00h)
"1" = On (Brightness registers are active)

BL : Backlight Control On/Off
"0" = Off (Completely turn off backlight circuit : Control Lines must be low.)
"1" = On

Restriction

Register Availability

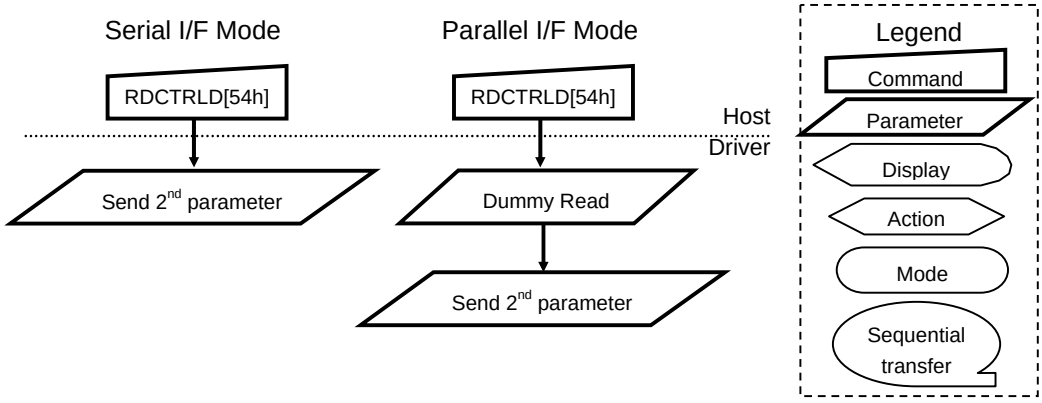
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart

Example:



7.1.36 WRCABC: Write Content Adaptive Brightness (55h)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
WRCTRLD	0	↑	1	-	0	1	0	1	0	0	1	1	(53h)
Parameter	1	↑	1	-	-	-	-	-	-	-	C1	C0	-

NOTE: "-" Don't care

Description

This command is used to set parameters for image content based adaptive brightness control functionality.

There is possible to use 4 different modes for content adaptive image functionality, which are difined on a table below

C1	C0	Function	Note
0	0	OFF	
0	1	User Interface Image	
1	0	Still Picture	
1	1	Moving Image	

Restriction

Register Availability

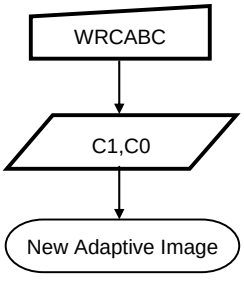
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

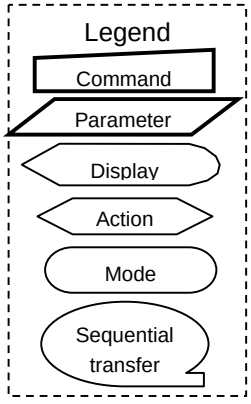
Default

Status	Default
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart

Example:





7.1.37 RDCABC : Read Content Adaptive Brightness (56h)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDCABC	0	↑	1	-	0	1	0	1	0	1	1	0	(56h)
Dummy read	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	-	-	-	-	-	-	C1	C0	-

NOTE: "-" Don't care

Description

This command is used to read the settings for image content based adaptive brightness control functionality.

There is possible to use 4 different modes for content adaptive image functionality, which are difined on a table below

C1	C0	Function	Note
0	0	OFF	
0	1	User Interface Image	
1	0	Still Picture	
1	1	Moving Image	

Restriction

Register Availability

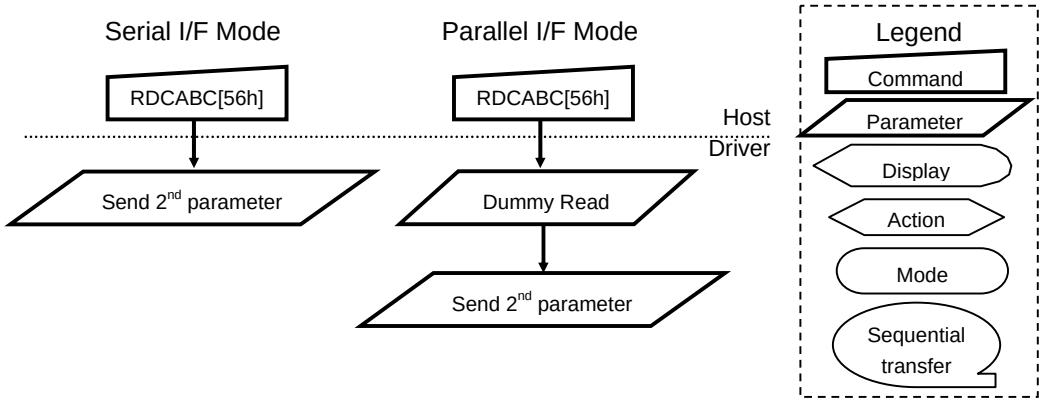
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart

Example:



7.1.38 RDID1: Read ID1 Value (DAh)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID1	0	↑	1	-	1	1	0	1	1	0	1	0	(DAh)
Dummy read	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-

NOTE: "-" Don't care

Description

This read byte returns 8-bit LCD module's manufacturer ID

The 1st parameter is dummy data

The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID.

NOTE: See command RDDID (04h), 2nd parameter.

Restriction

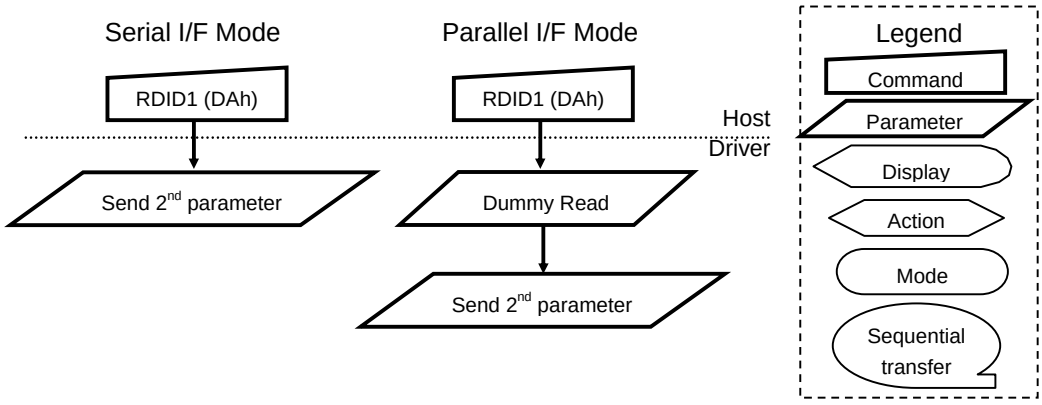
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Not Fixed
S/W Reset	Not Fixed
H/W Reset	Not Fixed

Flow Chart



7.1.39 RDID2: Read ID2 Value (DBh)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID2	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)
Dummy read	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-

NOTE: "-" Don't care

Description

This read byte returns 8-bit LCD module/driver version ID
The 1st parameter is dummy data
The 2nd parameter (ID26 to ID20): LCD module/driver version ID
Parameter Range: ID=80h to FFh
NOTE: See command RDDID (04h), 3rd parameter.

Restriction

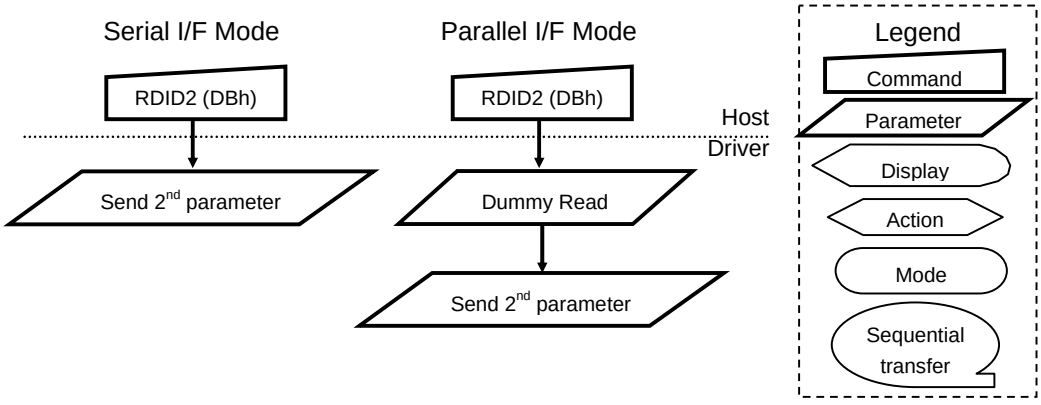
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Not Fixed
S/W Reset	Not Fixed
H/W Reset	Not Fixed

Flow Chart



7.1.40 RDID3: Read ID3 Value (DCh)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID3	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)
Dummy read	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-

NOTE: "-" Don't care

Description

This read byte returns 8-bit LCD module/driver ID.

The 1st parameter is dummy data

The 2nd parameter (ID37 to ID30): LCD module/driver ID.

NOTE: See command RDDID (04h), 4th parameter.

Restriction

-

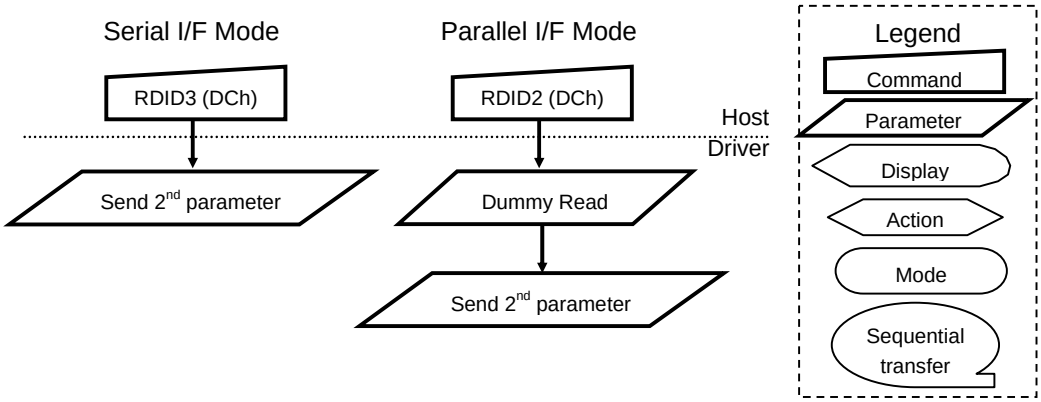
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Not Fixed
S/W Reset	Not Fixed
H/W Reset	Not Fixed

Flow Chart



7.1.41 IFMODE: Set Display Interface Mode (B0h)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
IFMODE	0	↑	1	-	1	0	1	1	0	0	0	0	(B0h)
1st parameter	1	↑	1	-	-	-	-	-	-	-	IF1	IF0	-
2nd parameter	1	↑	1	-	-	-	DW	-	DP	EP	HSP	VSP	-

NOTE: "-" Don't care

Description

Sets the operation status of the display interface. The setting becomes effective as soon as the command is received.

1st parameter: Interface mode set

IF1	IF0	Data Transfer Mode
0	0	MPU data transfer
0	1	RGB data transfer1
1	0	RGB data transfer2
1	1	RGB data transfer3

2nd parameter: RGB Interface bus width set

DW	RGB Interface Data Width
0	24-bit (1-transfer for one pixel)
1	8-bit (1-transfer for one pixel)

2nd parameter: Clock polarity set for RGB interface
DP: DCK polarity set ("0"=data fetched at the rising edge, "1"=data fetched at the falling edge)
EP: ENABLE polarity ("0"= High enable for RGB interface, "1"=Low enable for RGB interface)
HSP: HSYNC polarity ("0"=Low level sync clock, "1"=High level sync clock)
VSP: VSYNC polarity ("0"= Low level sync clock, "1"= High level sync clock)

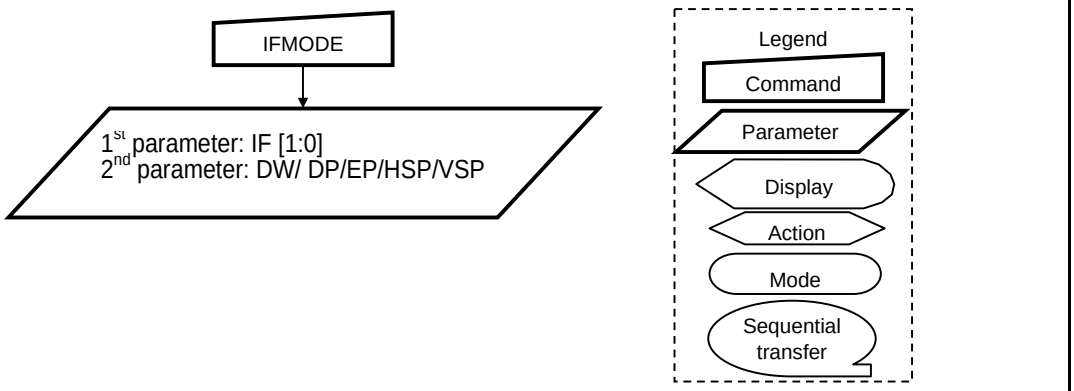
F

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	IF [1:0]	DW	DP/EP/HSP/VSP
Power On Sequence	00	0	0/0/0/0
S/W Reset	00	0	0/0/0/0
H/W Reset	00	0	0/0/0/0

Flow Chart	

IFMODE
1st parameter: IF [1:0]
2nd parameter: DW/ DP/EP/HSP/VSP
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

7.1.42 DISCLK: Display Clock Set (B1h)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DISCLK	0	↑	1	-	1	0	1	1	0	0	0	1	(B1h)
1st parameter	1	↑	1	-	HA7	HA6	HA5	HA4	HA3	HA2	HA1	HA0	-
2nd parameter	1	↑	1	-	-	-	BPA5	BPA4	BPA3	BPA2	BPA1	BPA0	-
3rd parameter	1	↑	1	-	-	-	FPA5	FPA4	FPA3	FPA2	FPA1	FPA0	-
4th parameter	1	↑	1	-	HB7	HB6	HB5	HB4	HB3	HB2	HB1	HB0	-
5th parameter	1	↑	1	-	-	-	BPB5	BPB4	BPB3	BPB2	BPB1	BPB0	-
6th parameter	1	↑	1	-	-	-	FPB5	FPB4	FPB3	FPB2	FPB1	FPB0	-

Description

Display clock condition set.

1st to 4th parameter: Display clock set for full colour display mode.

HA [8:0]: Number of clocks during 1H = HA

BPA [5:0]: Number of lines for vertical back porch

FPA [5:0]: Number of lines for vertical front porch

5th to 8th parameter: Display clock set for 8-colour display mode.

HB [8:0]: Number of clocks during 1H = HB

BPB [5:0]: Number of lines for vertical back porch

FPB [5:0]: Number of lines for vertical front porch

By using DISCLK command, frame frequency can be set like below

fFRA (Hz) = 1 / ((Number of gate + 1 dummy gate + BPA + FPA) * ((HA+1) * 2usec))

for full colour display mode

fFRB (Hz) = 1 / ((Number of gate + 1 dummy gate + BPB + FPB) * ((HB+1) * 2usec))

for 8-colour display mode

BPA (BPB) and FPA (FPB) are related to the vertical mode TE signal pulse width.

TE (vertical mode, high pulse width) = (BFA + FPA+2) * ((HA+1) * 2usec)

for full colour display mode

TE (vertical mode, high pulse width) = (BFB + FPB+2) * ((HB+1) * 2usec)

for 8-colour display mode

Restriction

-

Register Availability

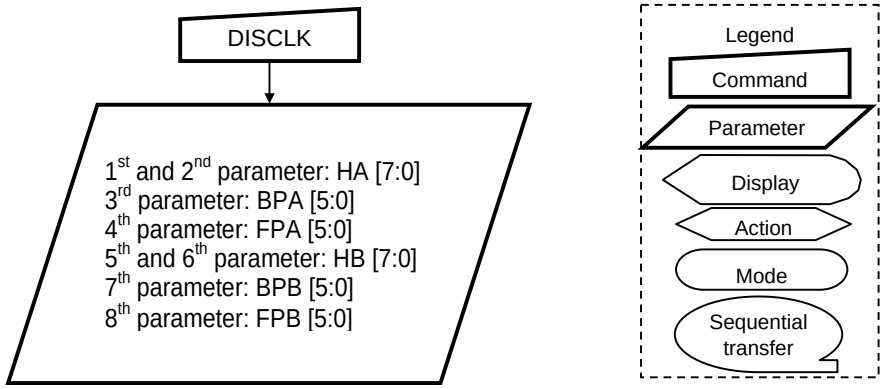
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value					
	HA [7:0]	BPA [5:0]	FPA [5:0]	HB [7:0]	BPB [5:0]	FPB [5:0]
Power On Sequence	23d (17h)	16d (10h)	6d (06h)	28d (1Ch)	16d (10h)	6d (06h)
S/W Reset	23d (17h)	16d (10h)	6d (06h)	28d (1Ch)	16d (10h)	6d (06h)
H/W Reset	23d (17h)	16d (10h)	6d (06h)	28d (1Ch)	16d (10h)	6d (06h)

The default frame frequency (normal mode, 320 gate + 1 dummy gate)
= 1/((321+16+6)*(23+1)*2usec) = 60.8Hz
The default frame frequency (idle mode, 320 gate + 1 dummy gate)
= 1/((321+16+6)*(28+1)*2usec) = 50.2Hz
Vertical TE signal high pulse width
= (16+6+2)*(23+1)*2usec = 1,152 usec (for normal mode)
= (16+6+2)*(28+1)*2usec = 1,392 usec (for idle mode)

Flow Chart



7.1.43 INVCTR: Inversion Control (B2h)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
INVCTR	0	↑	1	-	1	0	1	1	0	0	1	0	(B2h)
1st parameter	1	↑	1	-	0	0	0	0	-	NLA2	NLA1	NLA0	-
2nd parameter	1	↑	1	-	0	0	0	0	-	NLB2	NLB1	NLB0	-

Description

Display inversion mode set

1st parameter: for full colour display mode

NLA2 to NLA0: line inversion value set

2nd parameter: for 8 colour display mode

NLB2 to NLB0: line inversion value set

NLA2 (NLB2)	NLA1 (NLB1)	NLA0 (NLB0)	Inversion
0	0	0	Frame inversion
0	0	1	1-Line inversion
0	1	0	2-Line inversion
0	1	1	3-Line inversion
1	0	0	4-Line inversion
1	0	1	5-Line inversion
1	1	0	6-Line inversion
1	1	1	7-Line inversion

Restriction

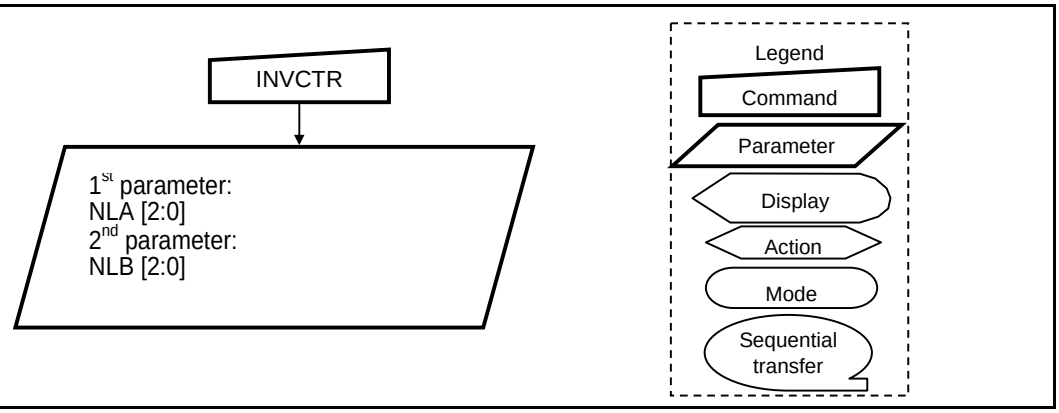
-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	1st parameter	2nd parameter
Power On Sequence	01h	00h
S/W Reset	01h	00h
H/W Reset	01h	00h

Flow Chart	

INVCTR
1st parameter:
NLA [2:0]
2nd parameter:
NLB [2:0]
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

7.1.44 REGCTR: Regulator Control (C0h)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
REGCTR	0	↑	1	-	1	1	0	0	0	0	0	0	(C0h)
1st parameter	1	↑	1	-	-	VR2	VR1	VR0	-	VS2	VS1	VS0	-

Description

Regulator voltage control

The 1st parameter:

VR [2:0]: VR regulator output control

VS [2:0]: VS regulator output control

VR [2:0]	VR output	VS [2:0]	VS/VG output
0	VR = 3.00V	0	VS = 3.00V
1	VR = 3.50V	1	VS = 3.50V
2	VR = 3.75V	2	VS = 3.75V
3	VR = 4.00V	3	VS = 4.00V
4	VR = 4.25V	4	VS = 4.25V
5	VR = 4.50V	5	VS = 4.50V
6	VR = 4.75V	6	VS = 4.75V
7	VR = 5.00V	7	VS = 5.00V

Restriction

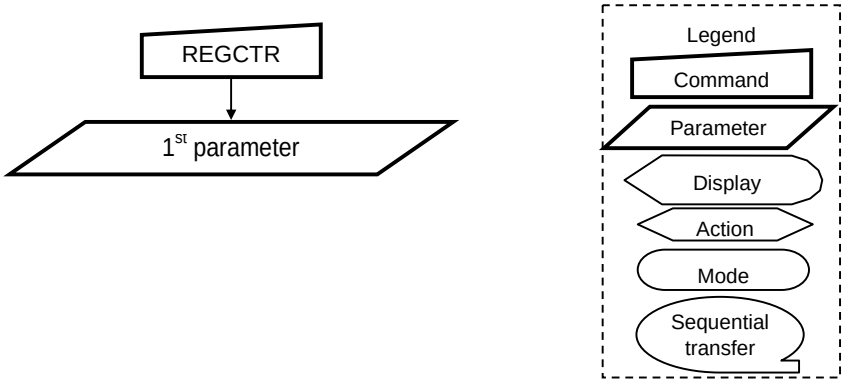
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	VR [2:0]	VS [2:0]
Power On Sequence	3h	5h
S/W Reset	3h	5h
H/W Reset	3h	5h

Flow Chart



7.1.45 VCOMCTR: VCOML / VCOMH Voltage Control (C1h)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VCOMCTR	0	↑	1	-	1	1	0	0	0	0	0	1	(C1h)
1st parameter	1	↑	1	-	-	-	VCLC5	VCLC4	VCLC3	VCLC2	VCLC1	VCLC0	-
2nd parameter	1	↑	1	-	-	-	VCHC5	VCHC4	VCHC3	VCHC2	VCHC1	VCHC0	-

NOTE: "-" Don't care

Description

VCOML / VCOMH Voltage Control

The 1st parameter: VCOML voltage control (See below table)

The 2nd parameter: VCOMH voltage control (See below table)

VCLC [5:0]	VCOML output voltage	VCHC [5:0]	VCOMH output voltage
0	VCOML = -2.00 V	0	VCOMH = +2.50 V
1	VCOML = -1.95 V	1	VCOMH = +2.55 V
2	VCOML = -1.90 V	2	VCOMH = +2.60 V
:	:	:	:
60	VCOML = +1.00V	60	VCOMH = +5.50V
61 ~ 63	Not permitted	61 ~ 63	Not permitted

Restriction

Default value of VCOMH will be fixed to the trimmed value during wafer test.

Register Availability

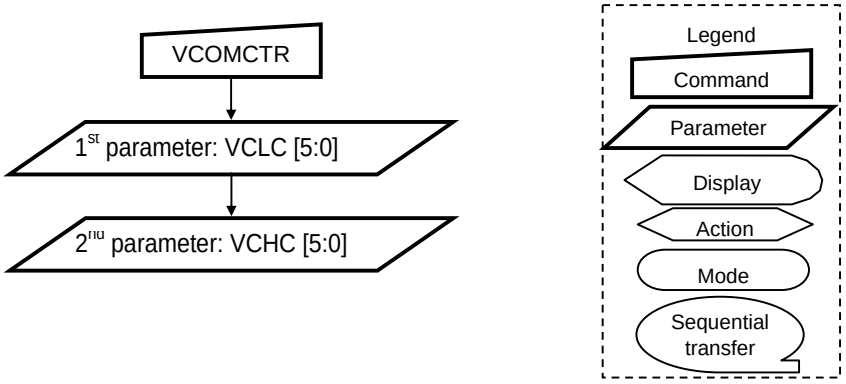
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	VCLC [5:0]	VCHC [5:0]
Power On Sequence	32h	See note
S/W Reset	32h	See note
H/W Reset	32h	See note

NOTE: After Wafer level test, the default value of VCHC will be trimmed to fit the target VCOM amplitude.

Flow Chart



7.1.46 GAMCTR1: Set Gamma Correction Characteristics (C8h)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GAMCTR1	0	↑	1	-	1	1	0	0	1	0	0	0	(C8h)
1st parameter	1	↑	1	-			GS102	GS101	GS100	GS112	GS111	GS110	
2nd parameter	1	↑	1	-			GS122	GS121	GS120	GS132	GS131	GS130	
3rd parameter	1	↑	1	-			GS142	GS141	GS140	GS152	GS151	GS150	
4th parameter	1	↑	1	-			GS162	GS161	GS160	GS172	GS171	GS170	

Description

Set the gray scale voltage to adjust the gamma characteristics of the TFT panel.
It apply to gamma curve selection by instruction code 26h.
1st to 4th parameter: Gamma curve1 adjustment register

Restriction

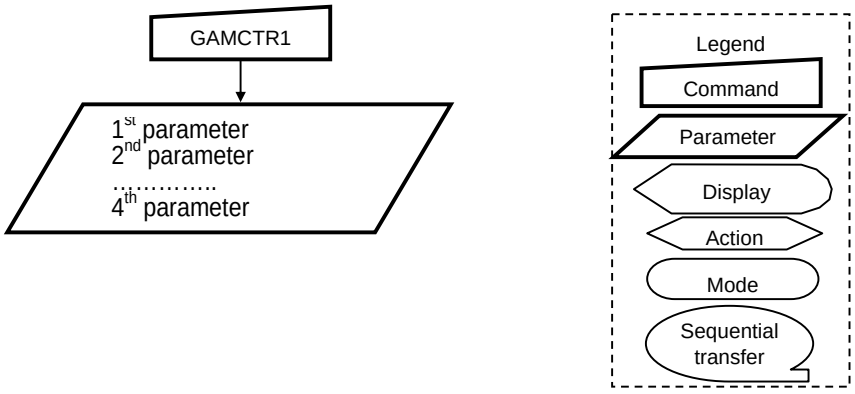
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	GS10[2:0] ~ GS17[2:0]
Power On Sequence	4/4/4/4/4/4/4/4
S/W Reset	4/4/4/4/4/4/4/4
H/W Reset	4/4/4/4/4/4/4/4

Flow Chart



7.1.47 GAMCTR2: Set Gamma Correction Characteristics (C9h)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GAMCTR2	0	↑	1	-	1	1	0	0	1	0	0	1	(C9h)
1st parameter	1	↑	1	-			GS202	GS201	GS200	GS212	GS211	GS210	
2nd parameter	1	↑	1	-			GS222	GS221	GS220	GS232	GS231	GS230	
3rd parameter	1	↑	1	-			GS242	GS241	GS240	GS252	GS251	GS250	
4th parameter	1	↑	1	-			GS262	GS261	GS260	GS272	GS271	GS270	

Description

Set the gray scale voltage to adjust the gamma characteristics of the TFT panel.
It apply to gamma curve selection by instruction code 26h.
1st to 4th parameter: Gamma curve2 adjustment register

Restriction

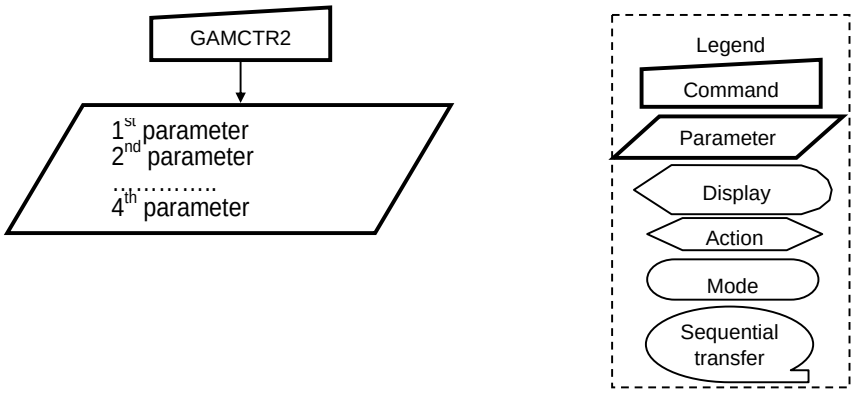
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	GS20[2:0] ~ GS27[2:0]
Power On Sequence	4/4/4/4/4/4/4/4
S/W Reset	4/4/4/4/4/4/4/4
H/W Reset	4/4/4/4/4/4/4/4

Flow Chart



7.1.48 GAMCTR3: Set Gamma Correction Characteristics (CAh)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GAMCTR3	0	↑	1	-	1	1	0	0	1	0	1	0	(CAh)
1st parameter	1	↑	1	-			GS302	GS301	GS300	GS312	GS311	GS310	
2nd parameter	1	↑	1	-			GS322	GS321	GS320	GS332	GS331	GS330	
3rd parameter	1	↑	1	-			GS342	GS341	GS340	GS352	GS351	GS350	
4th parameter	1	↑	1	-			GS362	GS361	GS360	GS372	GS371	GS370	

Description

Set the gray scale voltage to adjust the gamma characteristics of the TFT panel.
It apply to gamma curve selection by instruction code 26h.
1st to 4th parameter: Gamma curve3 adjustment register

Restriction

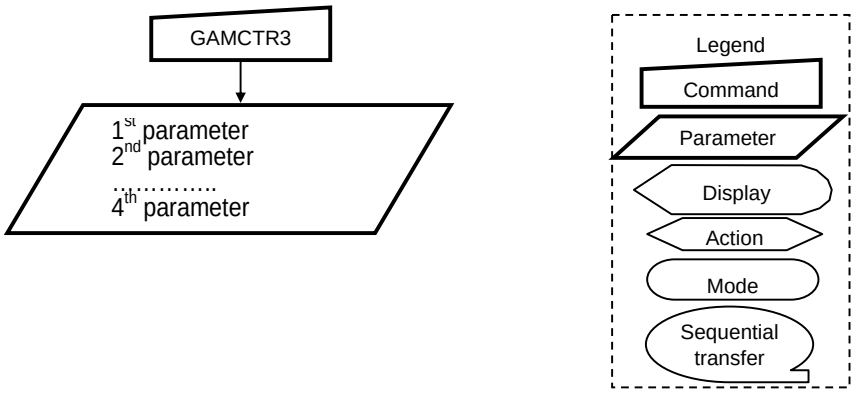
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	GS30[2:0] ~ GS37[2:0]
Power On Sequence	4/4/4/4/4/4/4/4
S/W Reset	4/4/4/4/4/4/4/4
H/W Reset	4/4/4/4/4/4/4/4

Flow Chart



7.1.49 GAMCTR4: Set Gamma Correction Characteristics (CBh)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GAMCTR4	0	↑	1	-	1	1	0	0	1	0	1	1	(CBh)
1st parameter	1	↑	1	-			GS402	GS401	GS400	GS412	GS411	GS410	
2nd parameter	1	↑	1	-			GS422	GS421	GS420	GS432	GS431	GS430	
3rd parameter	1	↑	1	-			GS442	GS441	GS440	GS452	GS451	GS450	
4th parameter	1	↑	1	-			GS462	GS461	GS460	GS472	GS471	GS470	

Description

Set the gray scale voltage to adjust the gamma characteristics of the TFT panel.
It apply to gamma curve selection by instruction code 26h.
1st to 4th parameter: Gamma curve4 adjustment register

Restriction

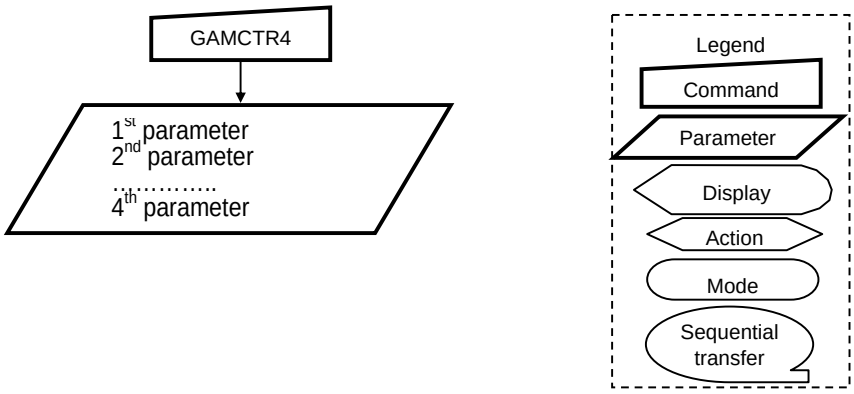
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	GS40[2:0] ~ GS47[2:0]
Power On Sequence	4/4/4/4/4/4/4/4
S/W Reset	4/4/4/4/4/4/4/4
H/W Reset	4/4/4/4/4/4/4/4

Flow Chart



7.1.50 EPPGMDB: Write ID2, VCOM Offset Value

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
EPPGMDB	0	↑	1	-	1	1	0	1	0	0	0	0	(D0h)
Parameter	1	↑	**1**	-	-	-	-	-	-	VCOF82	VCOF81	VCOF80	-
Parameter	1	↑	**1**	-	-	-	VCOF5	VCOF4	VCOF3	VCOF2	VCOF1	VCOF0	-
Parameter	1	↑	**1**	-	ID26	ID25	ID24	ID23	ID22	ID21	ID20	db_sel	-

NOTE: "-" Don't care

Description

This command is used to write the values of ID2 , VCOM and VCOM8 to internal register.

These value is programmed into EEPROM by command "EPPGM(D2h).

VCOM Offset Control

1st Parameter: VCOM offset control(8color)

VCOF8 [2:0]	VCLC (Internal)	VCHC (Internal)
0(default)	VCLC	VCHC
1	VCLC-3	VCHC-3
2	VCLC-2	VCHC-2
3	VCLC-1	VCHC-1
4	VCLC	VCHC
5	VCLC+1	VCHC+1
6	VCLC+2	VCHC+1
7	VCLC+3	VCHC+3

2nd Parameter: VCOM offset control

VCOF [5:0]	VCLC (Internal)	VCHC (Internal)
0(default)	VCLC	VCHC
1	VCLC-31	VCHC-31
:	:	:
31	VCLC-1	VCHC-1
32	VCLC	VCHC
33	VCLC+1	VCHC+1
:	:	:
63	VCLC+31	VCHC+31

NOTE: If VCLC (Internal) or VCHC (Internal) is less than 0, it becomes 0.
If VCLC (Internal) or VCHC (Internal) is larger than 31, it becomes 31.
The VCOF[5:0] is stored in EEPROM to fit contrast.

3rd Parameter: ID2[6:0]

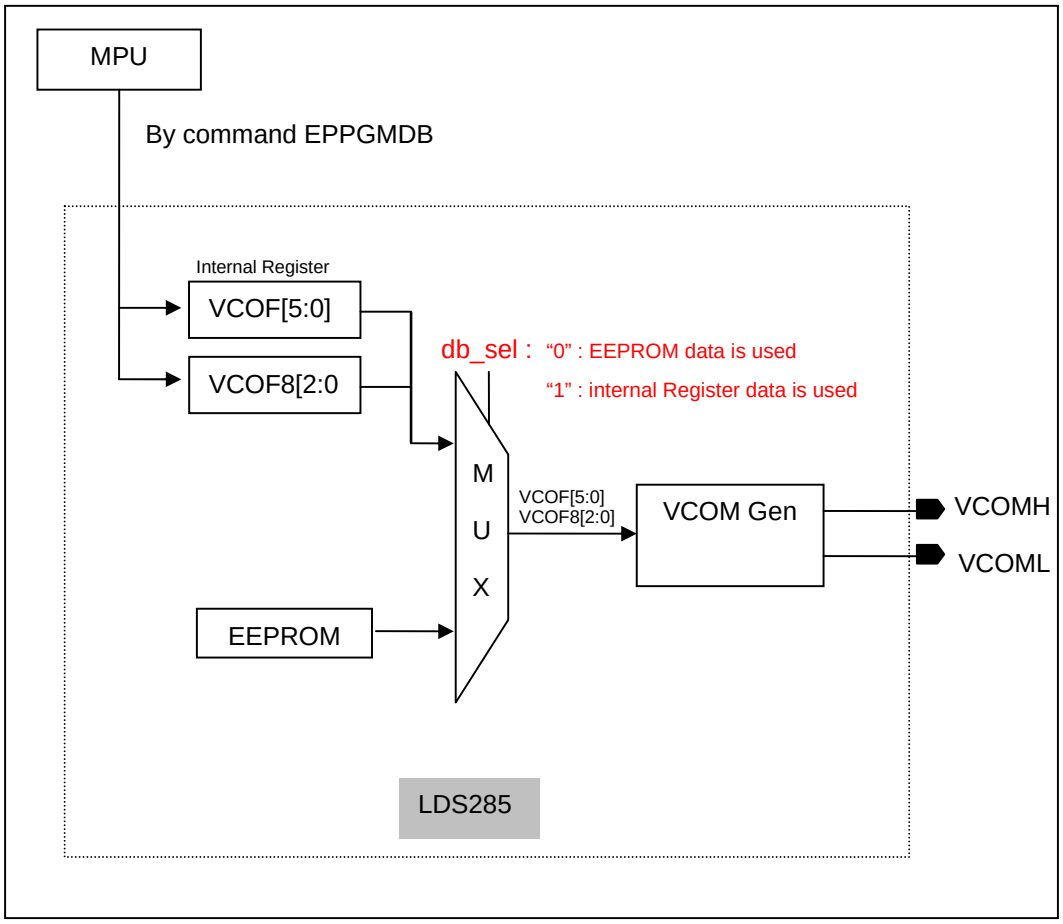
Write 7-bit LCD module/driver version ID to save it to EEPROM.

3rd Parameter: db_sel

"0" = Using the EEPROM data for making VCOMH & VCOML.

"1" = Using the internal register values written by EPPGMDB for VCOMH & VCOML.

The following drawing shows how to use "db_sel" to fix the VCOF and the VCOF8.



The user shoule fix VCOF and VCOF8 to adjust the VCOMH and VCOML output voltage level.

The user can use "db_sel" to find out which value is suitable for VCOMH and VCOML.

If the user sets "db_sel" to "1", then LDS285 uses the internal register value to make the proper VCOMH and VCOML output voltage instead of the value read from EEPROM.

That means that the user can control and monitor the VCOMH and VCOML output voltage by changing the parameter of the command "EPPGMDB" and find out the proper value of the 1st and the 2nd parameter of the command "EEPGMDB" before programming the VCOF[5:0] and VCOF8[2:0] into EEPROM.

Restriction

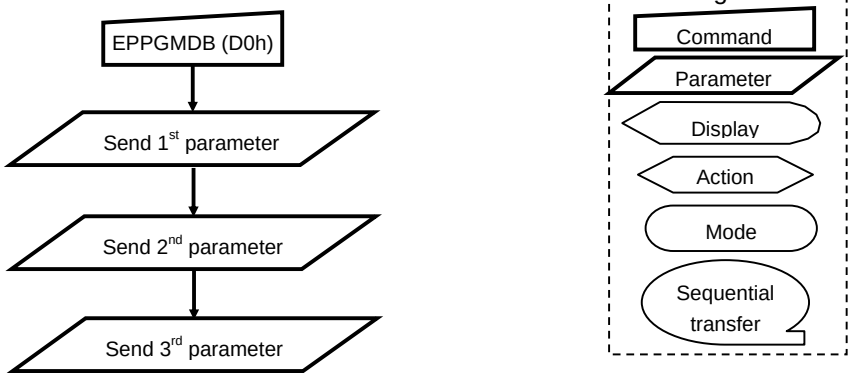
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value			
	VCOF8[2:0]	VCOF[5:0]	ID2	db_sel
Power On Sequence	0	0	Not Fixed (80 ~ FFh)	0
S/W Reset	0	0	Not Fixed (80 ~ FFh)	0
H/W Reset	0	0	Not Fixed (80 ~ FFh)	0

Flow Chart



7.1.51 EPERASE: EPROM Erase (D1h)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
EPERASE	0	↑	1	-	1	1	0	1	0	0	0	1	(D1h)
Parameter	No Parameter												

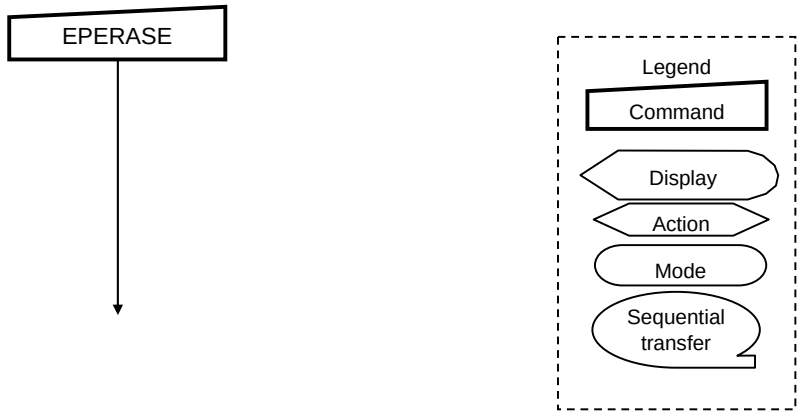
Description	EEPROM data erase.
Restriction	It will be necessary to wait more than 150msec after EEPROM erase start . Refer to 7.3.3&7.3.4 EEPROM access flow. EPERASE should be excuted in Sleep-in mode.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	No
Normal Mode On, Idle Mode On, Sleep Out	No
Partial Mode On, Idle Mode Off, Sleep Out	No
Partial Mode On, Idle Mode On, Sleep Out	No
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Disable
S/W Reset	Disable
H/W Reset	Disable

Flow Chart



7.1.52 EPPROG: EPROM Program (D2h)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
EPPROG	0	↑	1	-	1	1	0	1	0	0	1	0	(D2h)
Parameter	No Parameter												

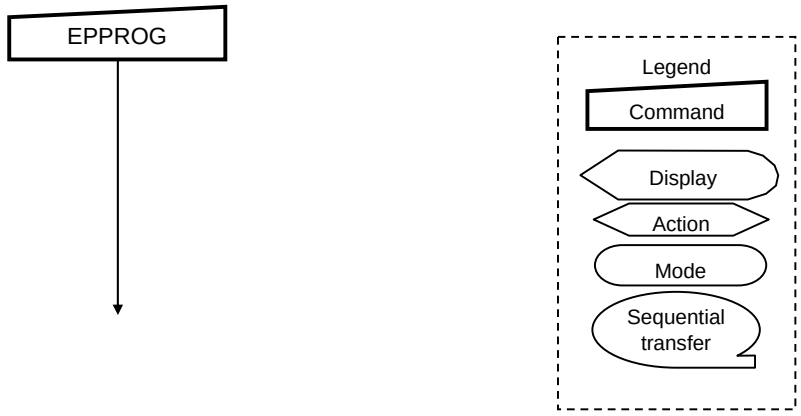
Description	EEPROM data program.
Restriction	It will be necessary to wait more than 100msec after EEPROM program start . Refer to 6.3.3&6.3.4 EEPROM access flow. EEPROG should be excuted in Sleep-in mode.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	No
Normal Mode On, Idle Mode On, Sleep Out	No
Partial Mode On, Idle Mode Off, Sleep Out	No
Partial Mode On, Idle Mode On, Sleep Out	No
Sleep In	Yes

Default

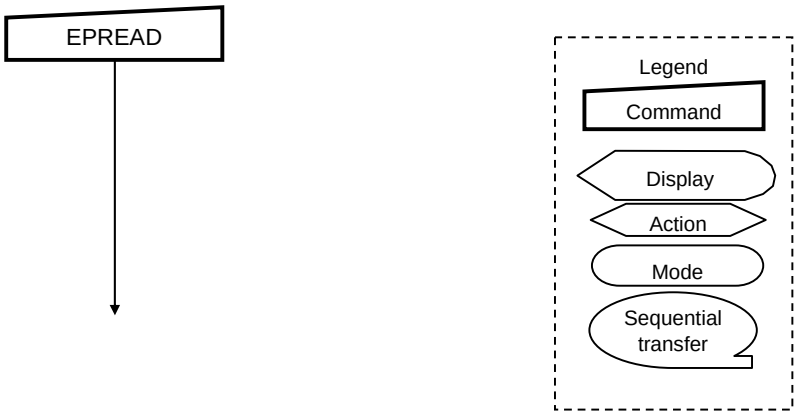
Status	Default Value
Power On Sequence	Disable
S/W Reset	Disable
H/W Reset	Disable

Flow Chart



7.1.53 EPRDVRF: EPROM Read Verify (D3h)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
EPRDVRF	0	↑	1	-	1	1	0	1	0	0	1	1	(D3h)
Parameter	1	↑	1	-	-	-	-	-	READ	PGM VF	ERVF	0	

Description	.When READ =1, PGMVF =0 & ERVF =0 , then EEPROM data are normally read to Internal register. .When READ =0, PGMVF =1 & ERVF =0, then the read verification for the programmed data will be executed by using the internal reference voltage(VDD1). This mode is to read the programmed value from EEPROM under the more serious condition than normal read mode. .When READ =0, PGMVF =0 & ERVF = 1, then the read verification for the erased data verification will be executed by using the external reference voltage.(ME_CMP). This mode is to read the erased value from EEPROM under the more serious condition than normal read mode.
Restriction	It will be necessary to wait more than 100usec after EEPROM read start . Refer to 7.3.3&6.3.4 EEPROM access flow.
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes
Default	Status / Default Value Power On Sequence: Disable S/W Reset: Disable H/W Reset: Disable
Flow Chart	

7.1.54 RDVCOF: VCOM offset registers bits Read Back (D9h)

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDVCOF	0	↑	1	-	1	1	0	1	1	0	0	1	(D9h)
Dummy Read	1	**1**	↑	-	-	-	-	-	-	-	-	-	Dummy
2'nd Parameter	1	**1**	↑	-	-	-	RVCOF5	RVCOF4	RVCOF3	RVCOF2	RVCOF1	RVCOF0	
3'rd Parameter	1	**1**	↑	-	-	-	-	-	-	RVCOF82	RVCOF81	RVCOF80	

Description

This read 6-bit VCOM register offset value and additional 4-bit VCOM offset value. (**refer to 6.1.60**)
The 1st parameter is dummy data
The 2nd parameter RVCOF[5:0] : range 0d ~ 63d
The 2nd parameter RVCOF8[2:0]: range 0 ~ 7.

Restriction

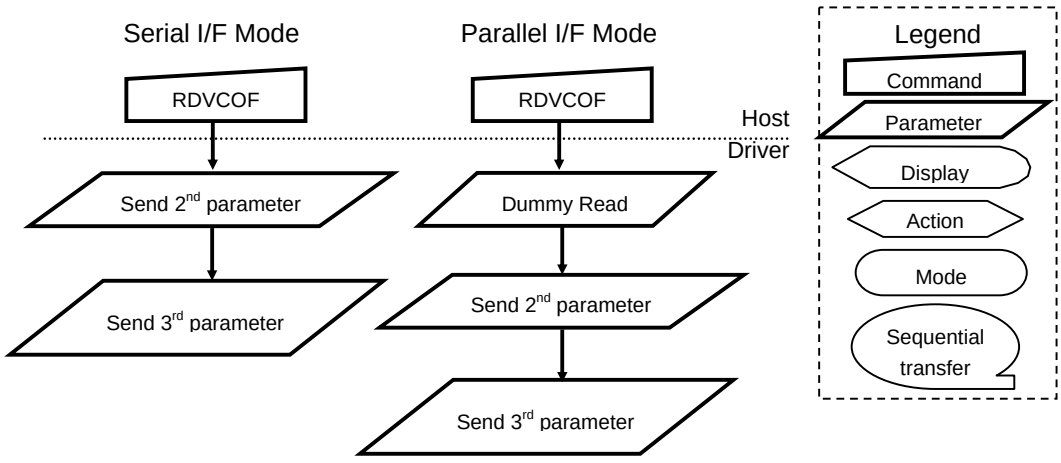
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	RVCOF[5:0], RVCOF8[2:0]
Power On Sequence	-
S/W Reset	-
H/W Reset	-

Flow Chart



7.1.55 LEDCTRL: Write the configuration for LED driver

Inst / Para	DC	WRB	RDB	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
EPPGMDB	0	↑	1	-	1	1	1	0	1	1	1	1	(EFh)
Parameter	1	↑	**1**	-	-	-	-	-	-	-	-	TYPE	-
Parameter	1	↑	**1**	-	0	ADR2	ADR1	ADR0	DB3	DB2	DB1	DB0	-
Parameter	1	↑	**1**	-	0	PER3	PER2	PER1	PER0	0	0	0	-

NOTE: "-" Don't care

Description

This command is used to configure the LED driver control

1st Parameter: TYPE

"0" : When LDS285 controls LED Driver type with pwm pulse contol.

"1" : When LDS285 controls LED Driver LDS8816 with 1-wire digital interface.

2nd Parameter: ADR[2:0], DB[3:0]

When TYPE = 1, LDS285 write DB[3:0] to ADDR[2:0] register in LDS8861.

(Please refer to Section 6.4 and the specification for LDS8861)

3rd Parameter: PER[3:0]

When TYPE = 0, PER[3:0] decide the period of PWM pulse which is sent through LCD_CNT.

(Please refer to Section 6.4)

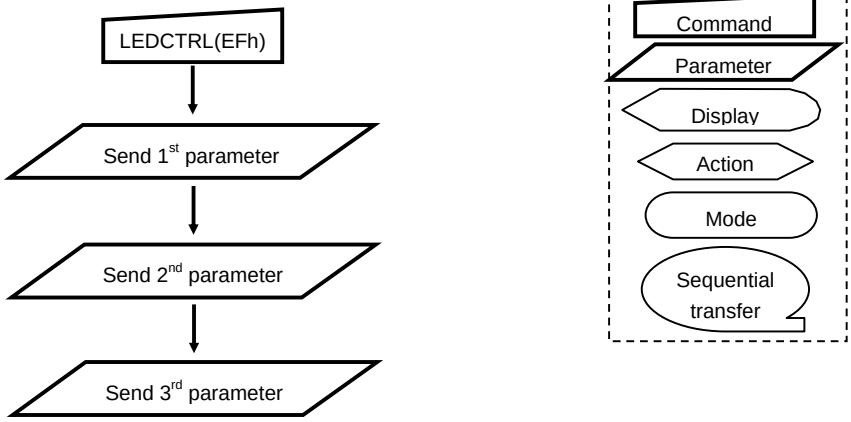
Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value			
	TYPE	ADR[2:0]	DB[3:0]	PER[3:0]
Power On Sequence	0	0	Eh	0
S/W Reset	0	0	Eh	0
H/W Reset	0	0	Eh	0

Flow Chart	

LEDCTRL(EFh)
Send 1st parameter
Send 2nd parameter
Send 3rd parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

7.2 RESET TABLE (DEFAULT VALUE) (TBD)

Item	After Power On	After Hardware Reset	After Software Reset
DDRAM	Random	No Change	No Change
Sleep In/Out	In	In	In
Display On/Off	Off	Off	Off
Display mode (normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address (XS)	0000h	0000h	0000h
Column: End Address (XE)	00EFh	00EFh	007Fh (239d) (when MV=0) 009Fh (319d) (when MV=1)
Row: Start Address (YS)	0000h	0000h	0000h
Row: End Address (YE)	013Fh	013FFh	009Fh (319d) (when MV=0) 007Fh (239d) (when MV=1)
Brightness Control Value *3)	FFh	FFh	FFh
Gamma setting	GC0	GC0	GC0
Partial: Start Address (PSL)	0000h	0000h	0000h
Partial: End Address (PEL)	013Fh	013Fh	013Fh
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode *4)	0 (Mode1)	0 (Mode1)	0 (Mode1)
Memory Data Access Control (MY/MX/MV/ML/RGB)	0/0/0/0/0	0/0/0/0/0	No Change
Interface Pixel Color Format	7 (24-Bit/Pixel)	7 (24-Bit/Pixel)	No Change
RDDPM	08h	08h	08h
RDDMADCTR	00h	00h	No Change
RDDCOLMOD	7 (24-Bit/Pixel)	7 (24-Bit/Pixel)	No Change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
RDDSDR	00h	00h	00h
ID1	TBD	TBD	TBD
ID2	TBD	TBD	TBD
ID3	TBD	TBD	TBD

Notes:

1. There will be no abnormal visible effects on the display when S/W or H/W Reset is applied.

2. Powered-On Reset finishes within 10µs after both VDD1_IO, VDD1 & VDD2 are applied.

3. Brightness conrol value is related with the command "WRDISBV(51h).

4. TE Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

7.3 INSTRUCTION SETUP FLOW

7.3.1 Initializing with the Built-in Power Supply Circuits (TBD)

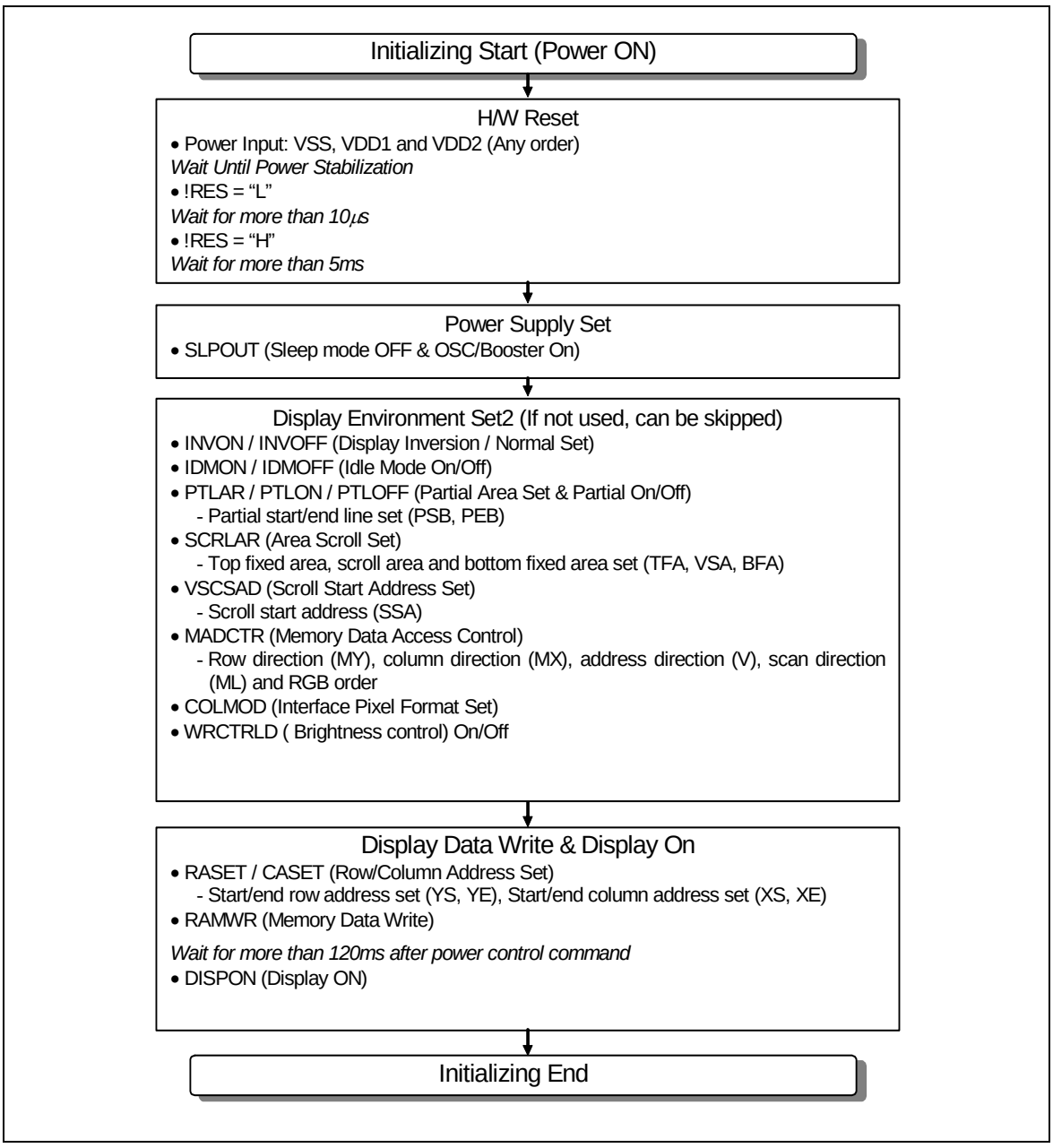


Fig. 7.3.1 Initializing with the built-in power supply circuits

The initializing sequence does not have any effect on the display. The display is in its normal background color during the initialization.

7.3.2 Power OFF Sequence (TBD)

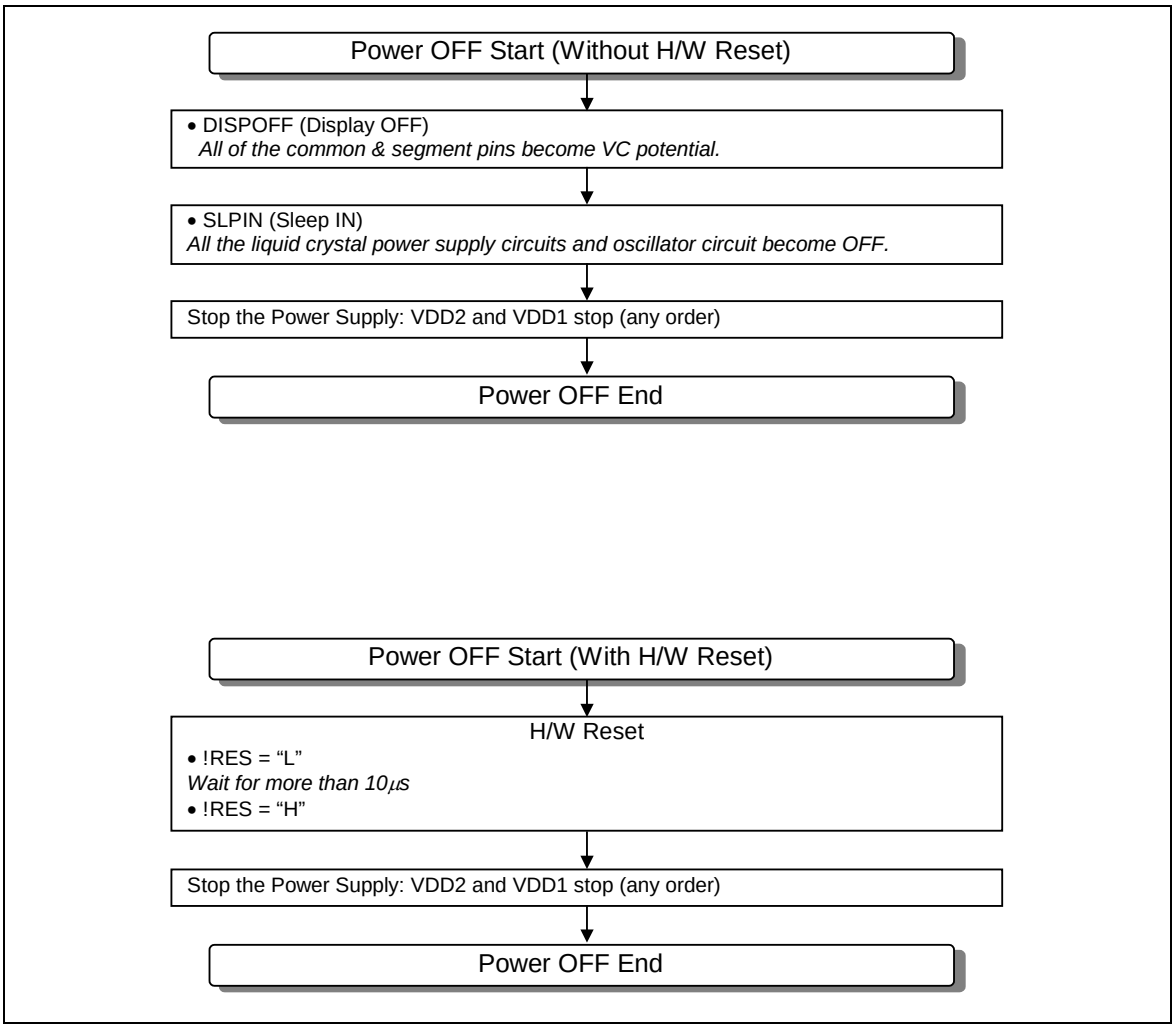
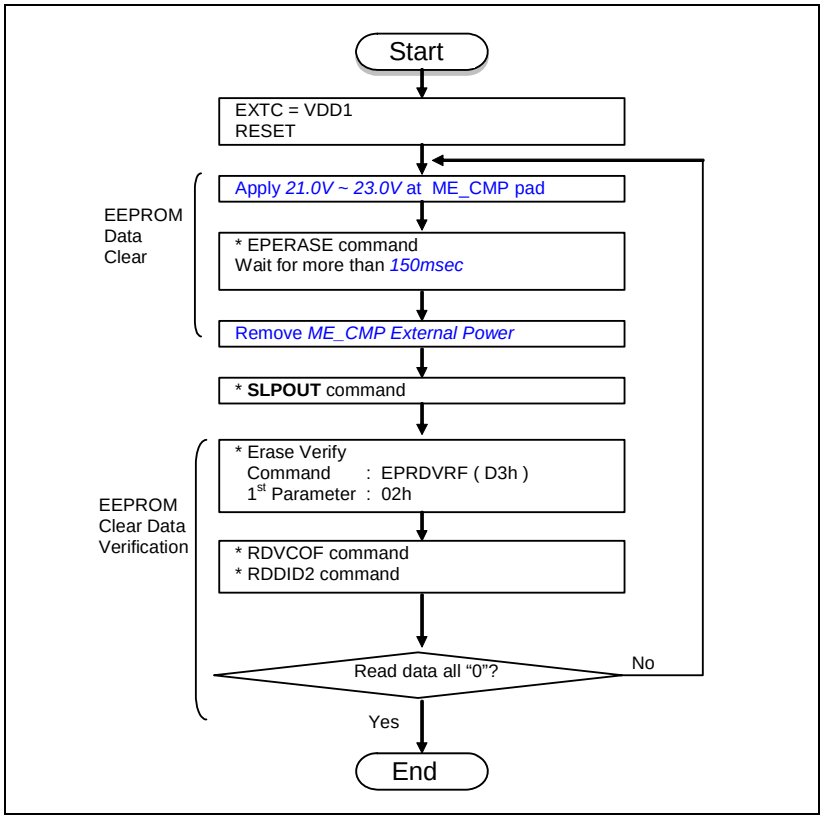
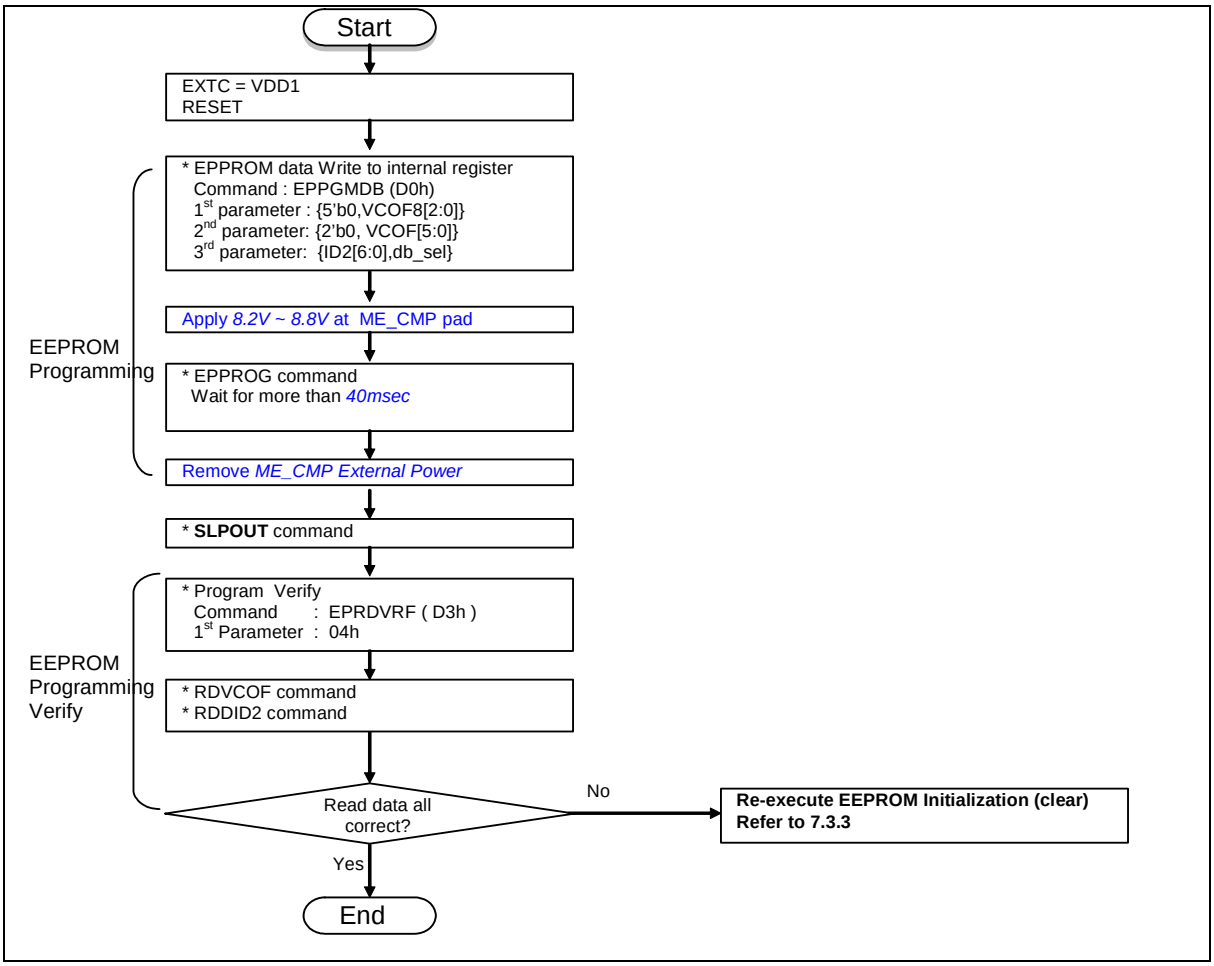


Fig. 7.3.2 Power OFF sequence

7.3.3 EEPROM Access Sequence for Initialization (Data Clear)



7.3.4 EEPROM Access Sequence for program (Data write) (TBD)



8 SPECIFICATIONS

8.1 ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

Item	Symbol	Value	Unit
Supply voltage (1)	V_{DD1}	- 0.3 ~ + 2.0	V
Supply voltage (2)	V_{DD2}	- 0.3 ~ + 3.6	V
Drive Supply Voltage	VGH – VGL	- 0.3 ~ + 28.0	V
Logic input voltage range	V_{IN}	- 0.3 ~ V_{DD1} + 0.3	V
Logic output voltage range	V_O	- 0.3 ~ V_{DD1} + 0.3	V
Operating temperature range	T_{OPR}	- 30 ~ + 75	°C
Storage temperature range	T_{STG}	- 55 ~ + 125	°C

NOTE: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings

8.2 ESD PROTECTION LEVEL

Table 8.2.1 ESD models.

Model	Test Condition	Protection Level	Unit
Human Body Model	C = 100 pF, R = 1.5 kΩ	> 2000	V
Machine Model	C = 200 pF, R = 0.0 Ω	> 200	V

8.3 LATCH-UP PROTECTION LEVEL

The device will not latch up at trigger current levels less than ±100 mA.

8.4 LIGHT SENSITIVITY

The operation of the IC will not be materially altered by incident light.

8.5 MAXIMUM SERIES RESISTANCE

The driver will operate in 'Chip on Glass' applications with series resistances (due to ITO track resistance). Voltages are specified at module I/O assuming maximum values as in ***Table 7.5.1.***

Table 8.5.1 Maximum series resistance on module.

Name	Type	Maximum Series Resistance	Unit
VDD1	Power supply	10	Ω
VDD2	Power supply	10	Ω
VSS	Power supply	10	Ω
OSC	Input	100	Ω
SRGB, SINV, SMX, SMY, VGLX4, FRM, EXTC, PSEL TGS, TEST2, TEST3	Input	100	Ω
P68, BS2, BS1, BS0	Input	100	Ω
RESB	Input	100	Ω
CSB (!SCE)	Input	100	Ω
DC (SCL)	Input	100	Ω
WRB	Input	100	Ω
RDB	Input	100	Ω
TE, VSYNCO	Output	100	Ω
D15 to D0	Input / Output	100	Ω
D23 to D16, VDO DCK, ENABLE, VSYNC, HSYNC	Input	100	Ω
VGH	Capacitor connection	10	Ω
VGL	Capacitor connection	10	Ω
VCOMH,VCOML	Capacitor connection	10	Ω
VR	Capacitor connection	10	Ω
VS	Capacitor connection	10	Ω
VREG_DC	Capacitor connection	5	Ω
VDC1	Booster1 Power Supply	5	Ω
C1P, C1M	Capacitor connection	10	Ω
C2P, C2M	Capacitor connection	10	Ω
C3P, C3M	Capacitor connection	10	Ω
C4P, C4M	Capacitor connection	10	Ω
C5P, C5M	Capacitor connection	10	Ω
C6P, C6M	Capacitor connection	10	Ω

8.6 DC CHARACTERISTICS

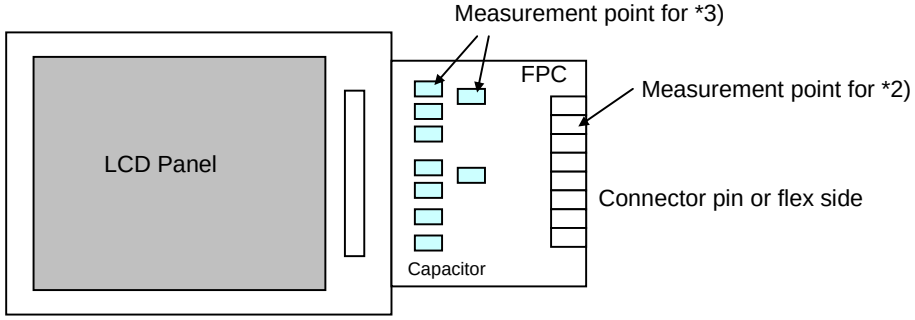
8.6.1 Basic Characteristics

(V_{SS}=0V, V_{DD1}=1.65V to 1.95V, V_{DD2}=2.3V to 2.9V,Ta = -30 to 70°C)

Parameter	Symbol	Conditions	Related Pins	MIN	TYP	MAX	Unit
Power & Operating Voltages							
I/O interface Voltage	V_{DD1IO}	-	*2) VDD1_IO,VDD1	1.65	1.8/2.75	3.3	V
Logic Operating voltage	V_{DD1}	PSEL=0	*2) VDD1	1.65	1.8	1.95	
Analog Operating voltage	V_{DD2}	-	*2) VDD2	2.3	2.75	3.3	
Gate Drive High Voltage1	VGH		*3) VGH	9	16.0	20.0	
Gate Drive Low Voltage1	VGL		*3) VGL	-15	-12.0	-6.0	
Drive Supply Voltage1	VGH-VGL		*3) VGH, VGL	15	28.0	30	
Input / Output							
High level input voltage	V_{IH}		*1) *2)	0.7V_{DD1}	-	V_{DD1}	V
Low level input voltage	V_{IL}	-	*1) *2)	V_{SS}	-	0.3V_{DD1}	
High level output voltage	V_{OH}	I_{OH} = -1.0mA	*2) D17 to D0, TE, TEST1	0.8V_{DD1}	-	V_{DD1}	
Low level output voltage	V_{OL}	I_{OL} = +1.0mA		V_{SS}	-	0.2V_{DD1}	
Input leakage current	I_{IL}	V_{IN} = V_{DD1} or V_{SS}	*1) *2)	-1.0	-	+1.0	μA
Oscillator frequency	f_{OSC}	-	-	450	500	550	kHz
Booster							
AVDD boost voltage1	AVDD1	IAVDD=1mA, dual-type, X2	*3) AVDD	1.9*VDD2	-	2.0*VDD2	V
AVDD boost voltage2	AVDD2	IAVDD=1mA, single-type, X2	*3) AVDD	1.8*VDD2	-	2.0*VDD	
AVDD boost voltage3	AVDD3	IAVDD=1mA, single-type, X3	*3) AVDD	2.7*VREG_DC		3.0*VREG_DC	
VGH boost voltage	VGH	I_{GH}=300uA, 4*VR	*3) VGH	3.6*VR	-	4.0*VR	
VGL boost voltage	VGL	I_{GL}=-300uA, -3*VR	*3) VGL	-2*VR	-	-1.8*VR	
VCL boost voltage	VCL	I_{CL}=-300uA, -1*V_{DD2}	*3) VCL	-1*VDD2	-	-0.9*VDD2	
VS output voltage	VS	Default, No load	*3) VS	3.00	4.2	6.00	
VR output voltage	VR	Default, No load	*3) VR	3.00	4.00	5.00	

*NOTE: *1) SRGB, SINV, SMX, SMY, DCK, ENABLE, VSYNC, HSYNC, OSC, P68, ,BS2, BS1, BS0, CSB, RESB, DC, WRB, RDB, D23 to D0 pins*

**2) *3) When the measurement are performed with LCD module, Measurement Points are like below*



Parameter	Symbol	Conditions	Related Pins	MIN	TYP	MAX	Unit
VCOM Generator							
VCOM amplitude	VCOMA	No load	VCOMH VCOML				V
VCOM output high resistance	R_{VCOMH}	VCOM output = High I_{VCOM} = 1mA	VCOM	-	200	TBD	Ω
VCOM output low resistance	R_{VCOML}	VCOM output = Low I_{VCOM} = 1mA	VCOM	-	200	TBD	
Source Driver							
Gray scale resistance	Rgray	Rap~Rjp, Ran~Rjn, R0~R62 of gray voltage generator	S1 to S720	0.7*Rx	Rx	1.3*Rx	Ω
*1) *2) Drive output current	I_{VOSH}	VS=3.75V, VSO=V0 at positive, VOUT=V0-2V	S1 to S720	-	-200	-100	μA
	I_{VOSL}	VS=3.75V, VSO=V0 at negative, VOUT=V0-2V	S1 to S720	100	200	-	μA
Output voltage deviation	D_{VOS}	VSS1+1.0 ~ VS-1.0	S1 to S720	-	±10	±20	mV
		VSS1+0.1V ~ VSS1+1.0 VS-1.0 ~ VS-0.1V	S1 to S720	-	±30	±50	mV
Output voltage range	V_{OS}	-	S1 to S720	0.1	-	VS-0.1	V
Gate Driver							
*3) Output ON resistance	R_{ONG}	Ta = 25°C	G1 to G320	-	2	3	kΩ

NOTE:

1) V_{SO} is the output voltage of source output pins S1 to S720.

2) V_{OUT} is the applied voltage to source output pins S1 to S720

3) Resistance value when -0.1[mA] is applied during the ON status of the gate output pin G1 to G320.

R_{ON} [kΩ] = ΔV [V] / 0.1[mA] (ΔV: Voltage change when –0.1[mA] is applied in the on status.)

8.6.2 Current Consumption

Host I/F	Mode of operation	Frame Frequency	Inversion Mode	Image	Memory Data Access Control (MY:MX:MV)	Current consumption			
						Typical		Worst case	
						VDD2 (mA)	VDD1 (mA)	VDD2 (mA)	VDD1 (mA)
Host interface NOT active	- Normal Mode On - Partial Mode Off - Idle Mode Off - Sleep Out Mode	60Hz	TBD	Note 1	X;X;X	TBD	TBD	TBD	TBD
			TBD	Note 2	X;X;X	TBD	TBD	TBD	TBD
			TBD	Note 3	X;X;X	TBD	TBD	TBD	TBD
			TBD	Note 4	X;X;X	TBD	TBD	TBD	TBD
			TBD	Note 5	X;X;X	TBD	TBD	TBD	TBD
	- Normal Mode On - Partial Mode Off - Idle Mode On - Sleep Out Mode	60Hz	TBD	Note 5	X;X;X	TBD	TBD	TBD	TBD
	- Normal Mode Off - Partial Mode On (32 lines) - Idle Mode Off - Sleep Out Mode	60Hz	TBD	Grey Levels	X;X;X	TBD	TBD	TBD	TBD
	- Normal Mode Off - Partial Mode On (32 lines) - Idle Mode On - Sleep Out Mode	60Hz	TBD	Note 6	X;X;X	TBD	TBD	TBD	TBD
			TBD	Note 7	X;X;X	TBD	TBD	TBD	TBD
	- Sleep In Mode	N/A	N/A	N/A	X;X;X	0.002		0.010	
Host interface active	- Normal Mode On - Partial Mode Off - Idle Mode Off - Sleep Out Mode	60Hz	TBD	262k Colors NOTE 8 CPU Access @ 15fps	0;0;0	TBD	TBD	TBD	TBD
					0;0;1	TBD	TBD	TBD	TBD
					0;1;0	TBD	TBD	TBD	TBD
					0;1;1	TBD	TBD	TBD	TBD
					1;0;0	TBD	TBD	TBD	TBD
					1;0;1	TBD	TBD	TBD	TBD
					1;1;0	TBD	TBD	TBD	TBD
					1;1;1	TBD	TBD	TBD	TBD
				262k Colors NOTE 8 CPU Access @ 25fps	0;0;0	TBD	TBD	TBD	TBD
					0;0;1	TBD	TBD	TBD	TBD
					0;1;0	TBD	TBD	TBD	TBD
					0;1;1	TBD	TBD	TBD	TBD
					1;0;0	TBD	TBD	TBD	TBD
					1;0;1	TBD	TBD	TBD	TBD
					1;1;0	TBD	TBD	TBD	TBD
					1;1;1	TBD	TBD	TBD	TBD

NOTE: X Do not care

1. *All pixels black*
2. *Checker board one by one*
3. *Checker board 4 by 4*
4. *Grey-scale from top to bottom*
5. *20% Black, 80%White*
6. *Black & White Checker board 8 by 8.*
7. *Absolute Worst Case Patterns: Defined by Display Supplier*
8. *Absolute Worst Case Patterns and Sequences: Defined by Display Supplier*
9. *Absolute worst case VDD current is less than TBD mA in the case of CPU access is inactive, Normal Mode On, Partial Mode Off, Idle Mode Off, Sleep Out mode.*
10. *Absolute worst case VDD1_IOI current is less than TBD mA in the case of CPU access is inactive, Normal Mode On, Partial Mode Off, Idle Mode Off, Sleep Out mode.*
11. *Inrush currents are not included in current consumption values*

Typical Case:
T_A = 25ºC
VDD2 = 2.75V
VDD1 = 1.8V

Worst Case:
T_A = -30 to70ºC
VDD2 = 2.5V to 2.9V
VDD1 = 1.65V to 1.95V
Includes Process Variance.

8.7 AC CHARACTERISTICS(TBD)

8.7.1 Parallel Interface Characteristics (8080-series MPU)

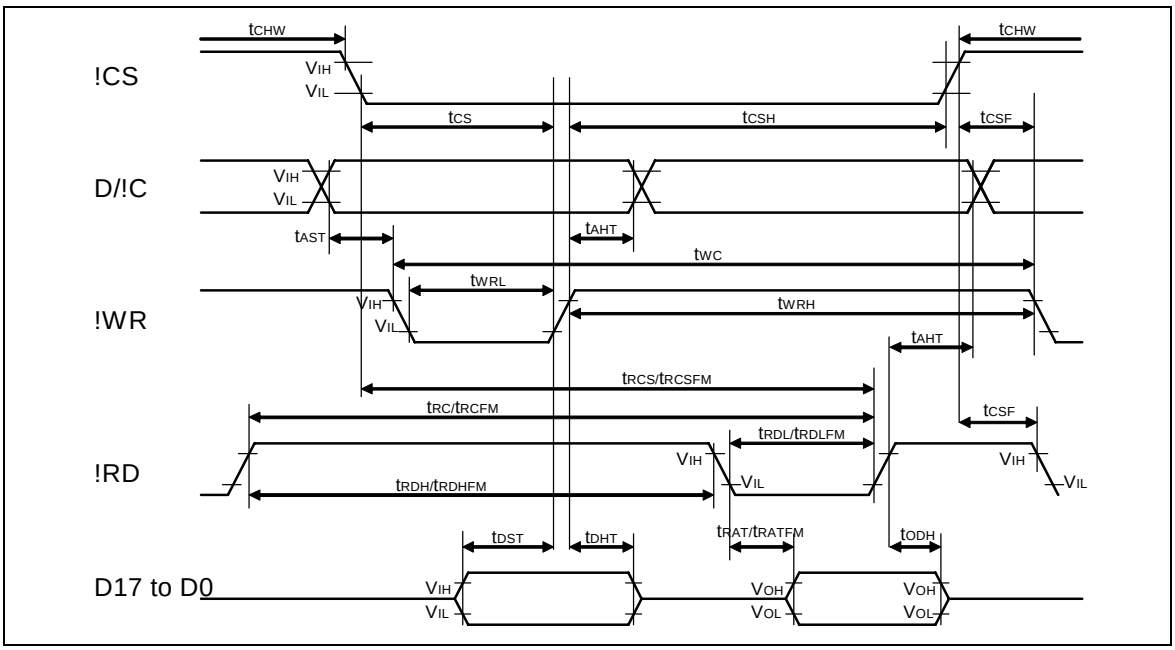


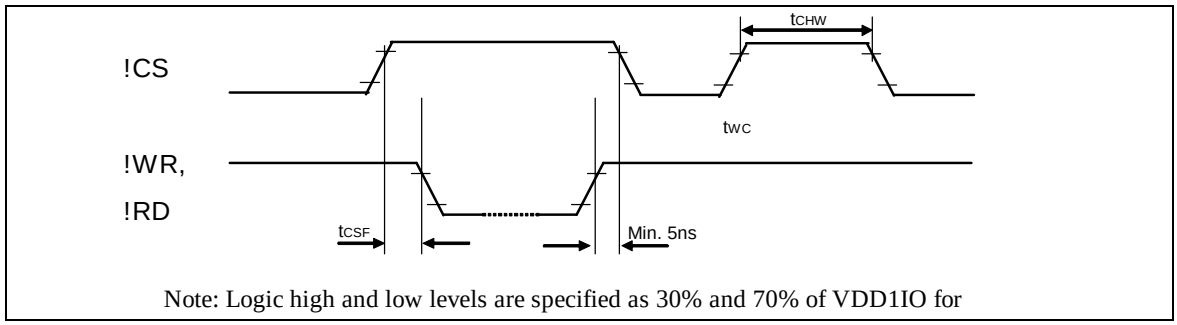
Fig. 8.7.1 Parallel Interface characteristics (8080-series MPU)

(V_{SS}=0V, V_{DD1}=1.65V to 1.95V, V_{DD2}=2.5V to 2.9V,Ta = -30 to 75°C

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DC	t_{AST} t_{AHT}	Address setup time Address hold time (Write/Read)	10 10	- -	ns	-
CSB	t_{CHW} t_{CS} t_{RCS} t_{RCSFM} t_{CSF} t_{CSH}	Chip select “H” pulse width Chip select setup time (Write) Chip select setup time (Read ID) Chip select setup time (Read FM) Chip select wait time (Write/Read) Chip select hold time	0 35 45 355 10 10	- - - - - -	ns	-
WRB	t_{WC} t_{WRH} t_{WRL}	Write cycle Control pulse “H” duration Control pulse “L” duration	100 35 35	- - -	ns	-
RDB (ID)	t_{RC} t_{RDH} t_{RDL}	Read cycle (ID) Control pulse “H” duration (ID) Control pulse “L” duration (ID)	160 90 45	- - -	ns	When read ID data
RDB (FM)	t_{RCFM} t_{RDHFM} t_{RDLFM}	Read cycle (FM) Control pulse “H” duration (FM) Control pulse “L” duration (FM)	450 90 355	- - -	ns	When read from DDRAM
D17 to D0	t_{DST} t_{DHT} t_{RAT} t_{RATFM} t_{ODH}	Data setup time Data hold time Read access time (ID) Read access time (FM) Output disable time	10 10 - - 20	- - 40 340 80	ns	For maximum C_L=30pF For minimum C_L=8pF

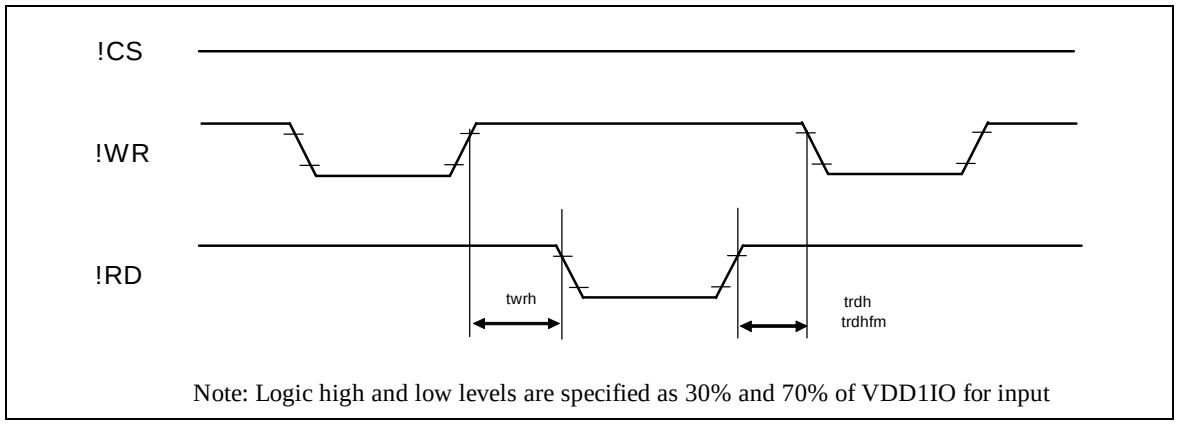
NOTE: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of VDD1 for Input signals. For output, see Section

7.7.6.1



Note: Logic high and low levels are specified as 30% and 70% of VDD1IO for

Fig. 8.7.2 Chip select timing



Note: Logic high and low levels are specified as 30% and 70% of VDD1IO for input

Fig. 8.7.3 Write to read and read to write timing

8.7.2 Parallel Interface Characteristics (6800-series MPU)

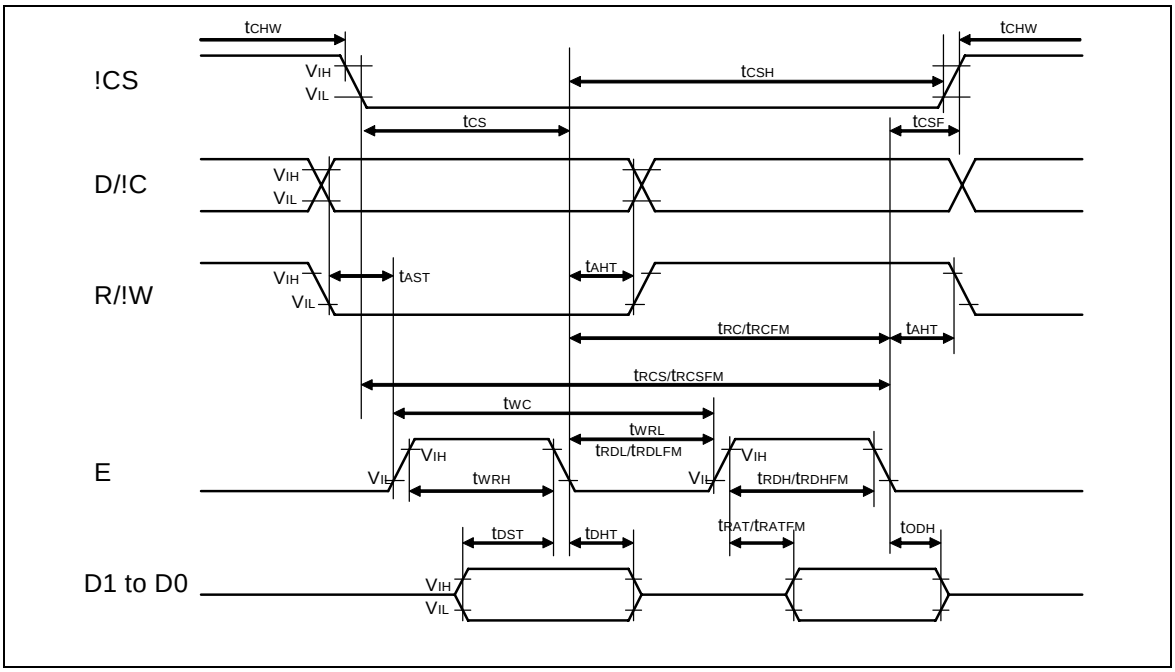


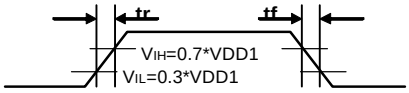
Fig. 8.7.4 Parallel Interface characteristics (6800-series MPU)

(V_{SS}=0V, V_{DD1}=1.65V to 1.95V, V_{DD2}=2.5V to 2.9V,Ta = -30 to 75°C)

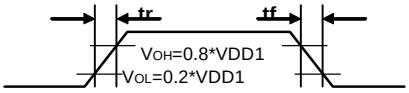
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DC	t_{AST} t_{AHT}	Address setup time Address hold time (Write/Read)	10 10	- -	ns	
CSB	t_{CHW} t_{CS} t_{RCS} t_{RCSFM} t_{CSF} t_{CSH}	Chip select “H” pulse width Chip select setup time (Write) Chip select setup time (Read ID) Chip select setup time (Read FM) Chip select wait time (Write/Read) Chip select hold time	0 35 45 355 10 10	- - - - - -	ns	-
WRB	t_{WC} t_{WRH} t_{WRL}	Write cycle Control pulse “H” duration Control pulse “L” duration	100 35 35	- - -	ns	
RDB (ID)	t_{RC} t_{RDH} t_{RDL}	Read cycle (ID) Control pulse “H” duration (ID) Control pulse “L” duration (ID)	160 90 45	- - -	ns	When read ID data
RDB (FM)	t_{RCFM} t_{RDHFM} t_{RDLFM}	Read cycle (FM) Control pulse “H” duration (FM) Control pulse “L” duration (FM)	450 90 355	- - -	ns	When read from DDRAM
D17 to D0	t_{DST} t_{DHT} t_{RAT} t_{RATFM} t_{ODH}	Data setup time Data hold time Read access time (ID) Read access time (FM) Output disable time	10 10 - - 20	- - 40 340 80	ns	For maximum C_L=30pF For minimum C_L=8pF

NOTE: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of VDD1_IO for Input signals. For output, see Section 7.7.6.1

Input Signal Slope



Output Signal Slope



8.7.3 Serial Interface Characteristics (3-Pin Serial)

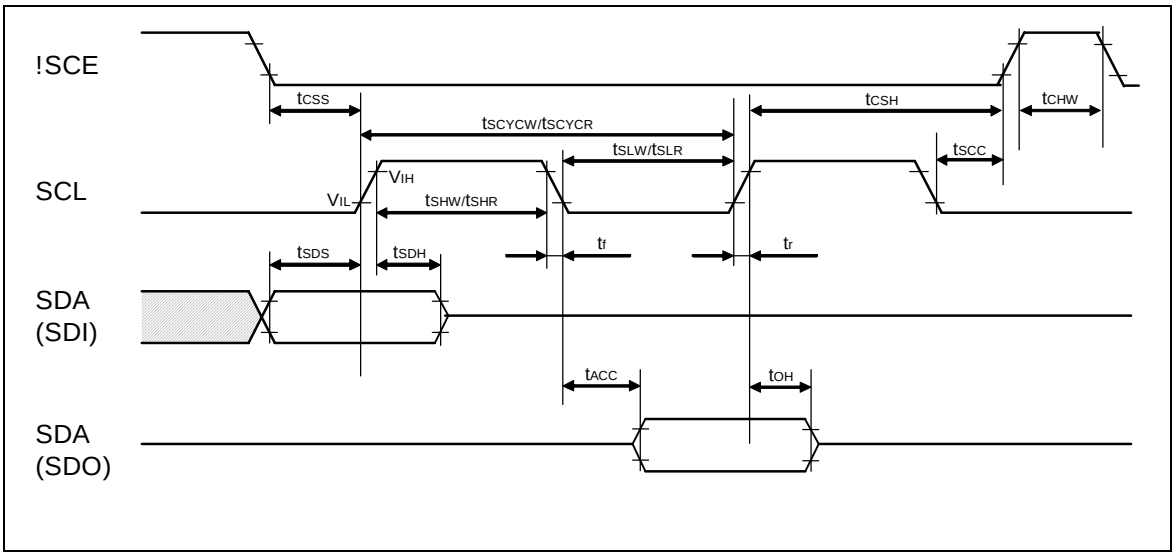


Fig. 8.7.5 3-pin serial interface characteristics

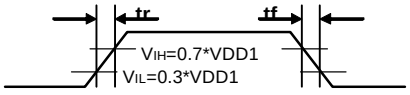
(V_{SS}=0V, V_{DD1}=1.65V to 1.95V, V_{DD2}=2.5V to 2.9V,Ta = -30 to 75°C)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Serial clock cycle (Write) SCL "H" pulse width (Write) SCL "L" pulse width (Write)	t_{SCYCW} t_{SHW} t_{SLW}	SCL	100 35 35		- -	ns
Data setup time (Write) Data hold time (Write)	t_{SDS} t_{SDH}	SDA	30 30		- -	ns
Serial clock cycle (Read) SCL "H" pulse width (Read) SCL "L" pulse width (Read)	t_{SCYCR} t_{SHR} t_{SLR}	SCL	150 60 60		- - -	ns
Access rime	t_{ACC}	SDA For maximum C_L=30pF For minimum C_L=8pF	10		50	ns
Output disable time	t_{OH}	SDA For maximum C_L=30pF For minimum C_L=8pF	15		50	ns
SCL to Chip select	t_{SCC}	!SCE	15			ns
SCEB "H" pulse width	t_{CHW}	!SCE	45			ns
Chip select setup time Chip select hold time	t_{CSS} t_{CSH}	!SCE	60 65		- -	ns

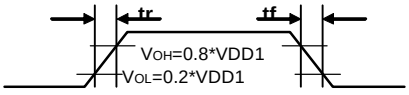
NOTE: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Logic high and low levels are specified as 30% and 70% of VDD1 for Input signals. For output, see Section 7.7.6.2

Input Signal Slope



Output Signal Slope



8.7.4 Serial Interface Characteristics (4-Pin Serial)

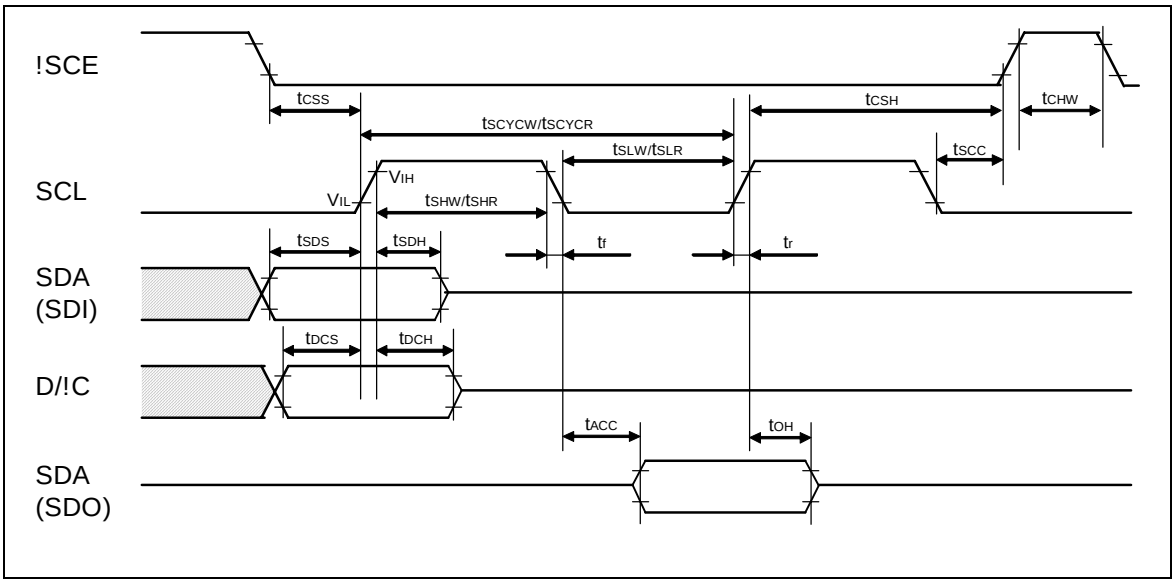


Fig. 8.7.6 4-pin serial interface characteristics

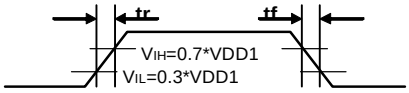
(V_{SS}=0V, V_{DD1}=1.65V to 1.95V, V_{DD2}=2.5V to 2.9V,Ta = -30 to 75°C)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Serial clock cycle (Write) SCL "H" pulse width (Write) SCL "L" pulse width (Write)	t_{SCYCW} t_{SHW} t_{SLW}	SCL	100 35 35		- -	ns
Data setup time (Write) Data hold time (Write)	t_{SDS} t_{SDH}	SDA	30 30		- -	ns
DC setup time DC hold time	t_{DCS} t_{DCH}	DC	30 30		- -	ns
Serial clock cycle (Read) SCL "H" pulse width (Read) SCL "L" pulse width (Read)	t_{SCYCR} t_{SHR} t_{SLR}	SCL	150 60 60		- - -	ns
Access rime	t_{ACC}	SDA For maximum C_L=30pF For minimum C_L=8pF	10		50	ns
Output disable time	t_{OH}	SDA For maximum C_L=30pF For minimum C_L=8pF	15		50	ns
SCL to Chip select	t_{SCC}	!SCE	15			ns
SCEB "H" pulse width	t_{CHW}	!SCE	45			ns
Chip select setup time Chip select hold time	t_{CSS} t_{CSH}	!SCE	60 65		- -	ns

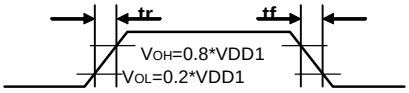
NOTE: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Logic high and low levels are specified as 30% and 70% of VDD1 for Input signals. For output, see Section 7.7.6.2

Input Signal Slope



Output Signal Slope



8.7.5 RGB Interface Characteristics

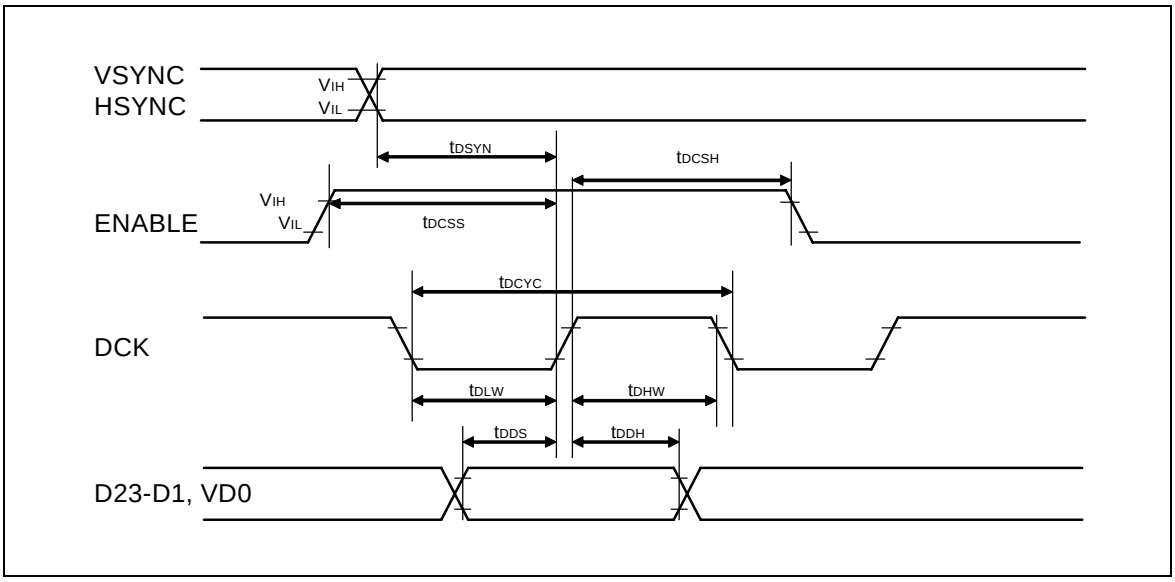


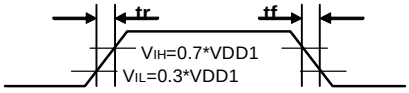
Fig. 8.7.7 RGB Interface characteristics

(V_{SS}=0V, V_{DD1}=1.65V to 1.95V, V_{DD2}=2.5V to 2.9V,Ta = -30 to 75°C)

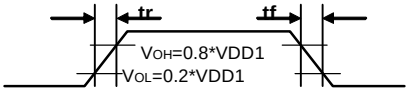
Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	Unit
t_{DCYC} t_{DLW} t_{CHW}	DCK cycle time DCK Low time DCK High time	-	DCK	TBD TBD TBD	- -	- -	ns
t_{DDS} t_{DDH}	RGB Data setup time RGB Data hold time	-	DCK, D23-D1, VD0	20 20	- -	- -	ns
t_{DCSS} t_{DCSH}	ENABLE setup time ENABLE hold Time	-	ENABLE	150 150	-	-	ns
t_{DSYN}	SYNC setup time	-	DCK, HSYNC, VSYNC	20	-	-	ns

NOTE: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Input Signal Slope



Output Signal Slope



8.7.6 Reset Input Timing

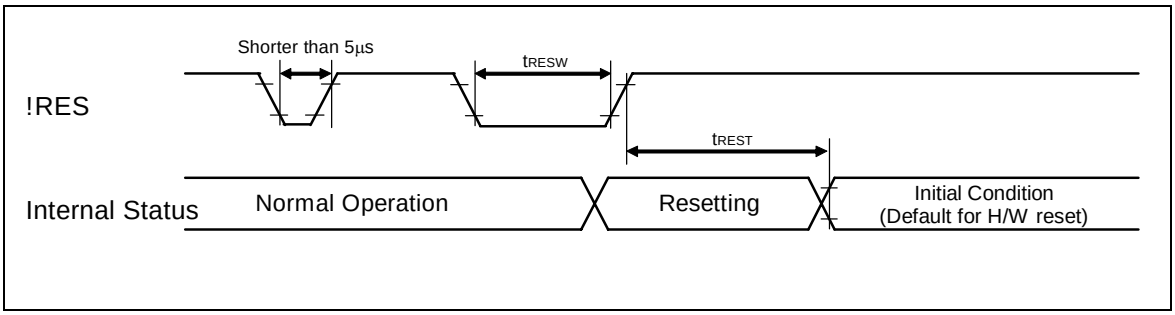


Fig. 8.7.8 Reset input timing

(V_{SS}=0V, V_{DD1}=1.65V to 1.95V, V_{DD2}=2.5V to 2.9V,Ta = -30 to 75°C)

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESB	10	-	-	-	µs
t_{REST}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep In mode	ms
		-		-	120	When reset applied during Sleep Out mode	ms

NOTE:

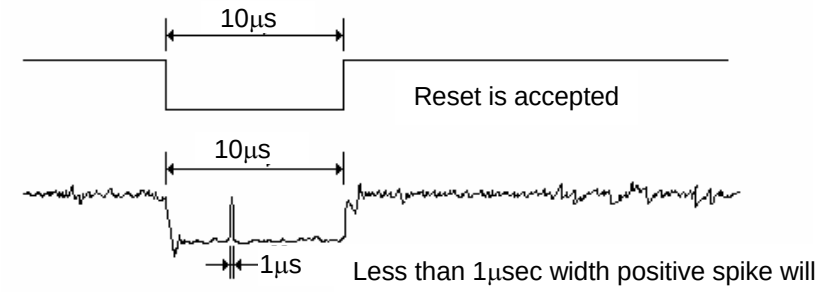
1) Spike due to an electrostatic discharge on RESB line does not cause irregular system reset according to the table below.

RESB Pulse	*Action*
Shorter than 5µs	*Reset Rejected*
Longer than 10µs	*Reset*
Between 5µs and 10µs	*Reset Start*

2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

3) During Reset Complete Time, ID2 and VCOMOF value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESB.

4) Spike Rejection also applies during a valid reset pulse as shown below:



5) It is necessary to wait 5msec after releasing RESB before sending commands. Also Sleep Out command cannot be sent for 120msec.

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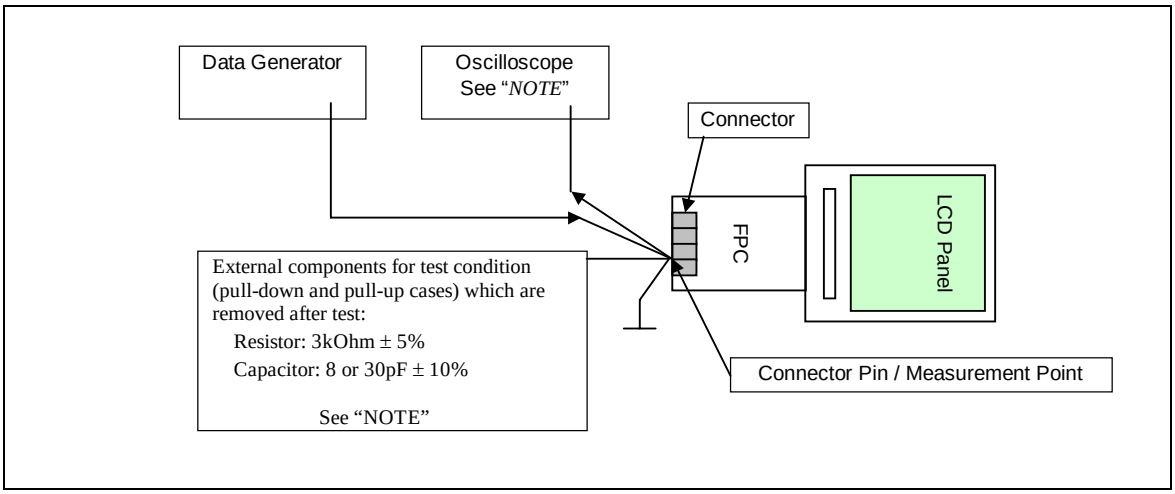
8.7.7 Measurement Conditions

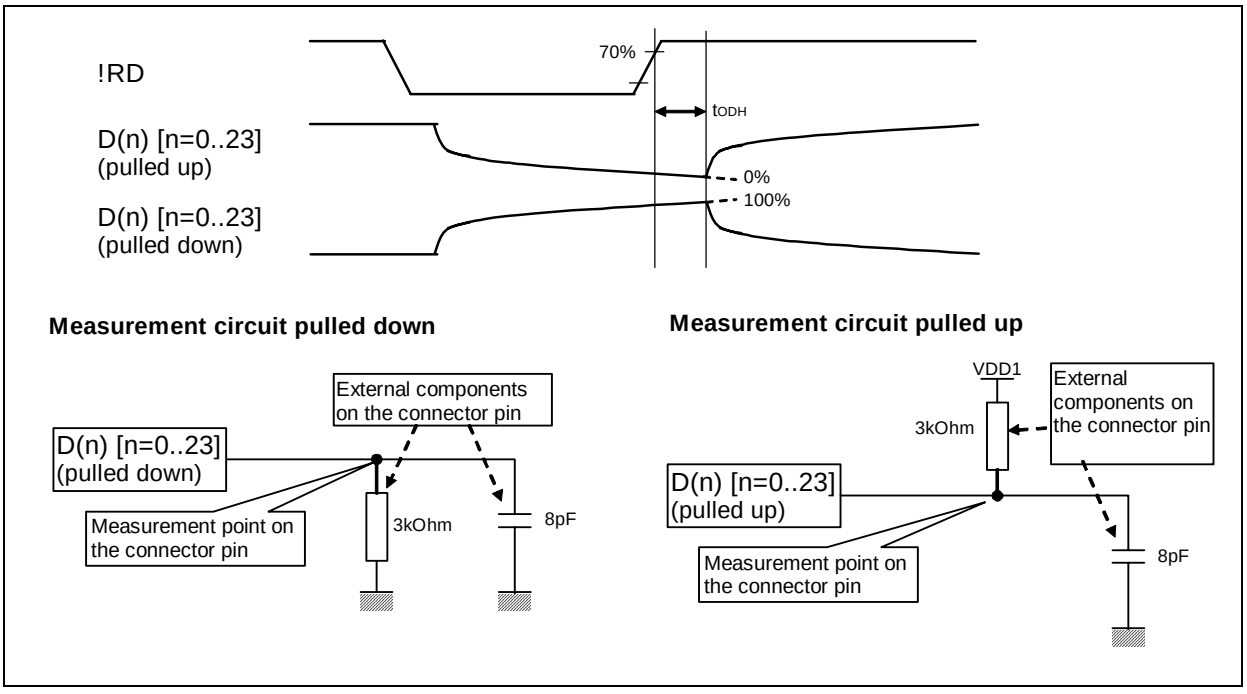
8.7.7.1 t_{RATFM}, t_{ODH} Measurement Condition

Measurement Condition Set-up

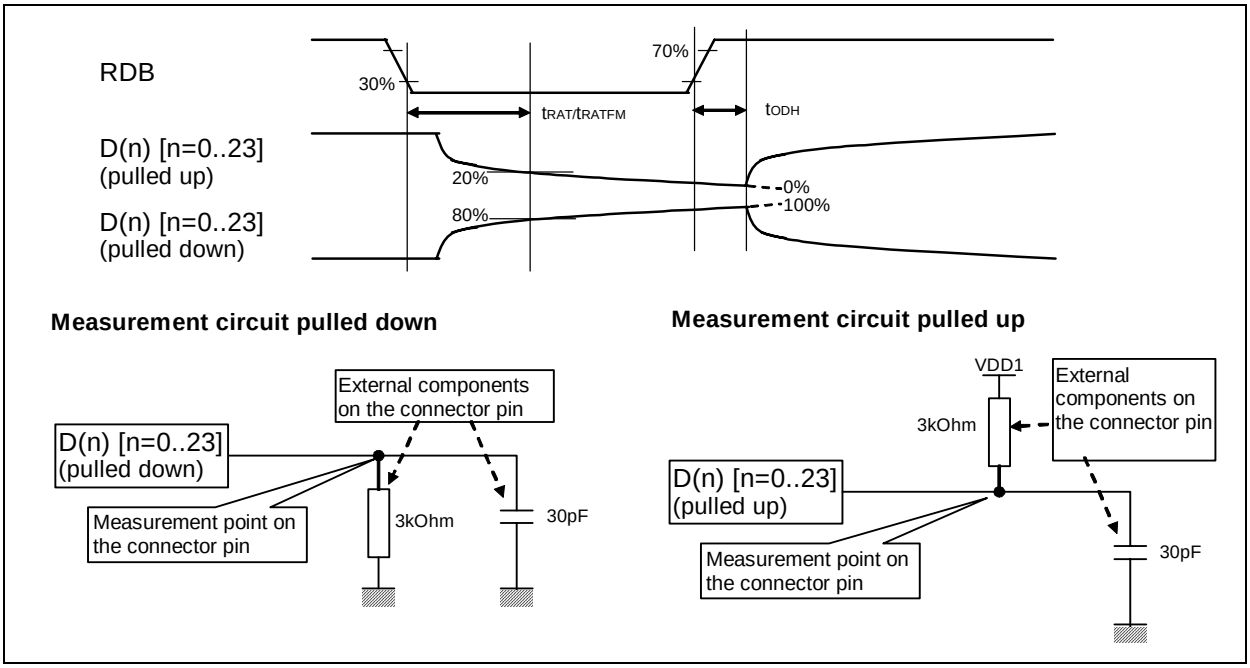


NOTE: Capacitances and resistances of the oscilloscope's probe must be included externals components in these measurements

Minimum Value Measurement

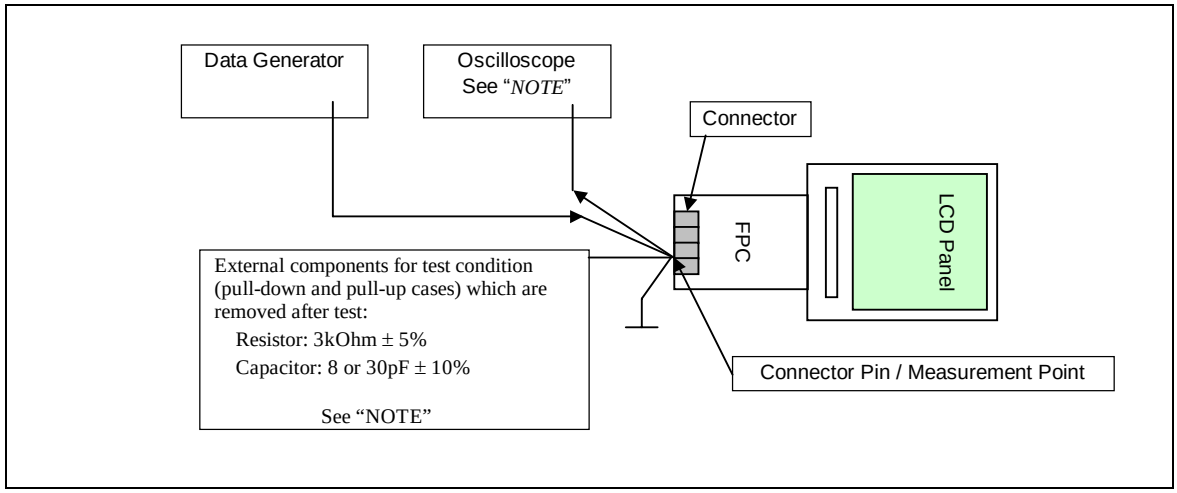


Maximum Value Measurement



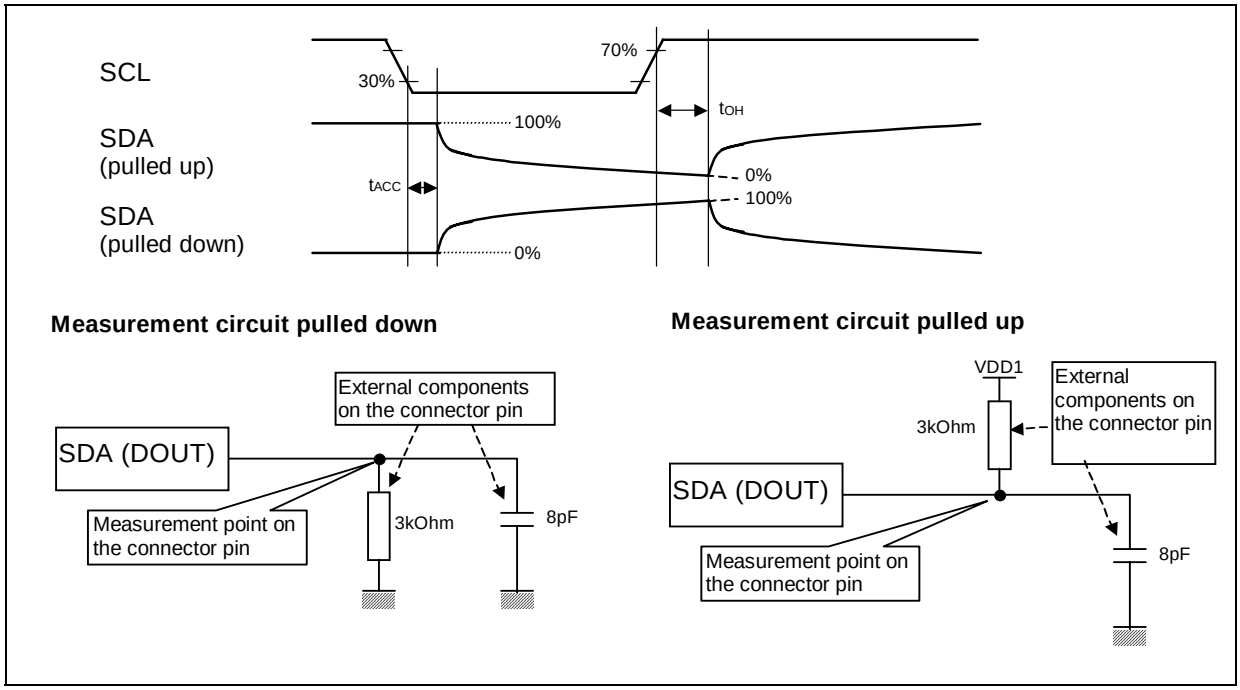
8.7.7.2 t_{ACC}, t_{OH} Measurement Condition

Measurement Condition Set-up

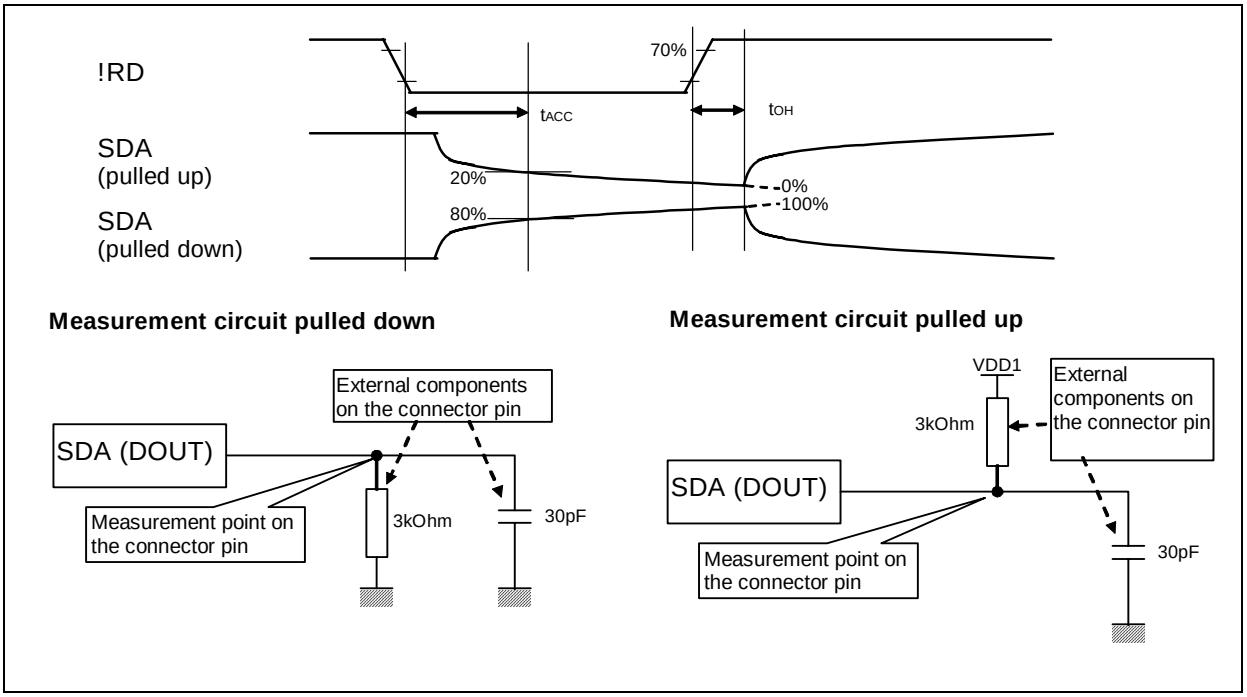


NOTE: Capacitances and resistances of the oscilloscope's probe must be included externals components in these measurements

Minimum Value Measurement



Maximum Value Measurement



9 REFERENCE APPLICATIONS

9.1 MICROPROCESSOR INTERFACE

9.1.1 Interfacing with 3-Pin Serial Mode (P68 = "L", BS2=”L”, BS1 = "L", BS0 = "L")

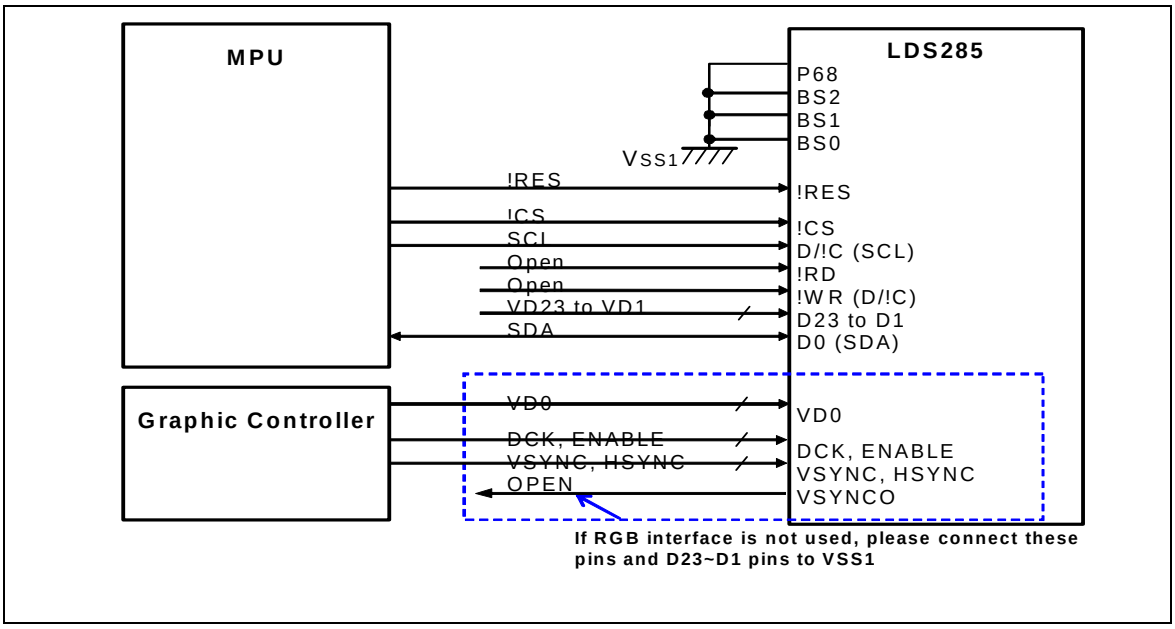


Fig. 9.1.1 Interfacing with 3-Pin Serial Mode

9.1.2 Interfacing with 4-Pin Serial Mode (P68 = "H", BS2=”L”, BS1 = "L", BS0 = "L")

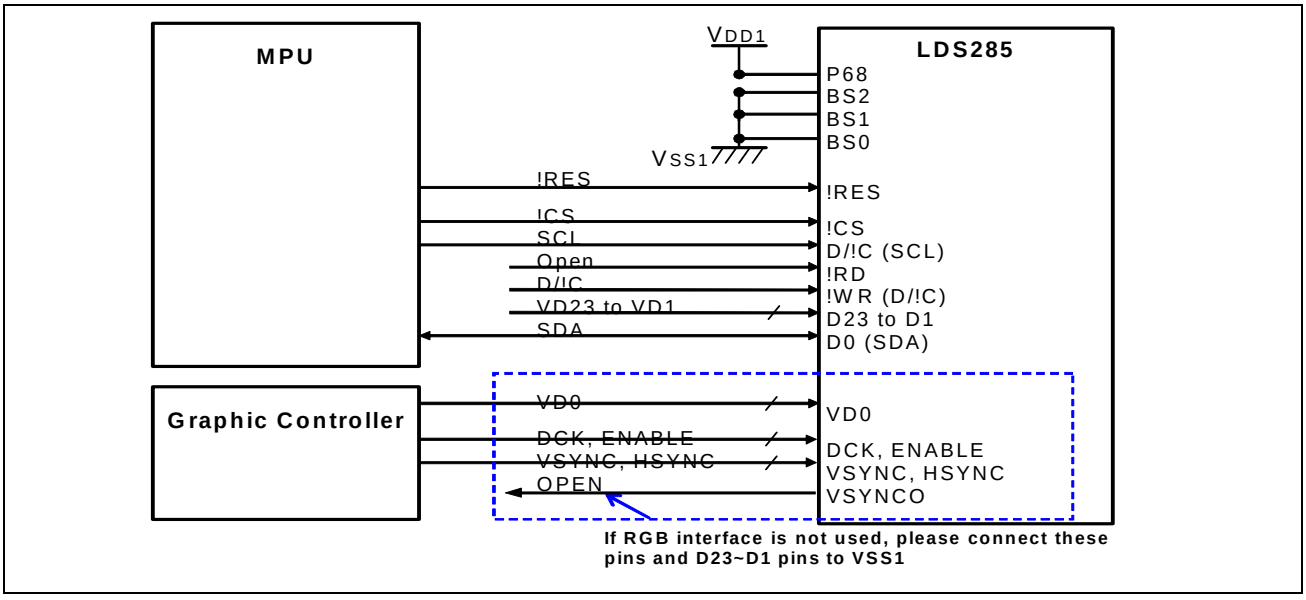


Fig. 9.1.2 Interfacing with 4-Pin Serial Mode

9.1.3 Interfacing with 8080-series MPU 8-Bit Bus (P68 = "L", BS2="L", BS1 = "L", BS0 = "H")

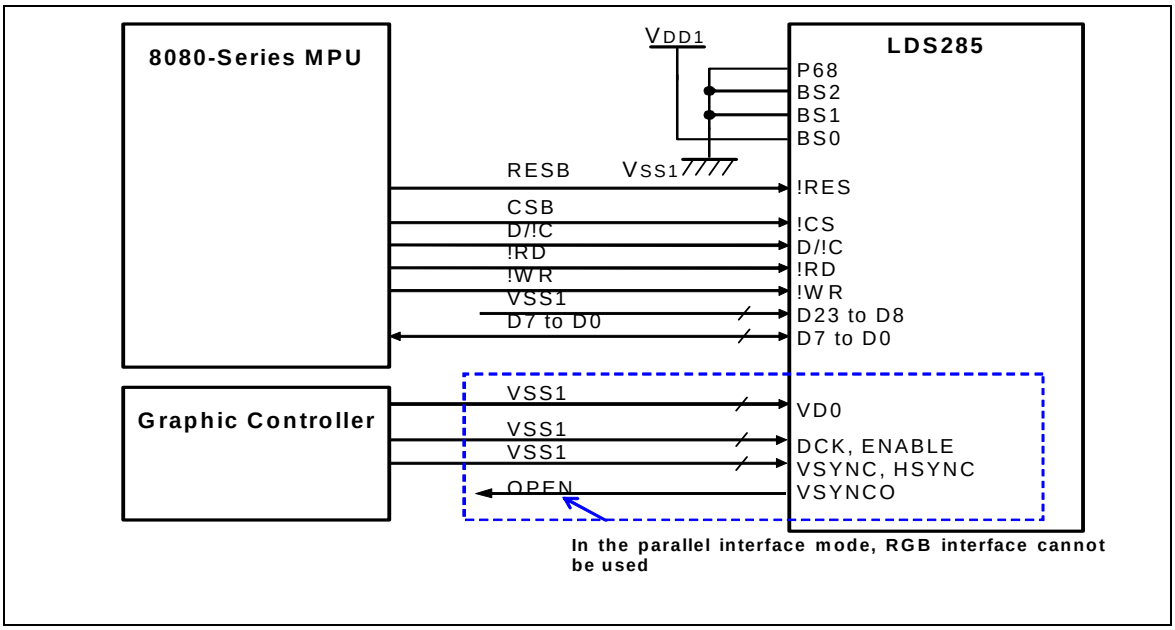


Fig. 9.1.3 Interfacing with 8-bit 8080-series

9.1.4 Interfacing with 6800-series MPU 8-Bit Bus (P68 = "H", BS2="L", BS1 = "L", BS0 = "H")

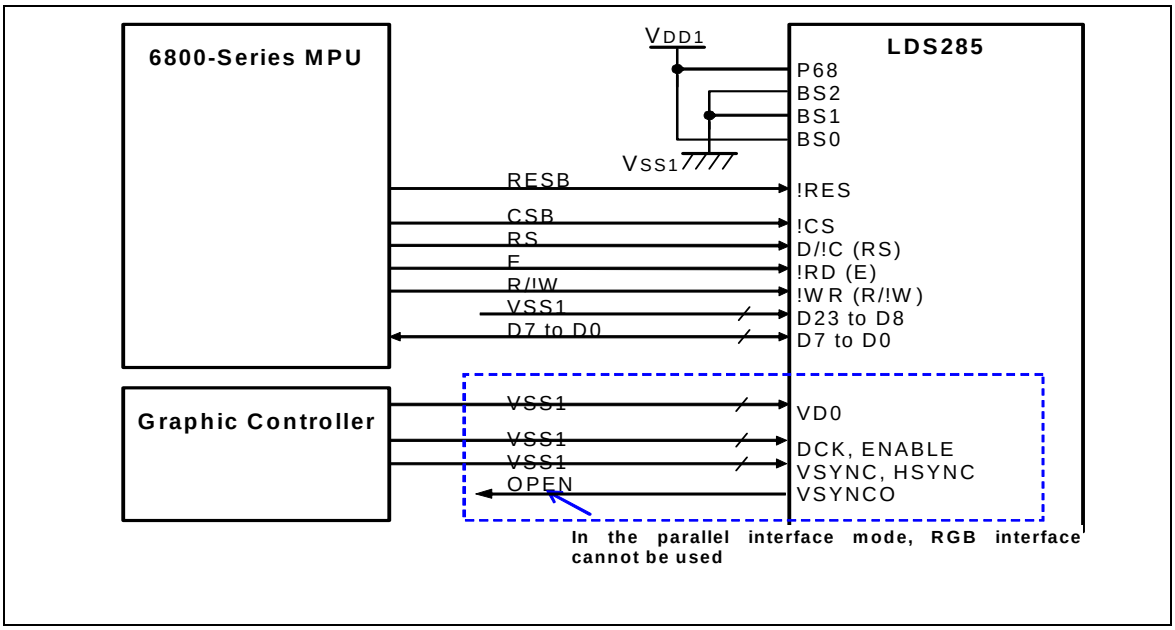


Fig. 9.1.4 Interfacing with 8-bit 6800-series

9.1.5 Interfacing with 8080-series MPU 9-Bit Bus (P68 = "L", BS2="H", BS1 = "L", BS0 = "L")

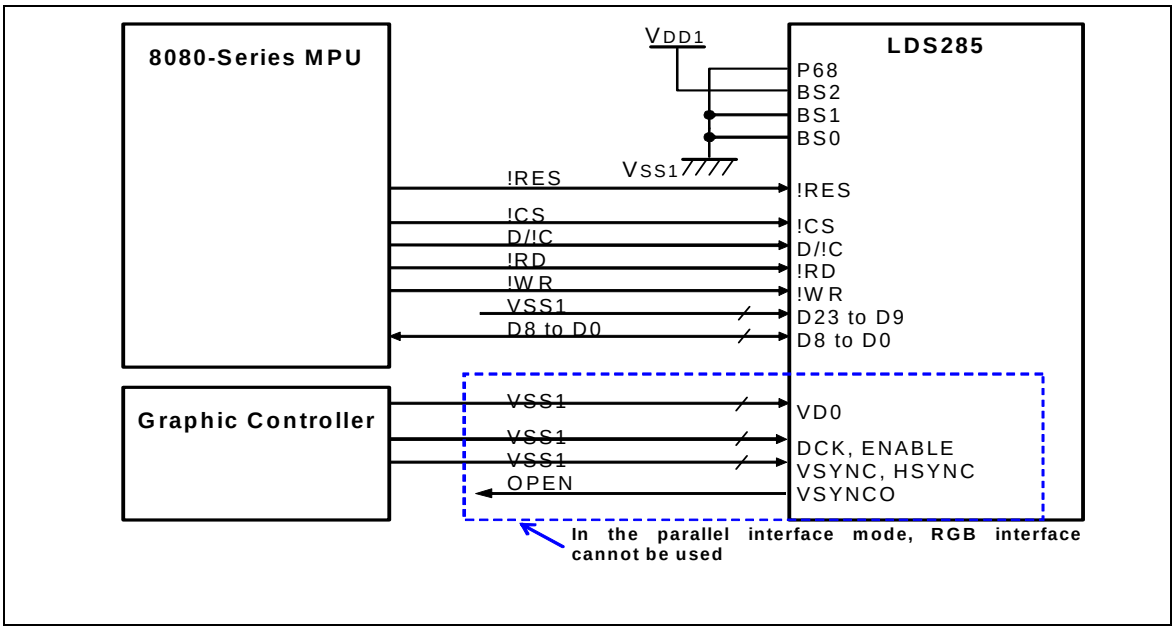


Fig. 9.1.5 Interfacing with 8-bit 8080-series

9.1.6 Interfacing with 6800-series MPU 9-Bit Bus (P68 = "H", BS2="H", BS1 = "L", BS0 = "L")

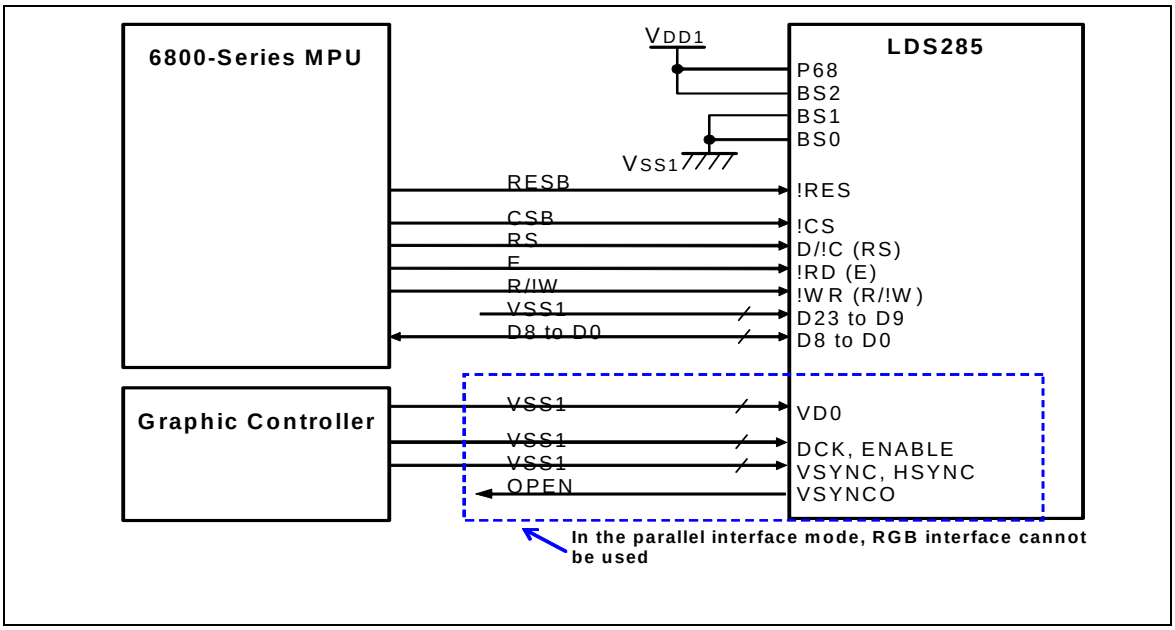


Fig. 9.1.6 Interfacing with 8-bit 6800-series

9.1.7 Interfacing with 8080-series MPU 16-Bit Bus (P68 = "L", BS2="L", BS1 = "H", BS0 = "H")

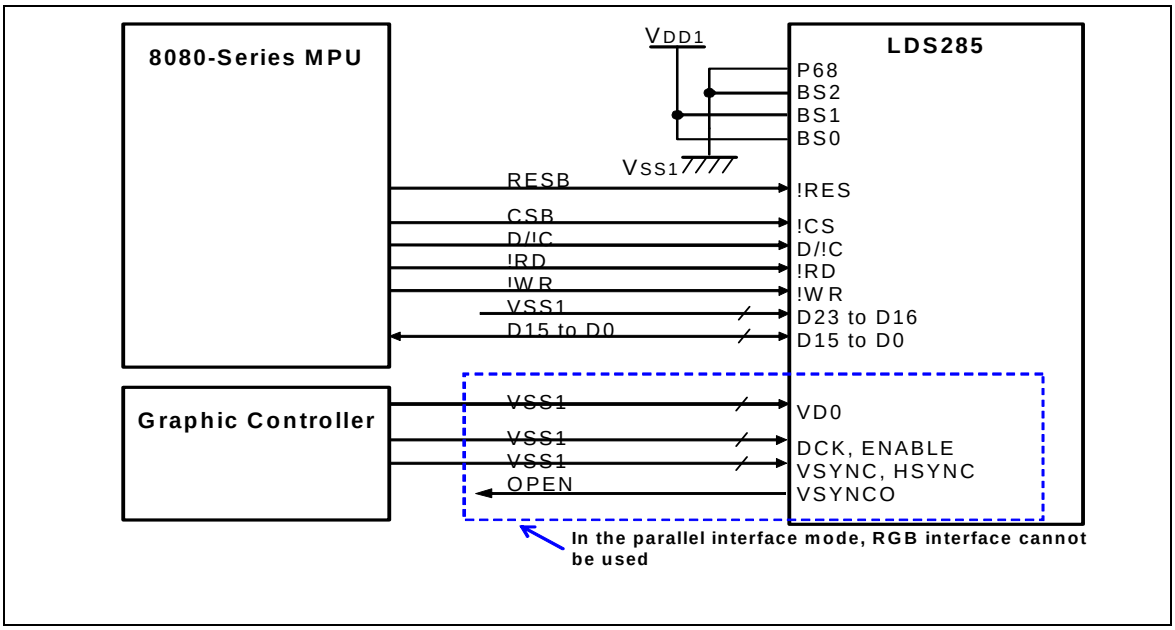


Fig. 9.1.7 Interfacing with 16-bit 8080-series

9.1.8 Interfacing with 6800-series MPU 16-Bit Bus (P68 = "H", BS2="L", BS1 = "H", BS0 = "H")

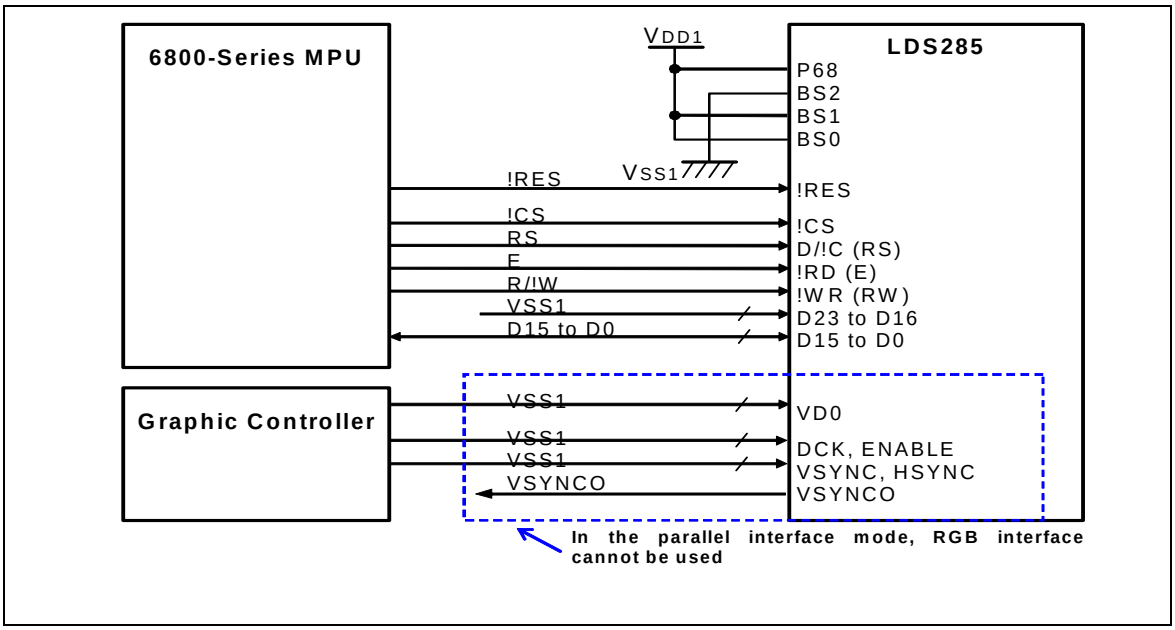


Fig. 9.1.8 Interfacing with 16-bit 6800-series

9.1.9 Interfacing with 8080-series MPU 18-Bit Bus (P68 = "L", BS2=”H”, BS1 = "H", BS0 = "L")

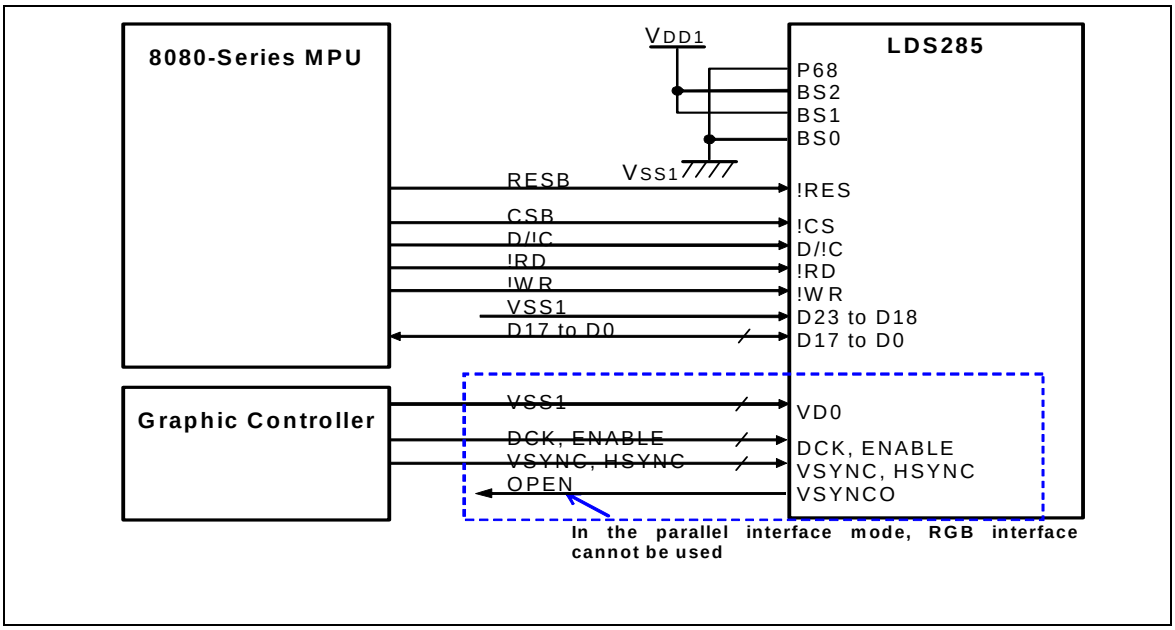


Fig. 9.1.9 Interfacing with 18-bit 8080-series

9.1.10 Interfacing with 6800-series MPU 18-Bit Bus (P68 = "H", BS2=”H”, BS1 = "H", BS0 = "L")

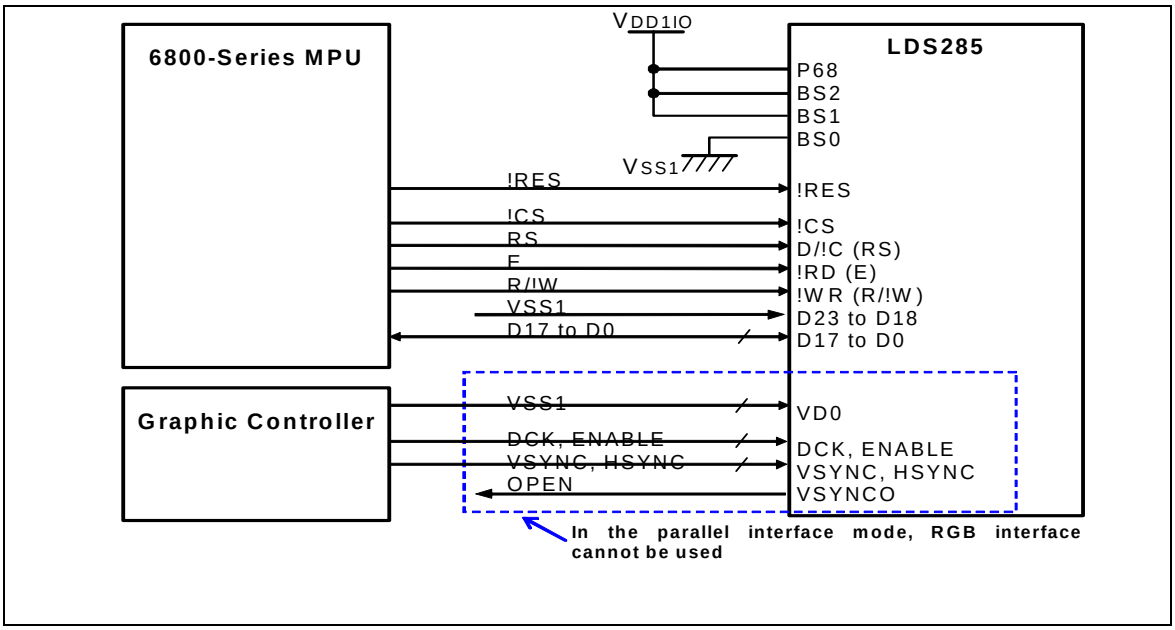
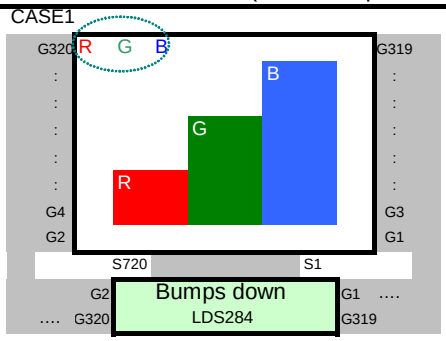
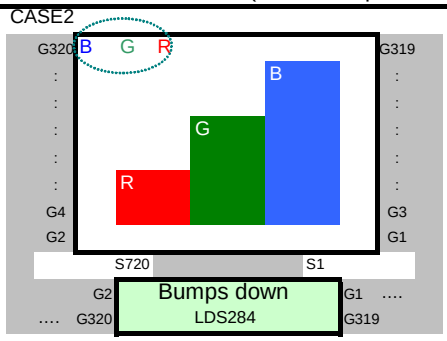
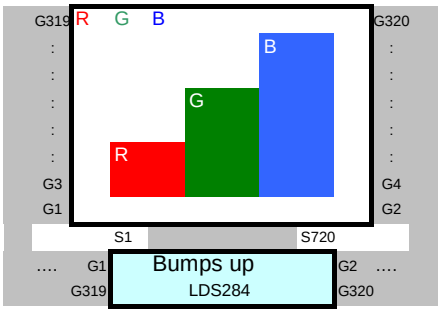
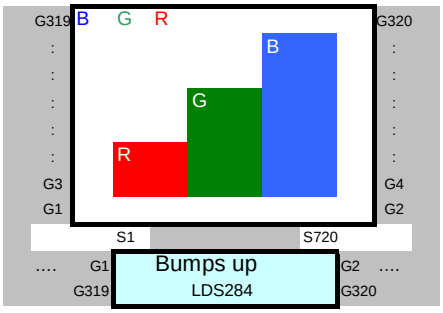
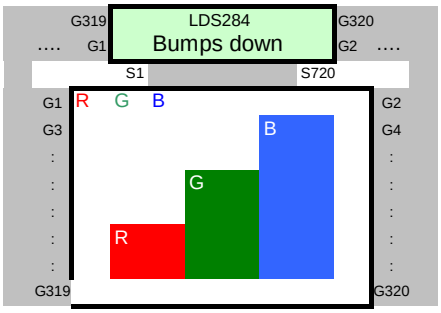
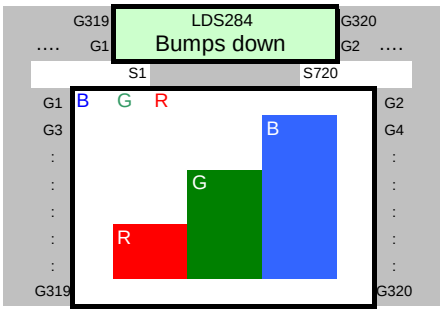
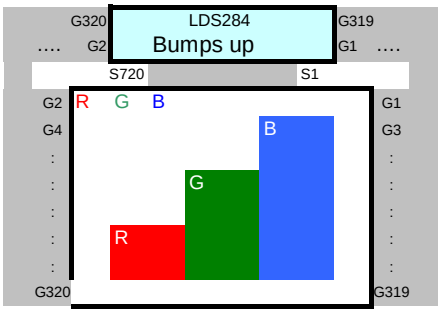
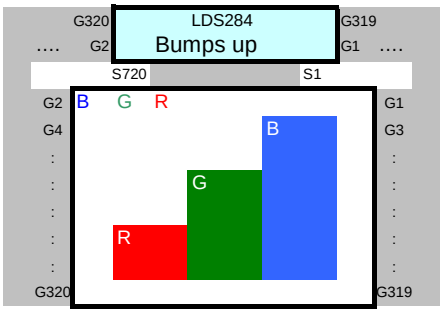


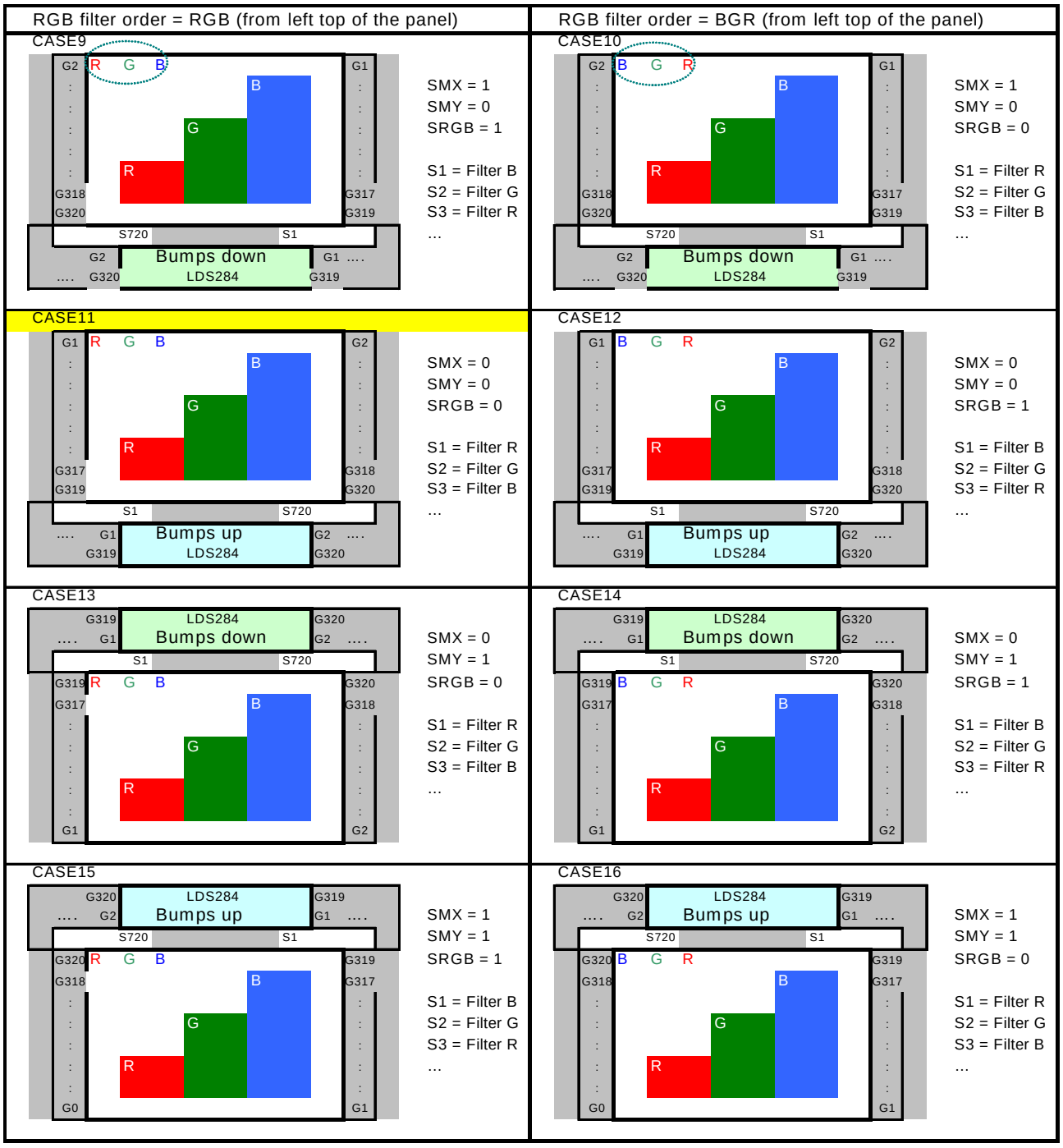
Fig. 9.1.10 Interfacing with 18-bit 6800-series

9.2 CONNECTIONS WITH LCD PANEL

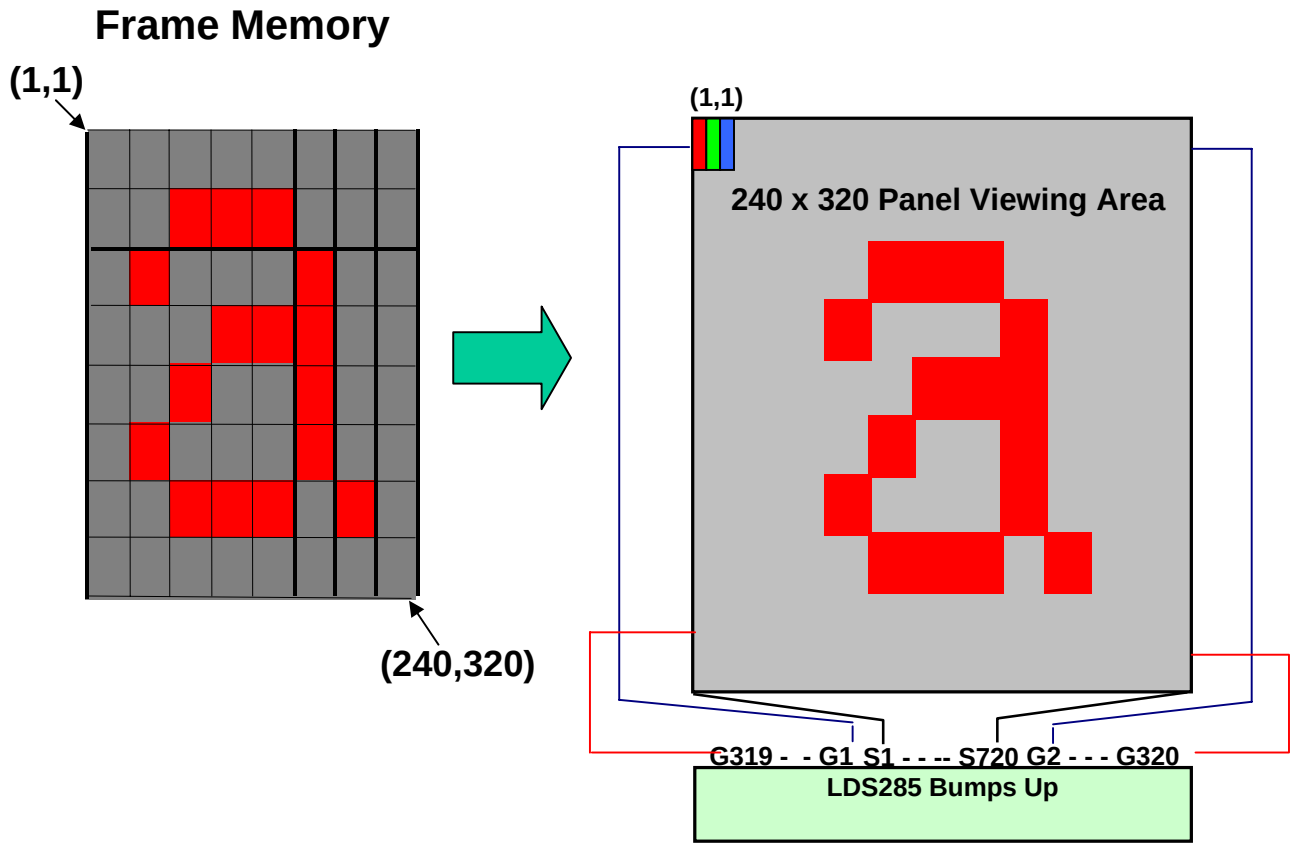
9.2.1 One Layer Connection for Gate output

RGB filter order = RGB (from left top of the panel)	RGB filter order = BGR (from left top of the panel)
CASE1  SMX = 1 SMY = 1 SRGB = 1 S1 = Filter B S2 = Filter G S3 = Filter R …	CASE2  SMX = 1 SMY = 1 SRGB = 0 S1 = Filter R S2 = Filter G S3 = Filter B …
CASE3  SMX = 0 SMY = 1 SRGB = 0 S1 = Filter R S2 = Filter G S3 = Filter B …	CASE4  SMX = 0 SMY = 1 SRGB = 1 S1 = Filter B S2 = Filter G S3 = Filter R …
CASE5  SMX = 0 SMY = 0 SRGB = 0 S1 = Filter R S2 = Filter G S3 = Filter B …	CASE6  SMX = 0 SMY = 0 SRGB = 1 S1 = Filter B S2 = Filter G S3 = Filter R …
CASE7  SMX = 1 SMY = 0 SRGB = 1 S1 = Filter B S2 = Filter G S3 = Filter R …	CASE8  SMX = 1 SMY = 0 SRGB = 0 S1 = Filter R S2 = Filter G S3 = Filter B …

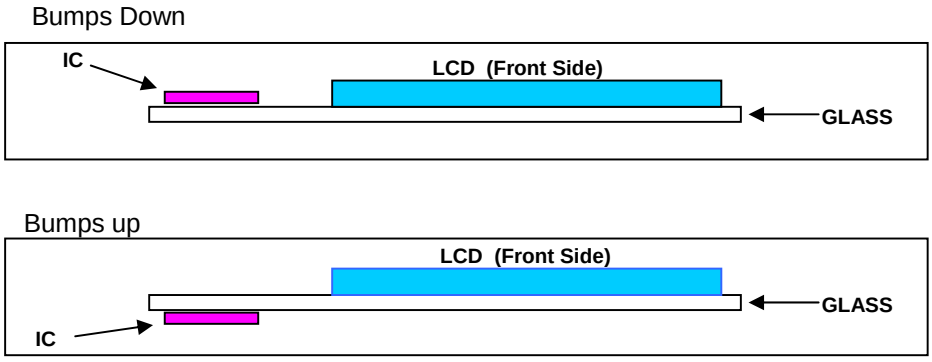
9.2.2 Two Layer Connection for Gate output



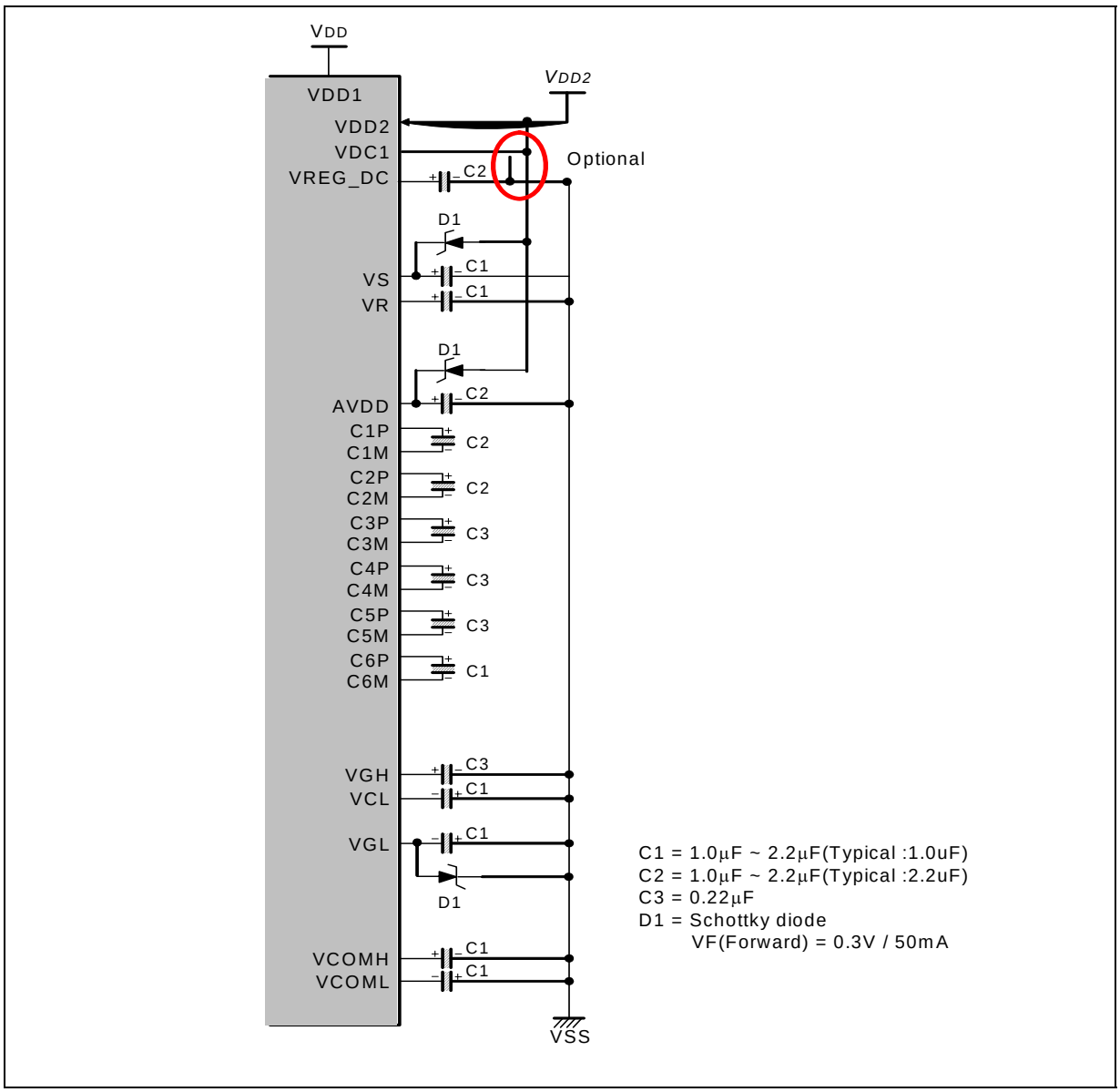
9.3 EXAMPLE CONNECTION WITH PANEL (CASE11)



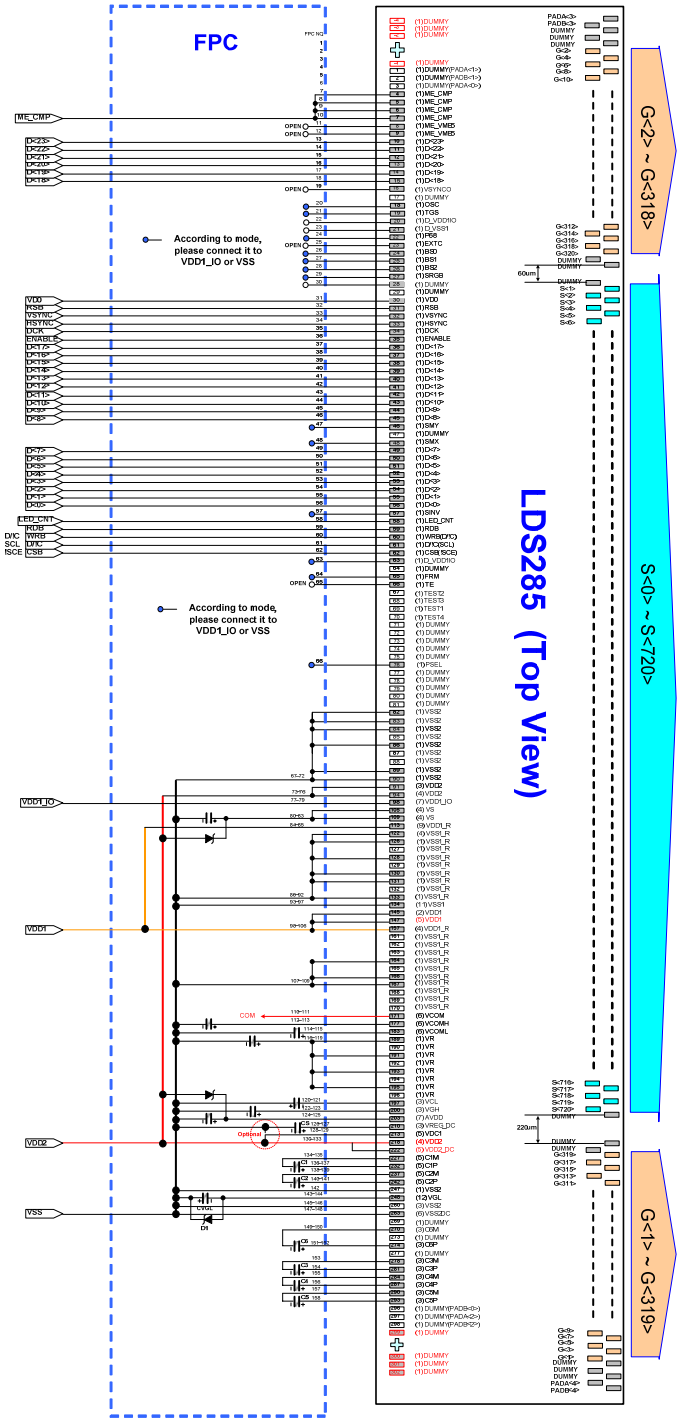
SMX = VSS
SMY = VSS
SRGB = VSS



9.4 CONNECTION EXAMPLE WITH EXTERNAL COMPONENTS



9.4.1 Application Circuit Example



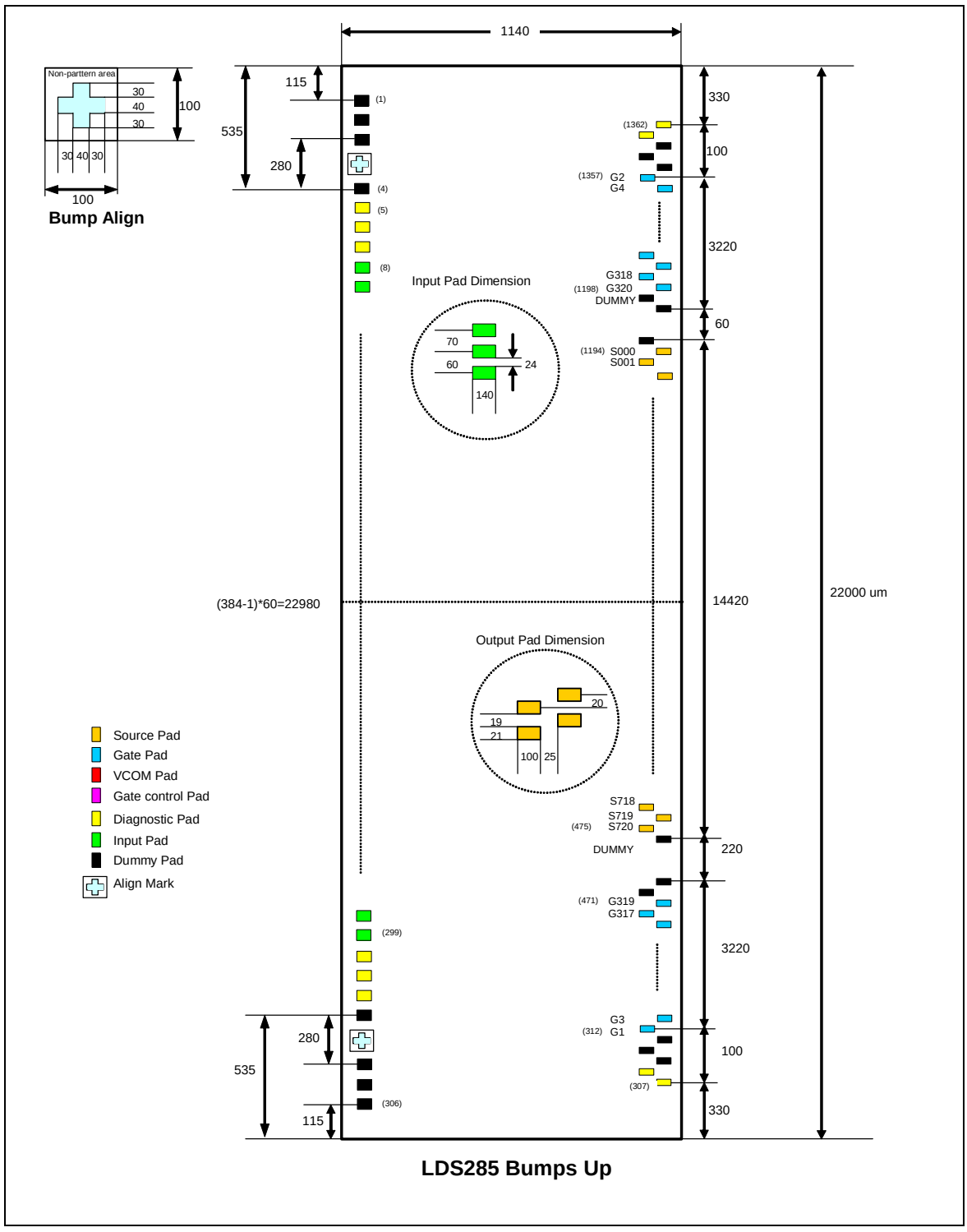
NOTE: 1) To use extended command set like EEPROM program, EXTC should be connected to VDD1 and External voltage should be appled to ME_CMP pad, so, EXTC and ME_CMP should have probing point for mass production.

9.5 EXTERNAL COMPONENTS CONNECTION

Pad Name	Connection	Typical capacitance value
VCOMH	Connect to Capacitor (Max 6V): VCOMH---(+)----| |--- (-)------VSS	1.0 uF
VCOML	Connect to Capacitor (Max 3V): VCOML ---(-)----| |--- (+)-----VSS	1.0 uF
VGL	Connect to Capacitor (Max 12V): VGL ---(-)----| |--- (+)-----VSS	1.0 uF
VCL	Connect to Capacitor (Max 5V): VCL ---(-)----| |--- (+)-----VSS	1.0 uF
VSS1_R	Connect to VSS(GND)	
VSS1	Connect to VSS(GND)	
VSS2	Connect to VSS(GND)	
VSS2_DC	Connect to VSS(GND)	
VDD1_R	Connect to VDD1	
VDD2_DC	Connect to VDD2	
VGH	Connect to Capacitor (Max 16V): VGH ---(+)----| |--- (-)-----VSS	1.0 uF
C6+, C6-	Connect to Capacitor (Max 5V): C6+ ---(+)----| |--- (-)-----C6-	1.0 uF
C5+, C5-	Connect to Capacitor (Max 7V): C5+ ---(+)----| |--- (-)-----C5-	1.0 uF
C4+, C4-	Connect to Capacitor (Max 7V): C4+ ---(+)----| |--- (-)-----C4-	1.0 uF
C3+, C3-	Connect to Capacitor (Max 7V): C3+ ---(+)----| |--- (-)-----C3-	1.0 uF
C2+, C2-	Connect to Capacitor (Max 5V): C2+ ---(+)----| |--- (-)-----C2-	2.2 uF
C1+, C1-	Connect to Capacitor (Max 5V): C1+ ---(+)----| |--- (-)-----C1-	2.2 uF
VDC1	Connect to VDD2(in case of x3 avdd3 mode, Connect to VREG_DC)	
VREG_DC	Connect to Capacitor (Max 2.6V): VREG_DC ---(+)----| |--- (-)-----VSS	2.2 uF
AVDD	Connect to Capacitor (Max 6V): AVDD ---(+)----| |--- (-)-----VSS	2.2 uF
VR	Connect to Capacitor (Max 6V): VR ---(+)----| |--- (-)-----VSS	1.0 uF
VS	Connect to Capacitor (Max 6V): VS ---(+)----| |--- (-)-----VSS	1.0 uF
VDD1	**When "PSEL = Low" VDDI (Digital Power)** **When "PSEL = High"** **Connect to Capacitor** (Max 5V): VDD1 (R) ---(+)----| |--- (-)-----VSS	**2.2 uF**
VGL	Connect to Shottky Diode between VSS	VF = 0.3V / 50mA
AVDD	Connect to Shottky Diode between VDD2	VF = 0.3V / 50mA
VS	Connect to Shottky Diode between VDD2	VF = 0.3V / 50mA

10 CHIP INFORMATION

10.1 CHIP OVERVIEW



NOTE:

** Chip Size = 22,000 x 1140 (Excluding Scribe Lane)*

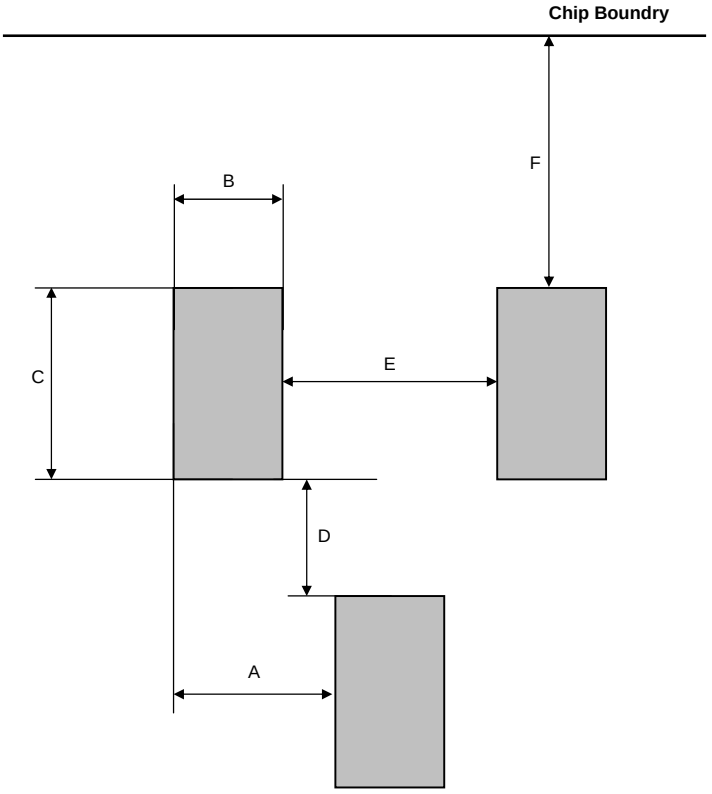
** Chip Thickness = 410 ± 12 μm*

** Bump height = 15 ± 3 μm (chip to chip), less than 2 μm (pad to pad in one chip)*

10.2 BUMP INFORMATION

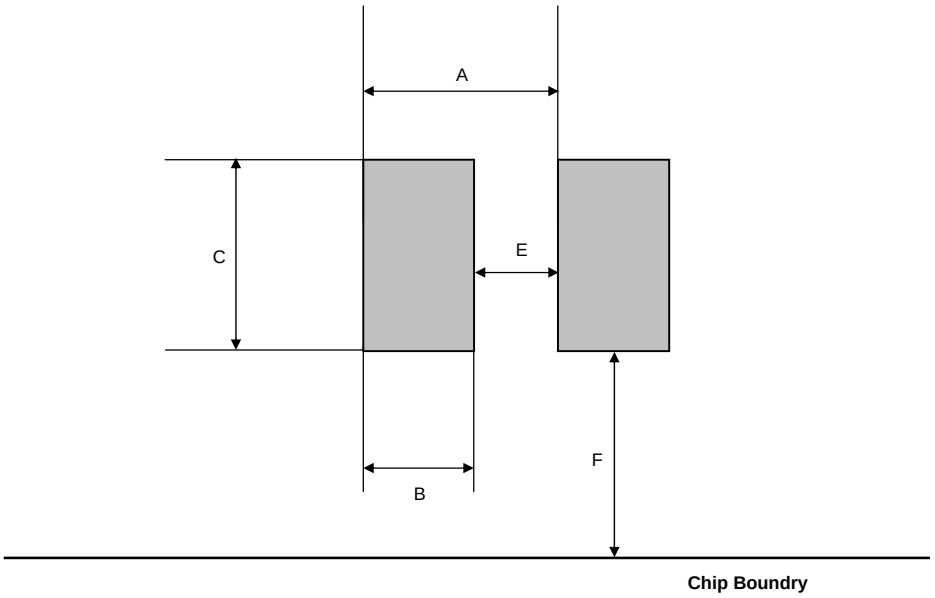
10.2.1 Source / Gate / VCOM / Gate control / Output side dummy Pad Format

Item	Symbol	Size
		Source / Gate / VCOM / Gate control / / Output side dummy pad
Pad pitch	A	20um
Bump width	B	21 um
Bump length	C	100 um
Bump to Bump gap1 (Vertical)	D	25 um
Bump to Bump gap2 (Horizontal)	E	19 um
Bump area	B*C	2100 um^2
Chip boundary to Bump edge	F	8.5 um



10.2.2 Input / Input side dummy Pad Format

Item	Symbol	Size
		Input / Input side dummy pad
Pad pitch	A	70 um
Bump width	B	50 um
Bump length	C	80 um
Bump to Bump gap (Horizontal)	E	20 um
Bump area	B*C	4000 um^2
Chip boundary to Bump edge	F	12.5 um



10.3 PAD COORDINATES

Table 10.3.1 Pad Center Coordinates

No	Name	X	Y	No	Name	X	Y
1	DUMMY	-10885	-517.5	51	DUMMY	-7175	-517.5
2	DUMMY	-10815	-517.5	52	SMX	-7105	-517.5
3	DUMMY	-10745	-517.5	53	D<7>	-7035	-517.5
4	DUMMY	-10465	-517.5	54	D<6>	-6965	-517.5
5	PADA<0>	-10395	-517.5	55	D<5>	-6895	-517.5
6	PADA<1>	-10325	-517.5	56	D<4>	-6825	-517.5
7	PADB<1>	-10255	-517.5	57	D<3>	-6755	-517.5
8	ME_CMP	-10185	-517.5	58	D<2>	-6685	-517.5
9	ME_CMP	-10115	-517.5	59	D<1>	-6615	-517.5
10	ME_CMP	-10045	-517.5	60	D<0>	-6545	-517.5
11	ME_CMP	-9975	-517.5	61	SINV	-6475	-517.5
12	ME_VME5	-9905	-517.5	62	LED_CNT	-6405	-517.5
13	ME_VME5	-9835	-517.5	63	RDB	-6335	-517.5
14	D<23>	-9765	-517.5	64	WRB	-6265	-517.5
15	D<22>	-9695	-517.5	65	DC	-6195	-517.5
16	D<21>	-9625	-517.5	66	CSB	-6125	-517.5
17	D<20>	-9555	-517.5	67	D_VDD1IO	-6055	-517.5
18	D<19>	-9485	-517.5	68	DUMMY	-5985	-517.5
19	D<18>	-9415	-517.5	69	FRM	-5915	-517.5
20	VSYNCO	-9345	-517.5	70	TE	-5845	-517.5
21	DUMMY	-9275	-517.5	71	TEST2	-5775	-517.5
22	OSC	-9205	-517.5	72	TEST3	-5705	-517.5
23	TGS	-9135	-517.5	73	TEST1	-5635	-517.5
24	D_VDD1IO	-9065	-517.5	74	TEST4	-5565	-517.5
25	D_VSS1	-8995	-517.5	75	DUMMY	-5495	-517.5
26	P68	-8925	-517.5	76	DUMMY	-5425	-517.5
27	EXTC	-8855	-517.5	77	DUMMY	-5355	-517.5
28	BS0	-8785	-517.5	78	DUMMY	-5285	-517.5
29	BS1	-8715	-517.5	79	DUMMY	-5215	-517.5
30	BS2	-8645	-517.5	80	PSEL	-5145	-517.5
31	SRGB	-8575	-517.5	81	DUMMY	-5075	-517.5
32	DUMMY	-8505	-517.5	82	DUMMY	-5005	-517.5
33	DUMMY	-8435	-517.5	83	DUMMY	-4935	-517.5
34	VD0	-8365	-517.5	84	DUMMY	-4865	-517.5
35	RSB	-8295	-517.5	85	DUMMY	-4795	-517.5
36	VSYNC	-8225	-517.5	86	VSS2	-4725	-517.5
37	HSYNC	-8155	-517.5	87	VSS2	-4655	-517.5
38	DCK	-8085	-517.5	88	VSS2	-4585	-517.5
39	ENABLE	-8015	-517.5	89	VSS2	-4515	-517.5
40	D<17>	-7945	-517.5	90	VSS2	-4445	-517.5
41	D<16>	-7875	-517.5	91	VSS2	-4375	-517.5
42	D<15>	-7805	-517.5	92	VSS2	-4305	-517.5
43	D<14>	-7735	-517.5	93	VSS2	-4235	-517.5
44	D<13>	-7665	-517.5	94	VSS2	-4165	-517.5
45	D<12>	-7595	-517.5	95	VDD2	-4095	-517.5
46	D<11>	-7525	-517.5	96	VDD2	-4025	-517.5
47	D<10>	-7455	-517.5	97	VDD2	-3955	-517.5
48	D<9>	-7385	-517.5	98	VDD2	-3885	-517.5
49	D<8>	-7315	-517.5	99	VDD2	-3815	-517.5
50	SMY	-7245	-517.5	100	VDD2	-3745	-517.5

- continued -

No	Name	X	Y	No	Name	X	Y
101	VDD2	-3675	-517.5	151	VDD1	-175	-517.5
102	VDD1_IO	-3605	-517.5	152	VDD1	-105	-517.5
103	VDD1_IO	-3535	-517.5	153	VDD1	-35	-517.5
104	VDD1_IO	-3465	-517.5	154	VDD1	35	-517.5
105	VDD1_IO	-3395	-517.5	155	VDD1	105	-517.5
106	VDD1_IO	-3325	-517.5	156	VDD1	175	-517.5
107	VDD1_IO	-3255	-517.5	157	VDD1	245	-517.5
108	VDD1_IO	-3185	-517.5	158	VDD1	315	-517.5
109	VS	-3115	-517.5	159	VDD1	385	-517.5
110	VS	-3045	-517.5	160	VDD1	455	-517.5
111	VS	-2975	-517.5	161	VDD1_R	525	-517.5
112	VS	-2905	-517.5	162	VDD1_R	595	-517.5
113	VS	-2835	-517.5	163	VDD1_R	665	-517.5
114	VS	-2765	-517.5	164	VDD1_R	735	-517.5
115	VS	-2695	-517.5	165	VSS1_R	805	-517.5
116	VS	-2625	-517.5	166	VSS1_R	875	-517.5
117	VDD1_R	-2555	-517.5	167	VSS1_R	945	-517.5
118	VDD1_R	-2485	-517.5	168	VSS1_R	1015	-517.5
119	VDD1_R	-2415	-517.5	169	VSS1_R	1085	-517.5
120	VDD1_R	-2345	-517.5	170	VSS1_R	1155	-517.5
121	VDD1_R	-2275	-517.5	171	VSS1_R	1225	-517.5
122	VDD1_R	-2205	-517.5	172	VSS1_R	1295	-517.5
123	VDD1_R	-2135	-517.5	173	VSS1_R	1365	-517.5
124	VDD1_R	-2065	-517.5	174	VSS1_R	1435	-517.5
125	VDD1_R	-1995	-517.5	175	VCOM	1505	-517.5
126	VSS1_R	-1925	-517.5	176	VCOM	1575	-517.5
127	VSS1_R	-1855	-517.5	177	VCOM	1645	-517.5
128	VSS1_R	-1785	-517.5	178	VCOM	1715	-517.5
129	VSS1_R	-1715	-517.5	179	VCOM	1785	-517.5
130	VSS1_R	-1645	-517.5	180	VCOM	1855	-517.5
131	VSS1_R	-1575	-517.5	181	VCOMH	1925	-517.5
132	VSS1_R	-1505	-517.5	182	VCOMH	1995	-517.5
133	VSS1_R	-1435	-517.5	183	VCOMH	2065	-517.5
134	VSS1_R	-1365	-517.5	184	VCOMH	2135	-517.5
135	VSS1_R	-1295	-517.5	185	VCOMH	2205	-517.5
136	VSS1_R	-1225	-517.5	186	VCOMH	2275	-517.5
137	VSS1_R	-1155	-517.5	187	VCOML	2345	-517.5
138	VSS1	-1085	-517.5	188	VCOML	2415	-517.5
139	VSS1	-1015	-517.5	189	VCOML	2485	-517.5
140	VSS1	-945	-517.5	190	VCOML	2555	-517.5
141	VSS1	-875	-517.5	191	VCOML	2625	-517.5
142	VSS1	-805	-517.5	192	VCOML	2695	-517.5
143	VSS1	-735	-517.5	193	VR	2765	-517.5
144	VSS1	-665	-517.5	194	VR	2835	-517.5
145	VSS1	-595	-517.5	195	VR	2905	-517.5
146	VSS1	-525	-517.5	196	VR	2975	-517.5
147	VSS1	-455	-517.5	197	VR	3045	-517.5
148	VSS1	-385	-517.5	198	VR	3115	-517.5
149	VDD1	-315	-517.5	199	VR	3185	-517.5
150	VDD1	-245	-517.5	200	VR	3255	-517.5

- continued -

No	Name	X	Y	No	Name	X	Y
201	VCL	3325	-517.5	251	VSS2	6825	-517.5
202	VCL	3395	-517.5	252	VGL	6895	-517.5
203	VCL	3465	-517.5	253	VGL	6965	-517.5
204	VGH	3535	-517.5	254	VGL	7035	-517.5
205	VGH	3605	-517.5	255	VGL	7105	-517.5
206	VGH	3675	-517.5	256	VGL	7175	-517.5
207	AVDD	3745	-517.5	257	VGL	7245	-517.5
208	AVDD	3815	-517.5	258	VGL	7315	-517.5
209	AVDD	3885	-517.5	259	VGL	7385	-517.5
210	AVDD	3955	-517.5	260	VGL	7455	-517.5
211	AVDD	4025	-517.5	261	VGL	7525	-517.5
212	AVDD	4095	-517.5	262	VGL	7595	-517.5
213	AVDD	4165	-517.5	263	VGL	7665	-517.5
214	VREG_DC	4235	-517.5	264	VSS2	7735	-517.5
215	VREG_DC	4305	-517.5	265	VSS2	7805	-517.5
216	VREG_DC	4375	-517.5	266	VSS2	7875	-517.5
217	VDC1	4445	-517.5	267	VSS2_DC	7945	-517.5
218	VDC1	4515	-517.5	268	VSS2_DC	8015	-517.5
219	VDC1	4585	-517.5	269	VSS2_DC	8085	-517.5
220	VDC1	4655	-517.5	270	VSS2_DC	8155	-517.5
221	VDC1	4725	-517.5	271	VSS2_DC	8225	-517.5
222	VDD2	4795	-517.5	272	VSS2_DC	8295	-517.5
223	VDD2	4865	-517.5	273	DUMMY	8365	-517.5
224	VDD2	4935	-517.5	274	C6M	8435	-517.5
225	VDD2	5005	-517.5	275	C6M	8505	-517.5
226	VDD2_DC	5075	-517.5	276	C6M	8575	-517.5
227	VDD2_DC	5145	-517.5	277	DUMMY	8645	-517.5
228	VDD2_DC	5215	-517.5	278	C6P	8715	-517.5
229	VDD2_DC	5285	-517.5	279	C6P	8785	-517.5
230	VDD2_DC	5355	-517.5	280	C6P	8855	-517.5
231	C1M	5425	-517.5	281	DUMMY	8925	-517.5
232	C1M	5495	-517.5	282	C3M	8995	-517.5
233	C1M	5565	-517.5	283	C3M	9065	-517.5
234	C1M	5635	-517.5	284	C3M	9135	-517.5
235	C1M	5705	-517.5	285	C3P	9205	-517.5
236	C1P	5775	-517.5	286	C3P	9275	-517.5
237	C1P	5845	-517.5	287	C3P	9345	-517.5
238	C1P	5915	-517.5	288	C4M	9415	-517.5
239	C1P	5985	-517.5	289	C4M	9485	-517.5
240	C1P	6055	-517.5	290	C4M	9555	-517.5
241	C2M	6125	-517.5	291	C4P	9625	-517.5
242	C2M	6195	-517.5	292	C4P	9695	-517.5
243	C2M	6265	-517.5	293	C4P	9765	-517.5
244	C2M	6335	-517.5	294	C5M	9835	-517.5
245	C2M	6405	-517.5	295	C5M	9905	-517.5
246	C2P	6475	-517.5	296	C5M	9975	-517.5
247	C2P	6545	-517.5	297	C5P	10045	-517.5
248	C2P	6615	-517.5	298	C5P	10115	-517.5
249	C2P	6685	-517.5	299	C5P	10185	-517.5
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304	DUMMY	10745	-517.5	354	G<85>	9730	386.5
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309	DUMMY	10630	511.5	359	G<95>	9630	511.5
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408	G<193>	8650	386.5	458	G<293>	7650	386.5
409	G<195>	8630	511.5	459	G<295>	7630	511.5
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413	G<203>	8550	511.5	463	G<303>	7550	511.5
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423	G<223>	8350	511.5	473	DUMMY	7350	511.5
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425	G<227>	8310	511.5	475	S<720>	7110	386.5
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505	S<690>	6510	386.5	555	S<640>	5510	386.5
506	S<689>	6490	511.5	556	S<639>	5490	511.5
507	S<688>	6470	386.5	557	S<638>	5470	386.5
508	S<687>	6450	511.5	558	S<637>	5450	511.5
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510	S<685>	6410	511.5	560	S<635>	5410	511.5
511	S<684>	6390	386.5	561	S<634>	5390	386.5
512	S<683>	6370	511.5	562	S<633>	5370	511.5
513	S<682>	6350	386.5	563	S<632>	5350	386.5
514	S<681>	6330	511.5	564	S<631>	5330	511.5
515	S<680>	6310	386.5	565	S<630>	5310	386.5
516	S<679>	6290	511.5	566	S<629>	5290	511.5
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519	S<676>	6230	386.5	569	S<626>	5230	386.5
520	S<675>	6210	511.5	570	S<625>	5210	511.5
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523	S<672>	6150	386.5	573	S<622>	5150	386.5
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545	S<650>	5710	386.5	595	S<600>	4710	386.5
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547	S<648>	5670	386.5	597	S<598>	4670	386.5
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605	S<590>	4510	386.5	655	S<540>	3510	386.5
606	S<589>	4490	511.5	656	S<539>	3490	511.5
607	S<588>	4470	386.5	657	S<538>	3470	386.5
608	S<587>	4450	511.5	658	S<537>	3450	511.5
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610	S<585>	4410	511.5	660	S<535>	3410	511.5
611	S<584>	4390	386.5	661	S<534>	3390	386.5
612	S<583>	4370	511.5	662	S<533>	3370	511.5
613	S<582>	4350	386.5	663	S<532>	3350	386.5
614	S<581>	4330	511.5	664	S<531>	3330	511.5
615	S<580>	4310	386.5	665	S<530>	3310	386.5
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618	S<577>	4250	511.5	668	S<527>	3250	511.5
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626	S<569>	4090	511.5	676	S<519>	3090	511.5
627	S<568>	4070	386.5	677	S<518>	3070	386.5
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635	S<560>	3910	386.5	685	S<510>	2910	386.5
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637	S<558>	3870	386.5	687	S<508>	2870	386.5
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704	S<491>	2530	511.5	754	S<441>	1530	511.5
705	S<490>	2510	386.5	755	S<440>	1510	386.5
706	S<489>	2490	511.5	756	S<439>	1490	511.5
707	S<488>	2470	386.5	757	S<438>	1470	386.5
708	S<487>	2450	511.5	758	S<437>	1450	511.5
709	S<486>	2430	386.5	759	S<436>	1430	386.5
710	S<485>	2410	511.5	760	S<435>	1410	511.5
711	S<484>	2390	386.5	761	S<434>	1390	386.5
712	S<483>	2370	511.5	762	S<433>	1370	511.5
713	S<482>	2350	386.5	763	S<432>	1350	386.5
714	S<481>	2330	511.5	764	S<431>	1330	511.5
715	S<480>	2310	386.5	765	S<430>	1310	386.5
716	S<479>	2290	511.5	766	S<429>	1290	511.5
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718	S<477>	2250	511.5	768	S<427>	1250	511.5
719	S<476>	2230	386.5	769	S<426>	1230	386.5
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722	S<473>	2170	511.5	772	S<423>	1170	511.5
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725	S<470>	2110	386.5	775	S<420>	1110	386.5
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1244	G<228>	-8310	511.5	1294	G<128>	-9310	511.5
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1246	G<224>	-8350	511.5	1296	G<124>	-9350	511.5
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1303	G<110>	-9490	386.5	1353	G<10>	-10490	386.5
1304	G<108>	-9510	511.5	1354	G<8>	-10510	511.5
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1306	G<104>	-9550	511.5	1356	G<4>	-10550	511.5
1307	G<102>	-9570	386.5	1357	G<2>	-10570	386.5
1308	G<100>	-9590	511.5	1358	DUMMY	-10590	511.5
1309	G<98>	-9610	386.5	1359	DUMMY	-10610	386.5
1310	G<96>	-9630	511.5	1360	DUMMY	-10630	511.5
1311	G<94>	-9650	386.5	1361	DUMMY	-10650	386.5
1312	G<92>	-9670	511.5	1362	DUMMY	-10670	511.5
1313	G<90>	-9690	386.5				
1314	G<88>	-9710	511.5	KEY_COG		-10613	-468
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