

LC7560



3057

CMOS LSI

Graphic Equalizer LCD Driver

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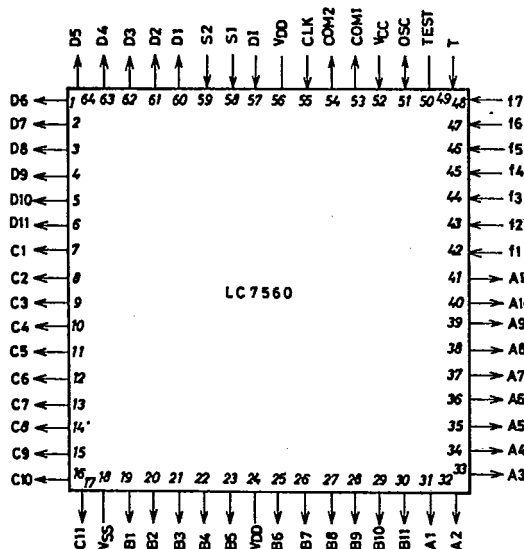
Use

LCD driver for display of graphic equalizers LC7520, 7522, 7523.

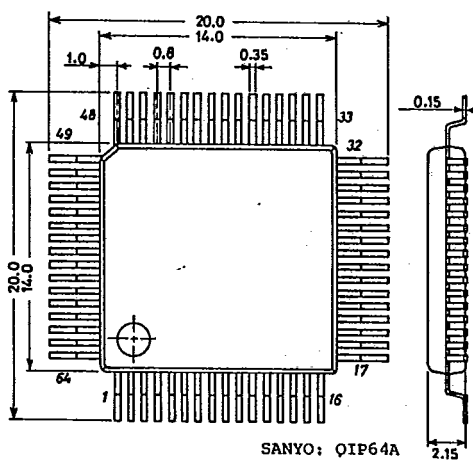
Features

- (1) 7-band display (+ accessory display or total display) : 11 x 8 segments.
 - . Display of bandpass signal strength → Spectrum analyzing display: 7 bands 2dB/step, 11-dot display
 - . Display of setting state in each band → Dot display: Flashable at the setting mode, R/L selectable
 - . Accessory display: 11 kinds of [MEMO], [M1] to [M5], [R], [L], [MIX], [LEVEL], [POSITION]. Total display also available.
- (2) In 1-chip applications, the signal strength display input is the L/R mixing input. (The mixing circuit is connected externally.)
- (3) Display unit: Dynamic drive of LCD. 1/2duty, 1/2bias (5V rating)
- (4) Bandpass filter for display: External equivalent filter.
- (5) System control: External microcomputer-controlled. Only 2 control buses.

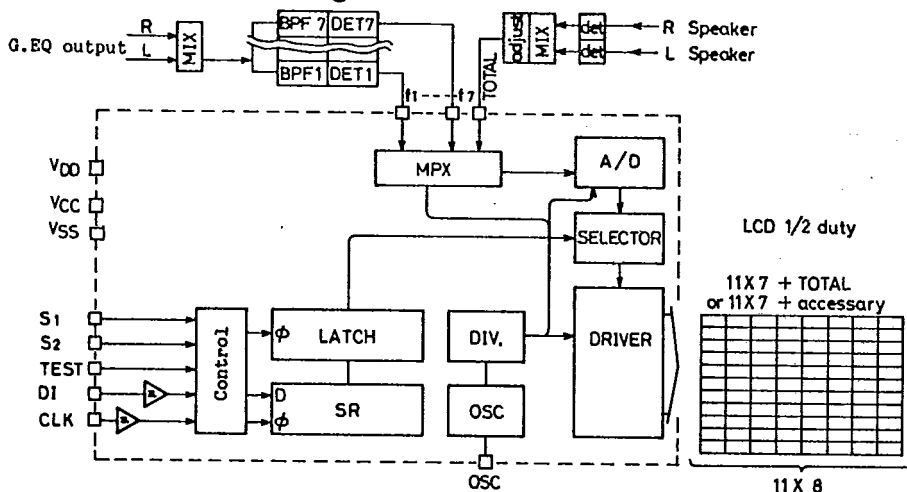
Pin Assignment



Case Outline 3057-Q64AIC (unit:mm)



Equivalent Circuit Block Diagram

Absolute Maximum Ratings at $T_a=25^{\circ}\text{C}$, $V_{SS}=0\text{V}$

				unit
Maximum Supply Voltage	$V_{DD\max}$	V_{DD}	$V_{SS}\text{to}V_{SS}+15$	V
	$V_{CC\max}$	V_{CC}	$V_{SS}\text{to}V_{SS}+7$	V
Maximum Input Voltage	$V_{I1\max}$	CLK, DI	$V_{SS}-0.3\text{to}V_{CC}+0.3$	V
	$V_{I2\max}$	f1to7, T, TEST, S1, S2	$V_{SS}-0.3\text{to}V_{DD}+0.3$	V
Maximum Output Voltage	$V_{O\max}$	A1toA11, B1toB11, COM1	$V_{SS}-0.3\text{to}V_{CC}+0.3$	V
		C1toC11, D1toD11, COM2		
Allowable Power Dissipation	$P_{d\max}$	$T_a\geq 75^{\circ}\text{C}$	200	mW
Operating Temperature	T_{opg}		-30 to +75	$^{\circ}\text{C}$
Storage Temperature	T_{stg}		-40 to +125	$^{\circ}\text{C}$

Allowable Operating Conditions at $T_a=25^{\circ}\text{C}$, $V_{SS}=0\text{V}$

			min	typ	max	unit
Supply Voltage	V_{DD}	V_{DD} C of 0.1 μF or greater must be connected.	7.5	13.0	14.0	V
Input 'H'-Level Voltage	V_{IH1}	V_{CC} CLK, DI	4.0	5.0	5.5	V
	V_{IH2}	S1, S2	0.8 V_{CC}		V_{CC}	V
Input 'L'-Level Voltage	V_{IL1}	CLK, DI	0.9 V_{DD}		V_{DD}	V
	V_{IL2}	S1, S2	V_{SS}	0.2 V_{CC}		V
Input Pulse Width	$t_{\phi W}$	CLK	V_{SS}	0.1 V_{DD}		V
Setup Time	t_{setup}	DI	1			us
Hold Time	t_{hold}	DI	1			us
External CR	R_{osc}	OSC		75		kohm
	C_{osc}	OSC	0.0033			μF

Electrical Characteristics at $T_a=25^{\circ}\text{C}$, $V_{SS}=0\text{V}$

			min	typ	max	unit
Input Sensitivity	V_{in}	f1to7, T; $V_{DD}=13\text{V}$, 0dB, lighted, Test Circuit #1		1.6		V
A/D Conversion Error	ΔB	f1to7, T; $V_{DD}=13\text{V}$, to 2dB step, Test Circuit #1	-1		1	dB
Current Dissipation	I_{DD}	V_{DD}			7	mA
	I_{CC}	V_{CC}			1	mA
Input OFF Leak Current	I_{off}	f1 to 7, T			10	μA
Output 'H'-Level Voltage	V_{OH}	A1 to 11, B1 to 11, COM1, C1 to 11, D1 to 11, COM2	0.8 V_{CC}		V_{CC}	V

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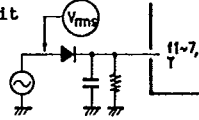
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Output 'L'-Level Voltage V_{OL} A1 to 11, B1 to 11, COM1,
C1 to 11, D1 to 11, COM2min typ max unit
 V_{SS} 0.2 V_{CC} VOutput 'M'-Level Voltage V_{OM}

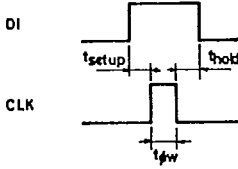
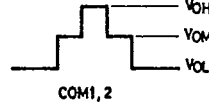
COM1,2 *2

 $1/2 V_{CC}$
10V
kohmOutput Impedance Z_O A1 to 11, B1 to 11, COM1,
C1 to 11, D1 to 11, COM2

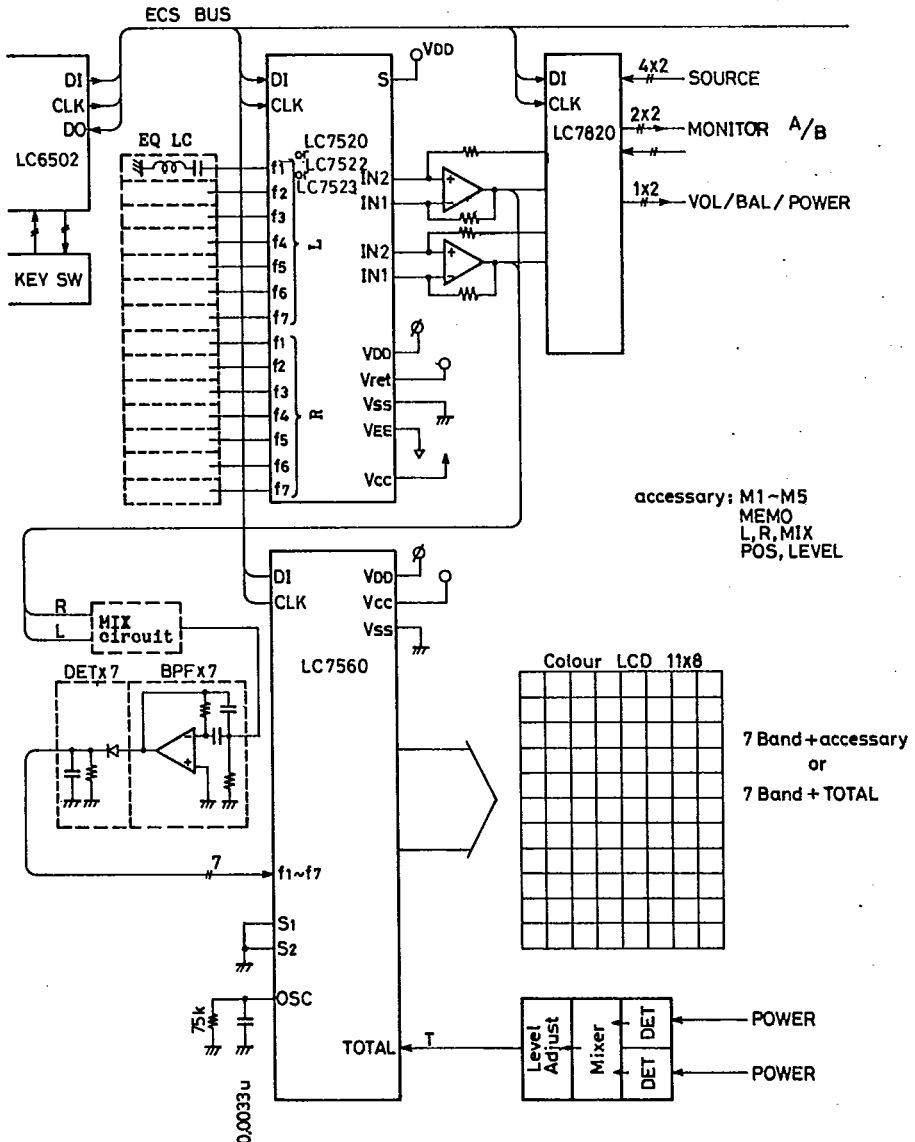
*1 Test Circuit



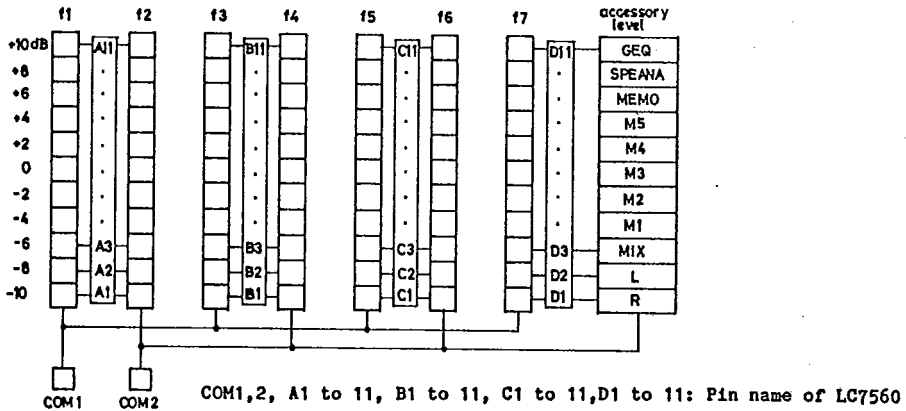
*2

**Sample Application Circuit****7-Band MIX Display**

(LC7520 x 1, LC7560 x 1 or LC7522 x 1, LC7560 x 1 or LC7523 x 1, LC7560 x 1)



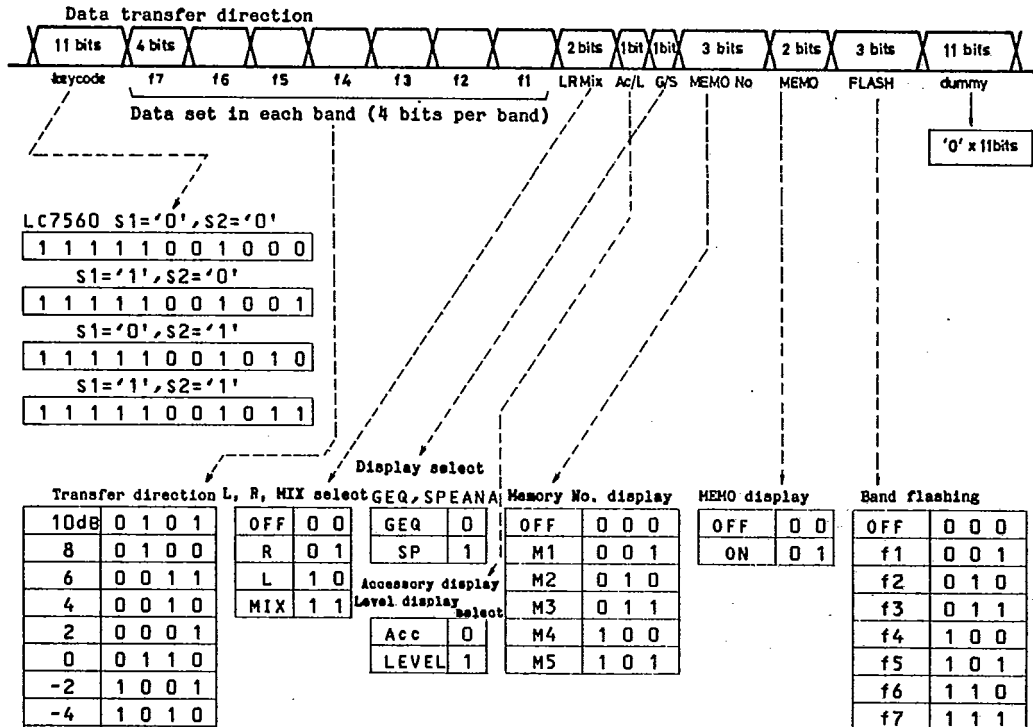
Segment Assignment



The following restrictions are imposed on accessory display.

- (1) All of R, L, MIX are unlighted or one of them is lighted.
- (2) All of M1 to 5 are unlighted or one of them is lighted.
- (3) MEMO can be turned ON/OFF independently.
- (4) Either GEQ or SPEANA is lighted. Lighting of GEQ/SPEANA is synchronized with the setting dot mode/spectrum analyzing mode respectively.


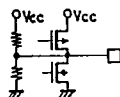
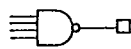
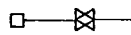
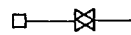
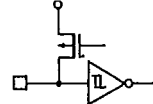
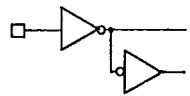
Data Code



Note 1. When power is applied, data "0" must be first transferred for 51 clocks (initial clock) or more. If data transfer is stopped halfway, the transfer of the remaining data must be completed or data transfer must be started after the initial clocks have been transferred.

Note 2. When the DI, CLK pins are shared with the LC7520, etc., the maximum initial clocks for such device must be transferred.

Pin Description

Pin Name	Pin No.	Pin Configuration	Description															
V _{DD}	24, 56		Power supply pin, +13V _{typ.} , Power supply for A/D conversion															
V _{CC}	52		Power supply pin, +5V, power supply for logic drive															
V _{SS}	18		Power supply pin, 0V															
DI	57		• Used to input data from CPU • Schmitt inverter type															
CLK	55		• Used to input CLK from CPU • Schmitt inverter type															
COM1 COM2	53 54		• Output pin to LCD common															
A1 to 11	31 to 41		• Output pin to LCD segment • Bands f1, f2															
B1 to 11	19 to 23 25 to 30		• Output pin to LCD segment • Bands f3, f4															
C1 to 11	7 to 17		• Output pin to LCD segment • Bands f5, f6															
D1 to 11	60 to 64 1 to 6		• Output pin to LCD segment • Band f7, total display or accessory display															
f1 to f7	42 to 48		• Used to input detection output of audio signal															
T	49		• Input pin for total display • Used to input detection output															
OSC	51		• Open drain type output buffer • Used to connect external CR for OSC															
S1,S2	58,59		• Select pin in applications where a plurality of chips (4 pcs. max.) are used <table data-bbox="622 1103 910 1247"><tr><th>S2</th><th>S1</th><th>Key code</th></tr><tr><td>1</td><td>1</td><td>7CB</td></tr><tr><td>1</td><td>0</td><td>7CA</td></tr><tr><td>0</td><td>1</td><td>7C9</td></tr><tr><td>0</td><td>0</td><td>7C8</td></tr></table>	S2	S1	Key code	1	1	7CB	1	0	7CA	0	1	7C9	0	0	7C8
S2	S1	Key code																
1	1	7CB																
1	0	7CA																
0	1	7C9																
0	0	7C8																
TEST	50		• IC test pin • Open during operation															