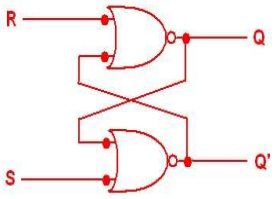
S	R	Q	Q'	Remarks
0	0	NC	NC	No Change
0	1	0	1	Reset
1	0	1	0	Set
1	1	Illegal	Illegal	Illegal

Characteristic Table for RS Latch



A Basic SR Latch

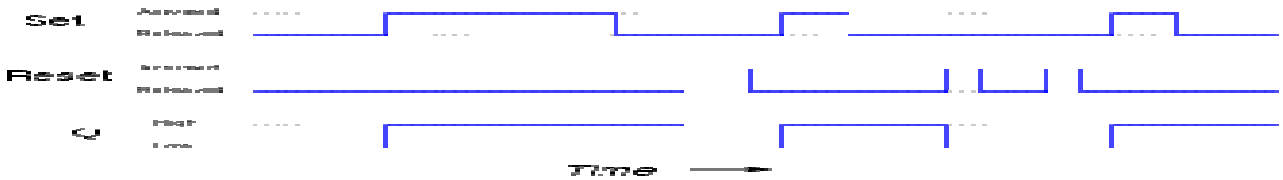
http:elprojects.blogspot.com

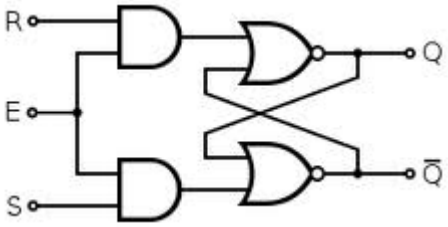
S-R Latch:

When Q=0 & Q'=1 latch is in reset state

When Q=1 & Q'=0 latch is in set state

This is bistable 2 stable states



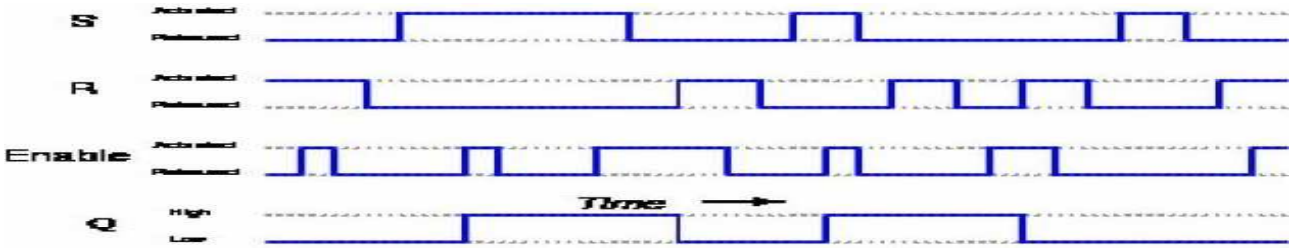


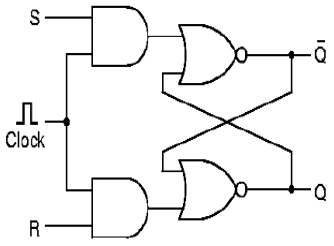
E	S	R	Q	Q̄
0	0	0	Latch	
0	0	1	Latch	
0	1	0	Latch	
0	1	1	Latch	
1	0	0	Latch	
1	0	1	0	1
1	1	0	1	0
1	1	1	0	0

Gated S-R Latch

When enabled input is low the S & R inputs are ignored.

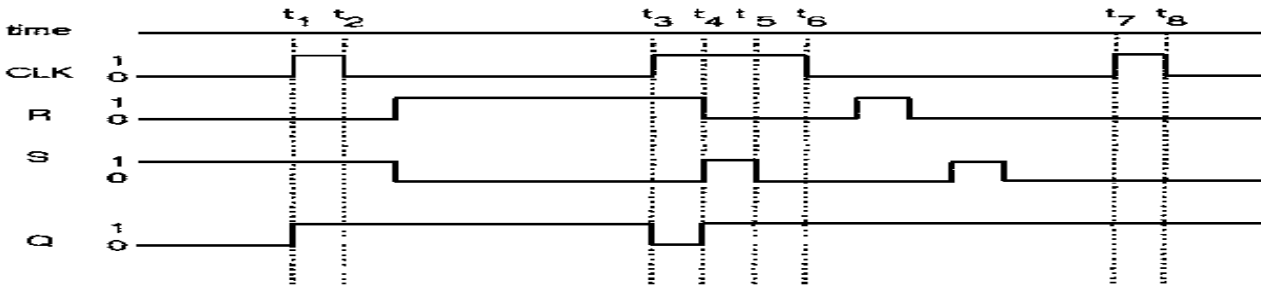
When enabled input is high the output is controlled by S & R inputs.

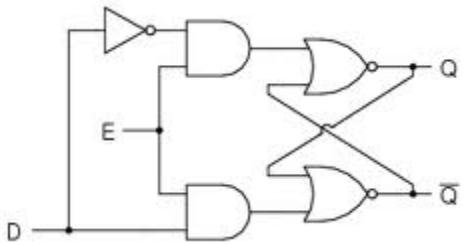




Inputs			Outputs		
S	R	C	Q	Q̄	Comments
0	0	X	Q_0	$\bar{Q}_0$	No Change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	?	?	Invalid

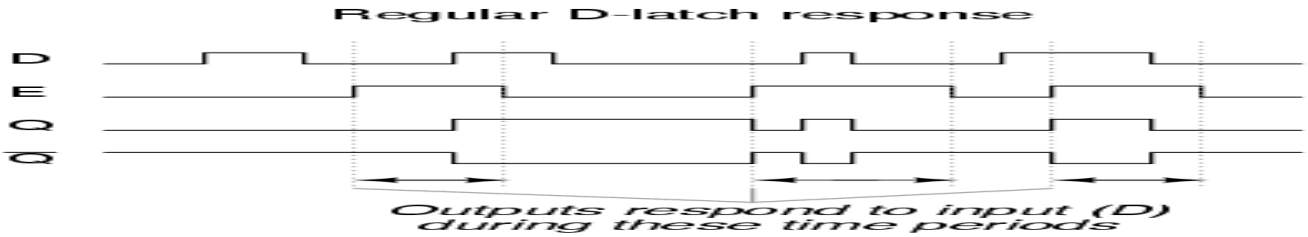
The edge triggered s-r flipflop. The inputs s &r are called synchronous inputs. The data on these inputs are only transferred to the outputs on the triggering edge of the clock pulse.

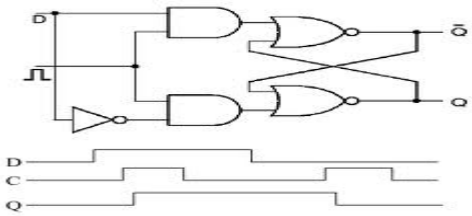




E	D	Q	$\overline{Q}$
0	0	latch	latch
0	1	latch	latch
1	0	0	1
1	1	1	0

When D is HIGH and E is HIGH the latch is set
When D is LOW and E is HIGH the latch is reset



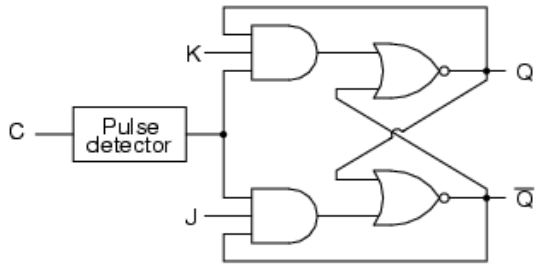


if D is HIGH when clock is applied it is in set state

if D is LOW when clock is applied it is in reset state

Function Table

INPUTS		OUTPUTS
CLK	D	Next state of Q
0	X	No change
1	0	Q = 0; Reset state
1	1	Q = 1; Set state



C	J	K	Q	$\overline{Q}$
⎍	0	0	latch	latch
⎍	0	1	0	1
⎍	1	0	1	0
⎍	1	1	toggle	toggle
x	0	0	latch	latch
x	0	1	latch	latch
x	1	0	latch	latch
x	1	1	latch	latch

J-K has no invalid state