HYCON TECHNOLOGY

HY3106/HY3104/HY3102
Datasheet
24-Bit Analog-to-Digital Convert
High Resolution ΣΔADC

Table of Contents

Attention：

1. HYCON Technology Corp. reserves the right to change the content of this datasheet without further notice. For most up-to-date information, please constantly visit our website: http://www.hycontek.com .
2. HYCON Technology Corp. is not responsible for problems caused by figures or application circuits narrated herein whose related industrial properties belong to third parties.
3. Specifications of any HYCON Technology Corp. products detailed or contained herein stipulate the performance, characteristics, and functions of the specified products in the independent state. We does not guarantee of the performance, characteristics, and functions of the specified products as placed in the customer's products or equipment. Constant and sufficient verification and evaluation is highly advised.
4. Please note the operating conditions of input voltage, output voltage and load current and ensure the IC internal power consumption does not exceed that of package tolerance. HYCON Technology Corp. assumes no responsibility for equipment failures that resulted from using products at values that exceed, even momentarily, rated values listed in products specifications of HYCON products specified herein.
5. Notwithstanding this product has built-in ESD protection circuit, please do not exert excessive static electricity to protection circuit.
6. Products specified or contained herein cannot be employed in applications which require extremely high levels of reliability, such as device or equipment affecting the human body, health/medical equipments, security systems, or any apparatus installed in aircrafts and other vehicles.
7. Despite the fact that HYCON Technology Corp. endeavors to enhance product quality as well as reliability in every possible way, failure or malfunction of semiconductor products may happen. Hence, users are strongly recommended to comply with safety design including redundancy and fire-precaution equipments to prevent any accidents and fires that may follow.
8. Use of the information described herein for other purposes and/or reproduction or copying without the permission of HYCON Technology Corp. is strictly prohibited.

1. Features

- Designed to process pre-signal of bridge sensors
- Built-in programmable gain amplifier (PGA) with gain of 1, 2, 4, 8, 16, 32, 64 and 128
- Operation clock switch selections: external crystal oscillator or internal high precision RC oscillator
- Data output rate: 10, 80, 640 or 2560SPS selection
- Built-in temperature sensor
- Simultaneous 50 / 60 Hz rejection at 10SPS
- RMS Noise :
  50nV (Gain=128) at 10SPS output rate
  150nV (Gain=128) at 80SPS output rate
- Selectable reference input buffer
- SPI interface
- SSOP16 package
- Built-in VDDA regulator, Off, 2.4V 2.7V, 3.0V or 3.3V voltage selection
- Supply range: 2.4V to 3.6V
- Temperature range: –40°C to +85°C
- Built-in DC bias, 0,±1/8, ±1/4, ±3/8, ±1/2, ±5/8, ±3/4, ±7/8 VREF bias voltage selection
- Low Sleep current, aprox.0.65uA (ENADC = 0)
- Built-in 4 switchable signal input modes.
- Operation Current :
  950uA@Gain=64,128;
  300uA@Gain= 1, 2, 4.

Model No.	Architecture	Input Channels	EONB (Bits)	RMS Noise	System Clock	Sample Rate(Max)	Built-In Temp. Sensor	DC Offset Set	Interface	Package
HY3102	Sigma-Delta	2	21	50nV (10SPS)	Int. 320kHz	2560SPS	YES	4 bits	SPI	SSOP 16
HY3104	Sigma-Delta	2	21	50nV (10SPS)	Int. 320kHz Ext.4.9152MHz	2560SPS	YES	4 bits	SPI	SSOP 16
HY3106	Sigma-Delta	4	21	50nV (10SPS)	Int. 320kHz Ext.4.9152MHz	2560SPS	YES	4 bits	SPI	SSOP 16

2. Application

- Weight Scales
- Strain Gauges
- Pressure Scales
- Industrial Process Control

3. Brief Description

HY310x (HY3106/HY3104/HY3102) is a high precision, low power 24-bit Analog-to-Digital Convertor (ADC). The built-in ultra low-noise programmable gain amplifier (PGA) has 21-bit effective number of bits (ENOB) (gain=1). The minimum signal resolution is 50nV (gain=128). Minimum supply voltage of the chip is 2.4V, current consumption is 950μA and sleep current is 0.65μA. HY3106/HY3104 can be clocked by the internal RC oscillator or an external clock source. HY3106 has two sets of analog signal inputs. The whole series chips are designed to process pre-signal of bridge sensor applications, including weight scale, strain gauge, pressure scale and industrial process control.

Ultra low-noise PGA has a gain of 8, 16 or 32. Based on diverse signal sizes, the maximum gain is 128 (with collocation of ADC gain 1, 2 & 4). Voltage reference (REFP–REFN) has multiple 1 or 1/2 selection. It can support full-scale differential input of ±1.28V, ±640mV, ±320mV, ±160mV, ±80mV, ±40m, ±20mV and ±10mV. The chip can select different output rate at 10SPS (50/60 Hz rejection), 80SPS, 640SPS and 2560SPS. Four signal input modes are used to deduct offset. There are 8 selection of DC bias 0, ±1/8, ±1/4, ±3/8, ±1/2, ±5/8, ±3/4 and ±7/8 VREF. The built-in VDDA regulator has off, 2.4, 2.7, 3.0 or 3.3V selection. An internal temperature sensor performs single point calibration with a deviation range under +/- 2℃.

HY310x data transmits through a built-in SPI module. Internally, there is an 8-bit readable/writable system control and a 16-bit readable/writable ADC control register. ADC data outputs from a 24-bit COMB Filter Buffer. The HY310X can be activated or kept in sleep mode via writing register bit (ENADC).

HY310x is available in a SSOP–16 package and is specified from -40℃ to 85℃.

4. Pin Definition

4.1. SSOP16 Pin Diagram

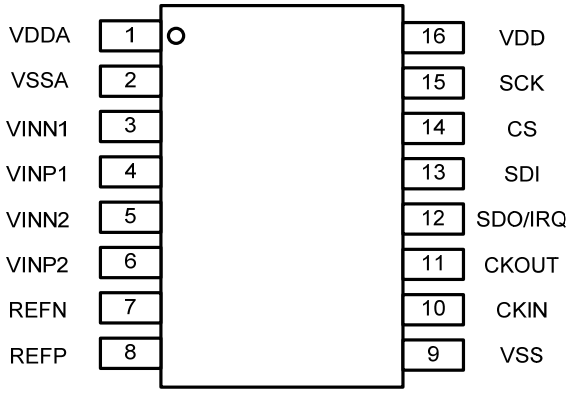


Figure 1 HY3106 SSOP16 Pin Diagram

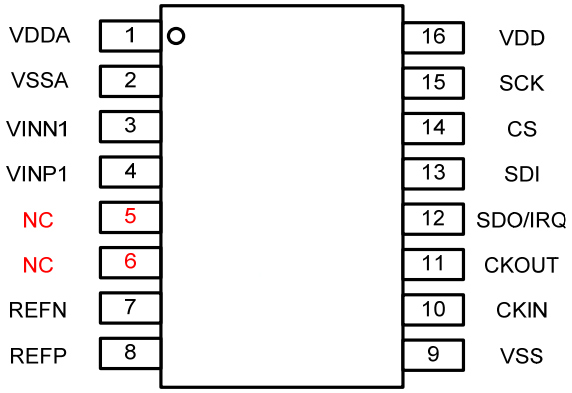


Figure 2 HY3104 SSOP16 Pin Diagram

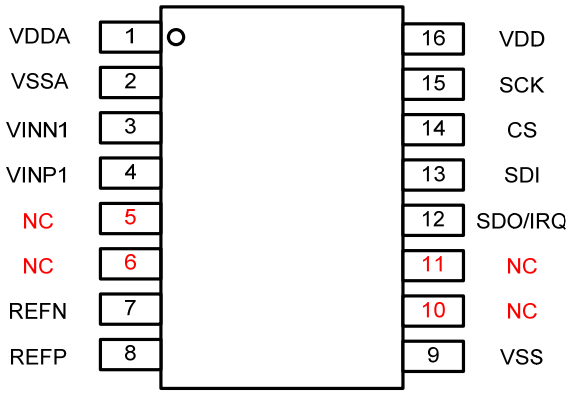


Figure 3 HY3102 SSOP16 Pin Diagram

4.2. I/O Pin Definition（SSOP16）

"I" input, "O" output, "S" Smith Trigger, "P" power supply, "A" analog channel

No.	Pin Name	Pin Characteristics		Function Description
		Type	Buffer	
1	VDDA	P	P	Analog Power Supply: 2.4~3.6V
2	VSSA	P	P	Analog Ground
3	VINN1	I	A	Analog Input1 (Negative)
4	VINP1	I	A	Analog Input1 (Positive)
5	VINN2	I	A	Analog Input2 (Negative)
6	VINP2	I	A	Analog Input2 (Positive)
7	REFN	I	A	Reference Input (Negative)
8	REFP	I	A	Reference Input (Positive)
9	VSS	P	P	Digital Ground
10	CKIN	I	A	External oscillator input
11	CKOUT	O	A	External oscillator output
12	SDO/IRQ	O	S	SPI Data Output
13	SDI	I	S	SPI Data Input
14	CS	I	A	SPI Chip select Input
15	SCK	I	A	SPI Clock Input
16	VDD	P	P	Digital Power Supply: 2.4~3.6V

Table 1 Pin Definition and Function Description

5. Application Circuit

5.1. Bridge Sensor

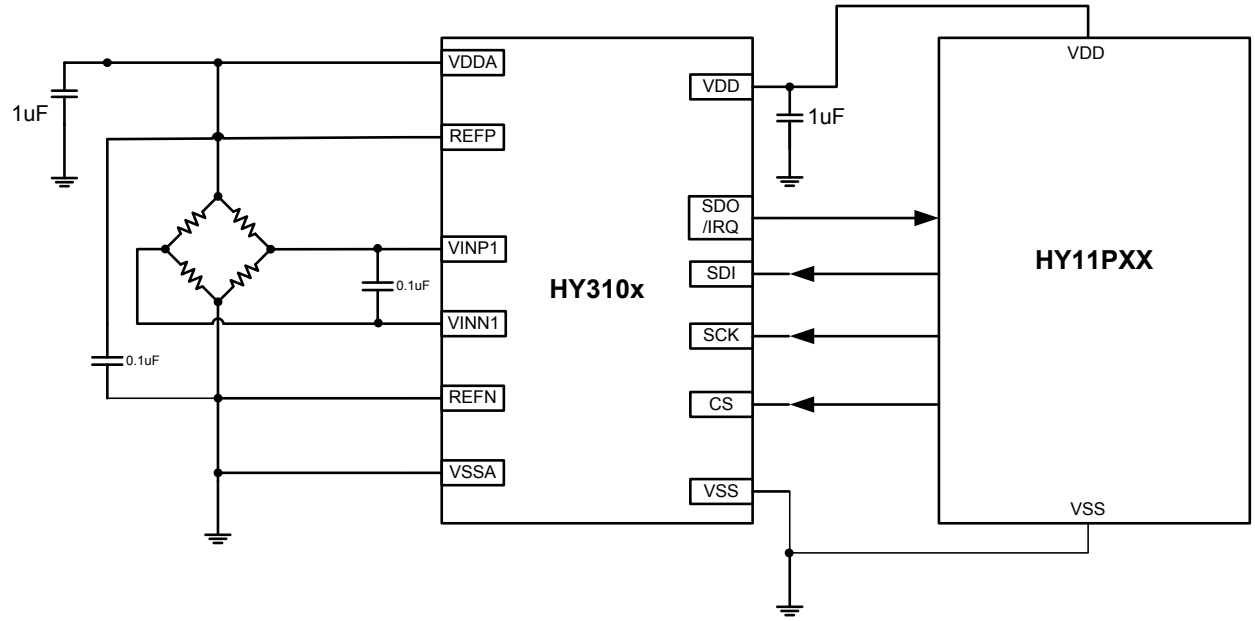


Figure 4 Application Circuit of Bridge Sensor

6. Register List

6.1. Register List

Register								
	SYS[7:0]							
Description	System Configuration							
Address	000							
Name	INOSC	LDO[1]	LDO[0]	ENLDO	REFOS	SDOH	CH	TS
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Status	0	0	0	0	0	1	0	0

Register								
	ADC[15:8]							
Description	ADC Control Register							
Address	001							
Name	DCSET[3]	DCSET[2]	DCSET[1]	DCSET[0]	INX[1]	INX[0]	ADGN[1]	ADGN[0]
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Status	0	0	0	0	0	0	0	0

Register								
	ADC[7:0]							
Description	ADC Control Register							
Address	001							
Name	PGA[2]	PGA[1]	PGA[0]	FRb	OSR[1]	OSR[0]	ENRB	ADCEN
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Status	0	0	0	0	0	0	0	0

Register	
	ADO0[23:0]
Description	ADC channel 1 measured date
Address	010
Initial Status	X
Read/Write	R

Register	
	ADO1[23:0]
Description	ADC channel 2 measured data
Address	100
Initial Status	X
Read/Write	R

Register	
	TSO[15:0]
Description	Temperature sensor measured data
Address	110
Initial Status	X
Read/Write	R

6.2. Register Description

SYS Register : System configuration control register (8bit)

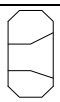
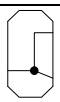
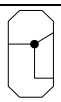
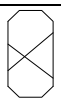
- INOSC : Oscillator source select
  - 0 : External oscillator
  - 1 : Internal oscillator
- LDO[1:0] : LDO output voltage selection
  - 00 : 3.3V
  - 01 : 3.0V
  - 10 : 2.7V
  - 11 : 2.4V
- ENLDO : Enable LDO control
  - 0 : Disable
  - 1 : Enable
- REFOS : Reference voltage selection
  - 0 : Disable
  - 1 : Enable
- SDOH : Enable SDO Pull High
  - 0 : Disable
  - 1 : Enable
- CH : ADC channel input select
  - 0 : Measure Vinp1 – Vinn1
  - 1 : Measure Vinp2 – Vinn2
- TS : Measure temperature sensor
  - 0 : Disable
  - 1 : Enable

ADC Register : ADC configuration control register (16bit)

- DCSET[3:0] : DC offset input voltage selection (VREF = REFP-REFN)
  - 0000 : 0 VREF
  - 0001 : +1/8 VREF
  - 0010 : +1/4 VREF
  - 0011 : +3/8 VREF
  - 0100 : +1/2 VREF
  - 0101 : +5/8 VREF
  - 0110 : +3/4 VREF
  - 0111 : +7/8 VREF
  - 1000 : 0 VREF
  - 1001 : -1/8 VREF
  - 1010 : -1/4 VREF

1011 : -3/8 VREF
1100 : -1/2 VREF
1101 : -5/8 VREF
1110 : -3/4 VREF
1111 : -7/8 VREF

INX[1:0] : Input voltage multiplexer
00 : Input no change
01 : Both of ADC input connects to VINN
10 : Both of ADC input connects to VINP
11 : input switch connection

INX[1:0]	00	01	10	11
Connection				

ADGN[1:0] : Input signal gain for modulator
00 : Gain = 1
01 : Gain = 2
10 : Gain = 3
11 : Gain = 4

PGA[2:0] : Input signal gain for modulator
000 : PGA Disable
001 : PGA Gain = 8
010 : Reserved
011 : PGA Gain = 16
100 : Reserved
101 : PGA Gain = 24
110 : Reserved
111 : PGA Gain = 32

FRb : Full reference range select
0 : Full reference range input
1 : 1/2 reference range input

OSR[1:0] : ADC output rate select
00 : 10SPS
01 : 80SPS
10 : 640SPS
11 : 2560SPS

ENRB : Enable reference buffer
0 : Disable
1 : Enable

ADCEN	:	ADC control
0	:	Disable
1	:	Enable

7. Electrical Characteristics

7.1. Absolute Maximum Ratings

Description	HY310x	UNIT
VDDA to VSSA	–0.3 to +3.6	V
VDD to VSS	–0.3 to +3.6	V
VSSA to VSS	–0.3 to +0.3	V
Input Current	100, Momentary	mA
	10, Continuous	mA
Analog Input Voltage to VSSA	–0.3 to VDDA + 0.3	V
Digital Input Voltage to VSS	–0.3 to VDD + 0.3	V
Maximum Junction Temperature	+150	°C
Operating Temperature Range	–40 to +85	°C
Storage Temperature Range	–60 to +150	°C

7.2. Electrical Characteristics

All specifications at TA = –40°C to +85°C, VDDA = VDD = REFP = +3V, REFN = VSSA, and PGA*Gain=128, unless otherwise noted.

PARAMETER	CONDITIONS	HY310x MIN	HY310x TYP	HY310x MAX	UNIT
Analog Inputs					
Full-Scale Input Voltage (VINP – VINN)	VREF =VDDA,		±0.5*VREF/(PGA*Gain)		V
Full-Scale Input Voltage (VINP – VINN)	VDDA=3.3V, VREF =1V,		±0.9*VREF/(PGA*Gain)		V
Negative Signal Input (VINN)		VSSA-0.1		VDDA	V
Positive Signal Input (VINP)		VSSA-0.1		VDDA	V
Common-Mode Input Range		VSSA-0.1		VDDA	V
System Performance					
Resolution	No Missing Codes		24		Bits
Data Rate	Internal Oscillator, SPEED = High		80		SPS
	Internal Oscillator, SPEED = Low		10		SPS
	External Oscillator, SPEED = High		f_{CLK}/61440		SPS
	External Oscillator, SPEED = Low		f_{CLK}/491520		SPS
Digital Filter Settling Time	Full Settling		4		Conversions
Integral Nonlinearity (INL)	Differential Input, End-Point Fit, G = 1, VIN=0.9*VR, delta VR~1.24V		10		ppm
Input Offset Error	Gain=1,		±50		ppm of FS
	Gain=128,		±3		ppm of FS
Input Offset Drift	Gain=1		1		uV/°C
	Gain=128,		10		nV/°C
Gain Drift	Reference Buffer off, Input common voltage=VDDA/2		5		ppm/°C
Normal-Mode Rejection	fIN = 50Hz or 60Hz ±1Hz, fDATA = 10SPS, External Oscillator(1)		90		dB
Common-Mode Rejection	at DC, Voltage=VDDA/2± 0.1V		80		dB
Input-Referred Noise	fDATA = 10SPS , Gain=128,		50		nV, rms
	fDATA = 80SPS , Gain=128,		150		nV, rms
Power-Supply Rejection	at DC,VDDA=3V±0.1V, Gain=1		80		dB
	at DC,VDDA=3V±0.1V, Gain=128		120		dB
Voltage Reference Input					
Voltage Reference Input (VREF)	VREF = REFP – REFN			VDDA	V

Negative Reference Input (REFN)			VSS-0.1	VDDA/2	V
Positive Reference Input (REFP)			VDDA/2	VDDA+0.1	V
Voltage Reference Input Current (Input buffer on)			10		nA
Digital					
Logic Levels	VIH	All digital inputs except CLKIN	0.7 VDD	VDD + 0.1	V
		CLKIN	0.7 VDD	3.7	V
	VIL		VSS	0.2 VSS	V
	VOH	IOH = 1mA	VDD – 0.4		V
	VOL	IOL = 1mA		0.2 VDD	V
Input Leakage		0 < VIN < VDD	0.1		nA
External Clock Input Frequency (fCLKIN)			4.9152		MHz
Serial Clock Input Frequency (fSCLK)				5	MHz
(1). HY3102 does not support external oscillator function.					

All specifications at VDD=VDDA, Internal Oscillator enable, unless otherwise noted.

PARAMETER	CONDITIONS	HY310x			UNIT
		MIN	TYP	MAX	
Power Supply					
Power-Supply Voltage (VDDA, VDD)		2.4		3.6	V
Analog Supply Current	Normal Mode, VDDA=2.4V, Gain=1		185		μA
	Normal Mode, VDDA=2.4V, Gain=128		730		μA
	Normal Mode, VDDA=3.0V, Gain=1		195		μA
	Normal Mode, VDDA=3.0V, Gain=128		770		μA
	Normal Mode, VDDA=3.6V, Gain=1		200		μA
	Normal Mode, VDDA=3.6V, Gain=128		800		μA
	Power-Down, VDDA=2.4V		10		μA
	Power-Down, VDDA=3.6V		15		μA
	Internal LDO (ENLDO=1)		45		μA
	Reference input buffer (ENRB=1)		45		μA
Digital Supply Current	Normal Mode, VDD = 2.4V		90		μA
	Normal mode, VDD = 3.6V		130		μA
	Power-Down, SCLK = High,VDD = 2.4V		0.6		μA
	Power-Down, SCLK = High,VDD = 3.6V		0.75		μA

8. ΣΔADC Noise Performance

HY310X offers essential input noise performance of ΣΔADC. Table 5 points out the relations between typical noise performance and gain, output rate and single end maximum input voltage. Test conditions are configured as external input signal short, 1.2V voltage reference and sampling 1024 data records.

ΣΔADC Noise Performance with Output rate/GAIN at VDDA=2.4V, VREF=1.2V										
Output rate (sps)	Max. Vin(mV) =0.9*VREF (1)	Gain	=	PGA	×	ADGN	ENOB (RMS Bit)	RMS Noise (uV)	Noise Free (Bit)	PEAK-TO-PEAK Noise (uV)
10	±1080	1	=	1	×	1	20.69	1.466	18.19	8.222
	±540	2	=	1	×	2	20.70	0.703	18.09	4.324
	±270	3	=	1	×	3	20.53	0.527	17.96	3.136
	±135	4	=	1	×	4	20.43	0.423	17.91	2.436
	±68	8	=	8	×	1	20.54	0.196	17.91	1.224
	±34	16	=	16	×	1	20.92	0.087	18.38	0.496
	±17	24	=	24	×	1	20.20	0.083	17.63	0.493
	±540	32	=	32	×	1	20.08	0.068	17.55	0.389
	±270	48	=	24	×	2	19.61	0.063	16.98	0.387
	±135	64	=	32	×	2	19.44	0.053	16.72	0.346
	±68	72	=	24	×	3	19.15	0.057	16.52	0.357
	±34	96	=	32	×	3	18.89	0.051	16.26	0.318
	±8	128	=	32	×	4	18.52	0.050	15.97	0.291
80	±1080	1	=	1	×	1	19.14	4.165	16.47	26.477
	±540	2	=	1	×	2	19.14	2.067	16.41	13.881
	±270	3	=	1	×	3	18.98	1.544	16.37	9.475
	±135	4	=	1	×	4	18.86	1.262	16.25	7.722
	±68	8	=	8	×	1	19.02	0.562	16.36	3.559
	±34	16	=	16	×	1	18.84	0.320	16.30	1.851
	±17	24	=	24	×	1	18.73	0.229	16.13	1.396
	±540	32	=	32	×	1	18.60	0.189	15.98	1.161
	±270	48	=	24	×	2	18.09	0.179	15.50	1.076
	±135	64	=	32	×	2	17.88	0.155	15.43	0.850
	±68	72	=	24	×	3	17.60	0.167	14.98	1.028
	±34	96	=	32	×	3	17.40	0.144	14.73	0.921
	±8	128	=	32	×	4	17.06	0.137	14.43	0.850
640	±1080	1	=	1	×	1	17.70	11.220	15.06	70.065
	±540	2	=	1	×	2	17.58	6.118	14.99	36.811
	±270	3	=	1	×	3	17.51	4.275	14.97	25.001
	±135	4	=	1	×	4	17.31	3.677	14.65	23.311
	±68	8	=	8	×	1	17.46	1.655	14.79	10.623
	±34	16	=	16	×	1	17.27	0.951	14.58	6.122
	±17	24	=	24	×	1	17.25	0.639	14.65	3.876
	±540	32	=	32	×	1	17.05	0.552	14.47	3.300
	±270	48	=	24	×	2	16.55	0.519	13.95	3.157
	±135	64	=	32	×	2	16.41	0.428	13.87	2.499
	±68	72	=	24	×	3	16.16	0.455	13.62	2.646
	±34	96	=	32	×	3	15.93	0.401	13.30	2.480
	±8	128	=	32	×	4	15.52	0.398	12.79	2.651
2560	±1080	1	=	1	×	1	16.21	31.686	13.48	212.248
	±540	2	=	1	×	2	16.05	17.600	13.26	122.420
	±270	3	=	1	×	3	16.07	11.640	13.46	70.846
	±135	4	=	1	×	4	15.95	9.444	13.27	60.938
	±68	8	=	8	×	1	16.03	4.482	13.38	27.995
	±34	16	=	16	×	1	15.93	2.395	13.29	15.017
	±17	24	=	24	×	1	15.82	1.729	13.04	11.896
	±540	32	=	32	×	1	15.85	1.266	13.27	7.617
	±270	48	=	24	×	2	15.44	1.119	12.65	7.796
	±135	64	=	32	×	2	15.27	0.944	12.64	5.864
	±68	72	=	24	×	3	15.04	0.989	12.49	5.808
	±34	96	=	32	×	3	14.83	0.852	12.31	4.903
	±8	128	=	32	×	4	14.46	0.826	11.92	4.810

(1) Max.Vin (mV) is the max. input voltage of single end to analog ground (AVSS).

Table 5 ΣΔADC Noise Performance Table

The RMS Noise and Peak-to-Peak noise are referred to the noise generated from the chip itself at the input end. RMS Noise is ADC input noise and the Peak-to-Peak noise referring in this spec is the deviation of maximum and minimum noise of 1024 records (±3.3 standard deviation).

The Effective Number of Bits (ENOB (RMS)) is defined as:

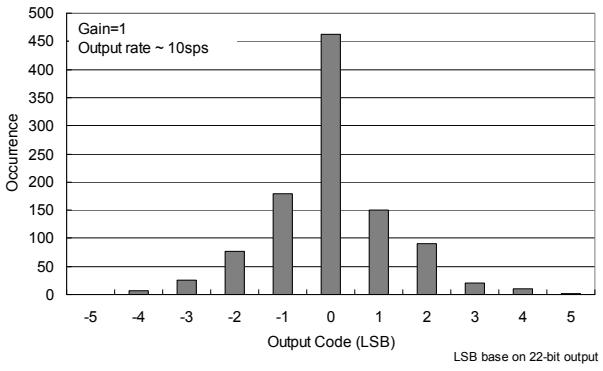
$$ENOB(RMS) = \frac{\ln\left(\frac{FSR}{RMS\ Noise}\right)}{\ln(2)}$$

$$RMS\ Noise = \frac{\left(2 \times VREF \times \sqrt{\sum_{k=1}^{1024}(ADO[k] - Average)^2}\right)}{2^{24}}$$

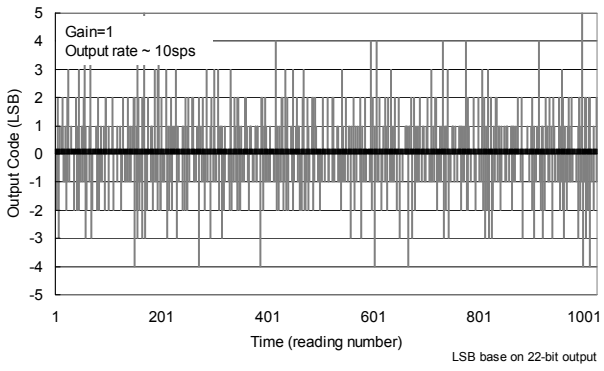
$$\text{Where } FSR\ (Full\text{-}Scale\ Range) = 2 \times VREF/Gain.$$

$$Average = \frac{\sum_{k=1}^{1024}(ADO[k])}{1024}$$

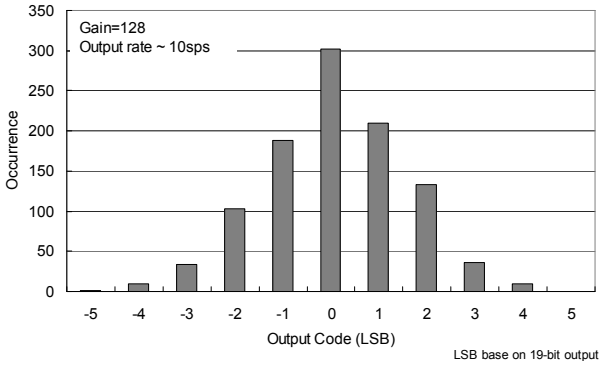
RMS Noise Diagram



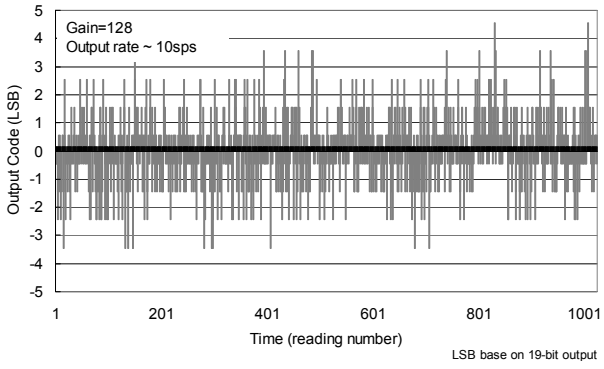
RMS Noise Diagram

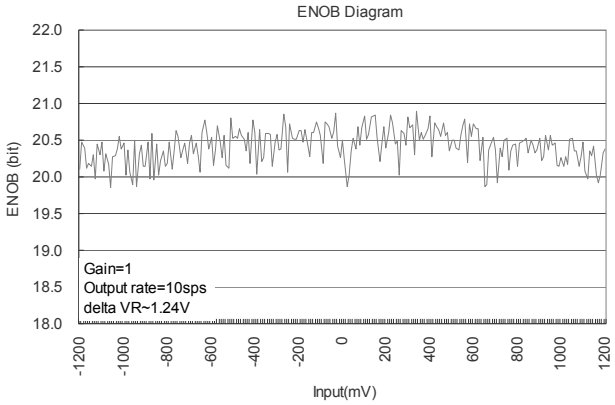


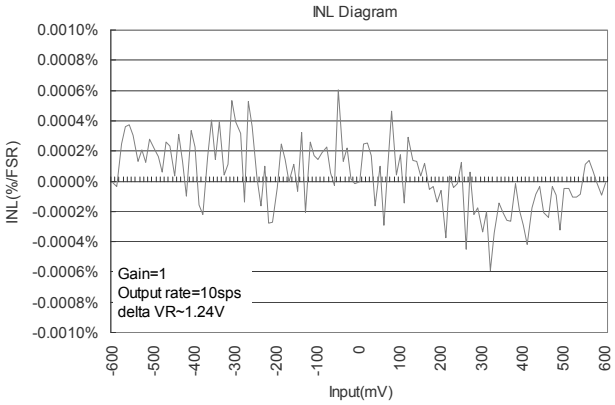
RMS Noise Diagram



RMS Noise Diagram




ENOB Diagram
ENOB (bit)
22.0
21.5
21.0
20.5
20.0
19.5
19.0
18.5
18.0
Gain=1
Output rate=10sps
delta VR~1.24V
-1200
-1000
-800
-600
-400
-200
0
200
400
600
800
1000
1200
Input(mV)


INL Diagram
INL(%/FSR)
0.0010%
0.0008%
0.0006%
0.0004%
0.0002%
0.0000%
-0.0002%
-0.0004%
-0.0006%
-0.0008%
-0.0010%
Gain=1
Output rate=10sps
delta VR~1.24V
-600
-500
-400
-300
-200
-100
0
100
200
300
400
500
600
Input(mV)

9. SPI

The communication interface of HY310x uses SPI Communication Protocol. There are four pins, namely CS, SDI, SDO and SCK. When CS = Low, SDO is pulled high. SPI initiates operation at this stage. SDI is data input channel; when SDI data is in SCK rising edge, HY310x receives data from Master devices. One frame of SPI is 8-bit, the first frame is command. Command format is shown in Figure 6 Command Format. The first bit is configured as read or write register. The following 3 bits is register address. The fifth bit is configured as no command read. When the fifth bit is high, as long as ADC sends out interrupt, no command needs to be written to read data register; status will be reset only when CS is high. The sixth to eighth bit of command must be set low. Next frame follows by end of command is data. Data length can be 1 to 3 frames. SDO received data is the rising edge trigger of SCK. SDI is falling edge trigger of SCK. Figure 7 Write Register and Read Registeris the clock source of SPI write and read register. The readout data is effective only when SDO=LOW. Figure 8 Continuous Read Modeis the continuous reading mode clock source. SDO will be pulled from high to low when ADC converts data. It can be used to notify master end that the data has been renewed. After data transmission, SDO will be held high until ADC data renewal completed. If CS stays in high, SDO will become high impedance. SDOH register of SYS can be pulled high to solve SDO floating problem.

After the setup of control register SYS[7:0], ADC[15:0] was finished, SDO will change from High to Low in first ADC interrupt signal (IRQ) which equals to 4 times of OSR, then to place Read Command. When Read Command accomplished, SCK can be sent out and received ADC output data after IRQ was generated.

SPI Command								
Name	Re/Wr	Add[2]	Add[1]	Add[0]	NCR	-	-	-
Description	Read =1 Write =0	Address bit2	Address bit1	Address bit0	No Command for Read	Reserved for 0	Reserved for 0	Reserved for 0
Status	1/0	1/0	1/0	1/0	1/0	0	0	0

Figure 6 Command Format

Re/Wr : Read or Write
1 : Read
0 : Write
Add[2:0] : Register Address
000 : SYS (8 bit long)
001 : ADC (16 bit long)
010 : ADO0 (24 bit long)
011 : Reserved
100 : ADO1 (24 bit long)
101 : Reserved

110 : TS (16 bit long)
111 : Reserved

NCR : No command for read
0 : disable
1 : enable (reset by CS = high)

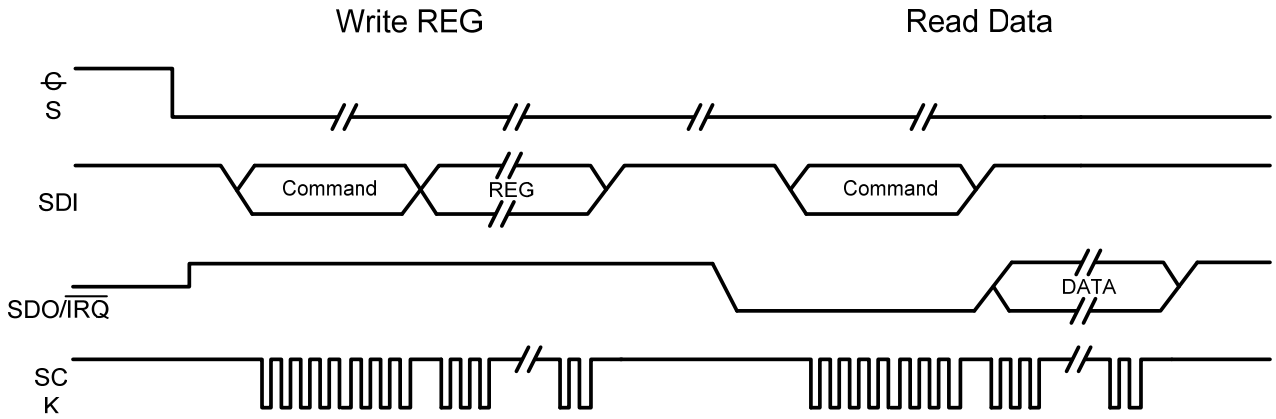


Figure 7 Write Register and Read Register

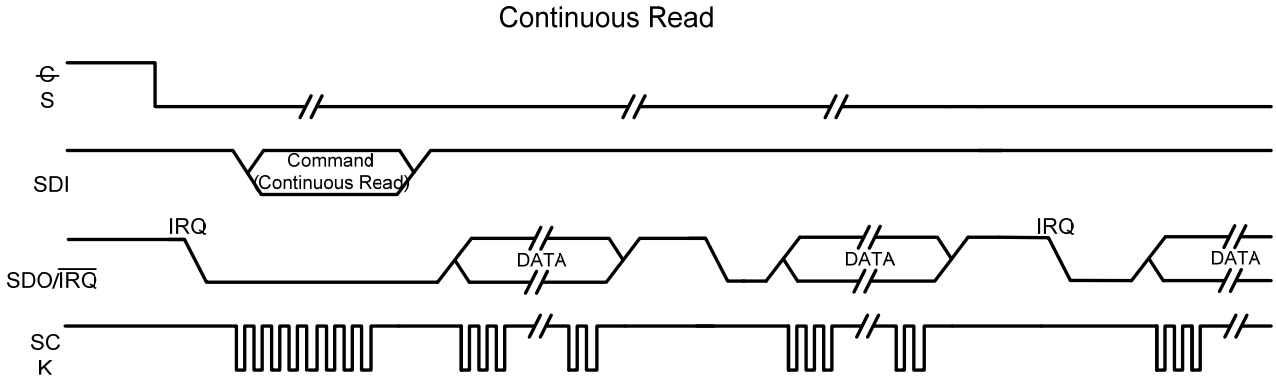


Figure 8 Continuous Read Mode

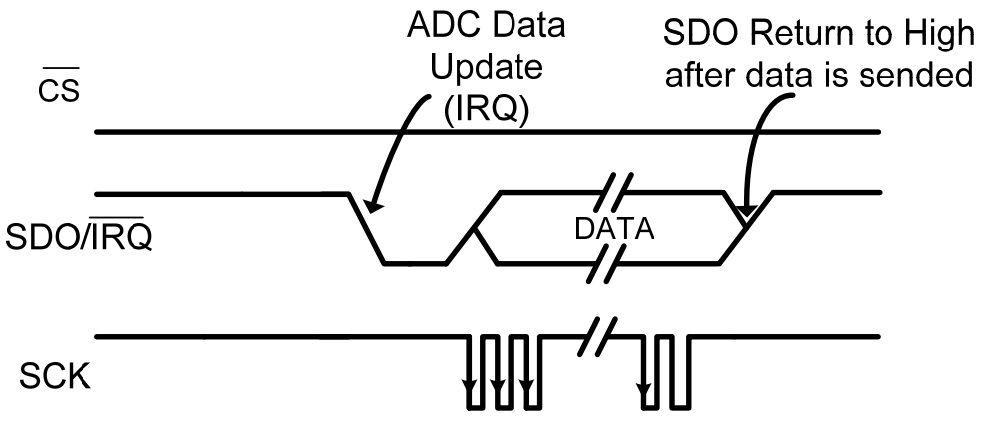


Figure 9 SPI IRQ Signal

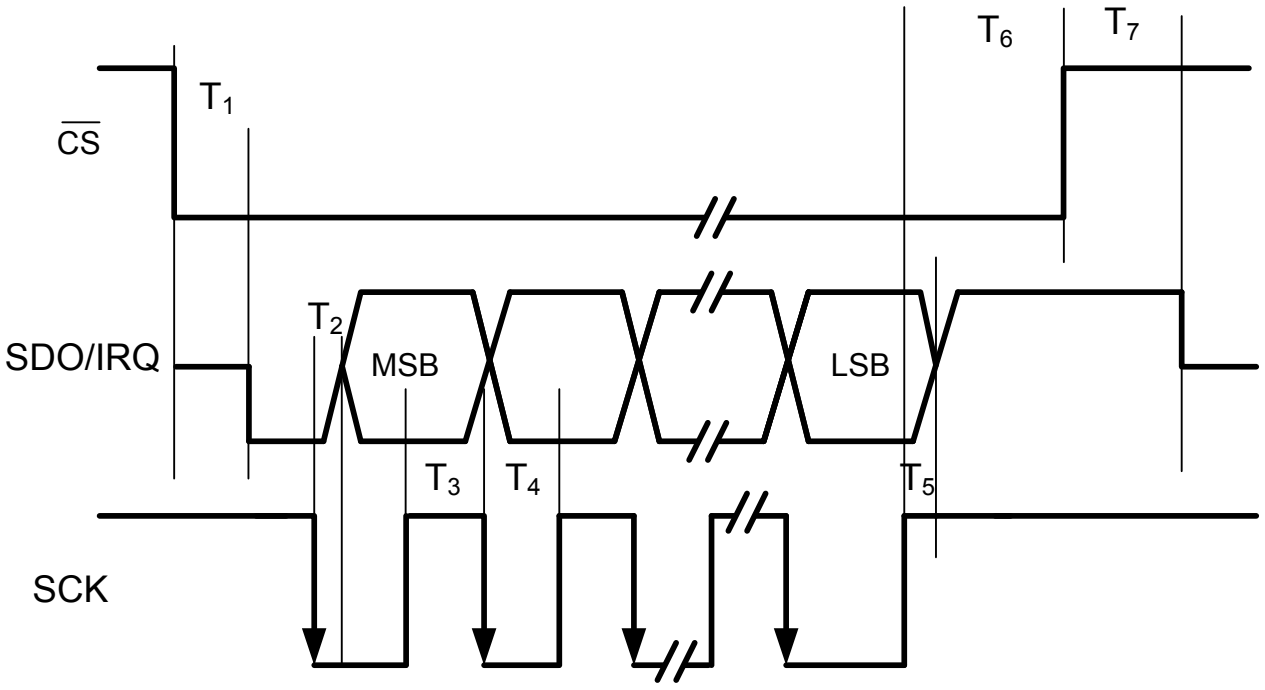


Figure 10 Read Cycle, SDO Timing

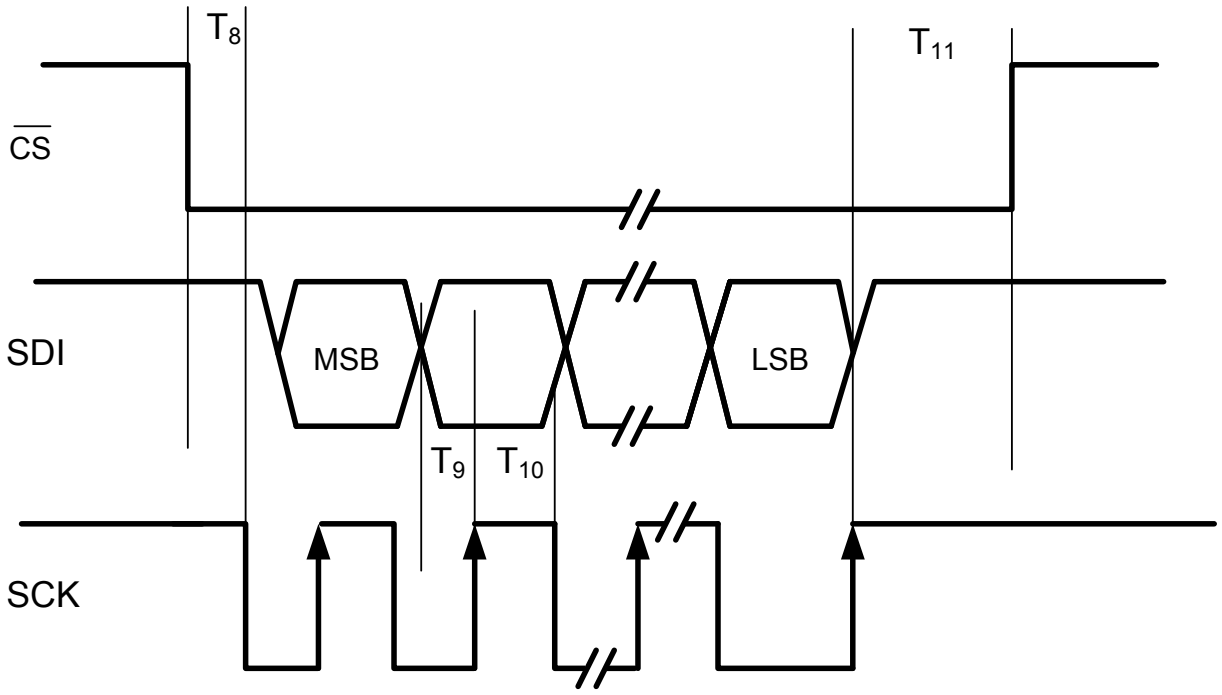


Figure 11 Write Cycle, SDI Timing

Parameter	Limit at TMIN to TMAX	Units	Conditions/Comments
T1	0 IRQ time	ns, min. ns, max.	CS low to SDO low(data out) setup time
T2	0 80	ns, min. ns, max.	SCK low to data valid delay
T3	100	ns, min.	SCK high Pulse width
T4	100	ns, min.	SCK Low Pulse width
T5	10	ns, min.	SCK high to SDO high
T6	10	ns, min.	SCK high to CS high
T7	10 80	ns, min. ns, max.	CS pull high after SDO done
T8	10	ns, min.	CS low to SCK high setup time
T9	30	ns, min.	Data valid to SCK edge setup time
T10	30	ns, min.	Data valid to SCK edge hold time
T11	10	ns, min.	CS high hold time before SDI done
Note: IRQ Time mean ADC's interrupt time.			

Table 2

10. Overview

10.1. Input Channel Multiplex

HY3106 consists of two analog inputs that stored in different memory after conversion. The updated data will be written to the memory and IRQ signal will be sent out after ADC stabilization. Analog inputs can be selected from four modes, input no change, both of ADC inputs connect to VINN, both of ADC inputs connect to VINP and input switch connection (please refers to INX register description on page 14). It takes times to stabilize ADC after switching channel multiplex. New updated data will be written into memory after ADC stabilized.

10.2. Low-Noise PGA

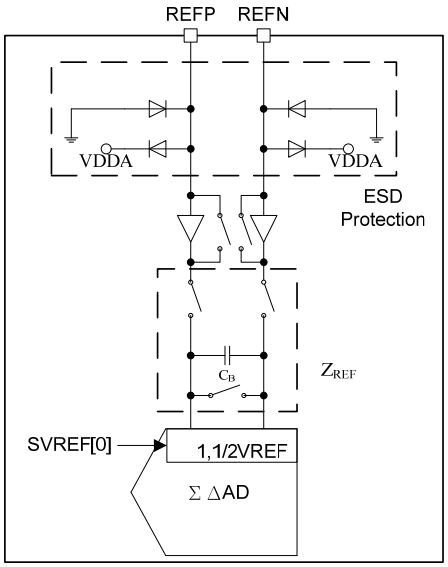
The HY310x features a low-drift, low-noise PGA that provides a complete pre-signal amplification for bridge sensors. A simplified table of sensors maximum output resistor is shown in Table 3 Sensors Maximum Output Resistor. The minimum resolution is 50nV, by selecting gain=8, 16 or 32 of PGA Module, the signal transmits to ADC. Different input impedance must be configured according to different gains. In order to obtain the most stabilized value, the resistors must be accurately-matched to the choice of sensor.

Gain	Sensor Output Impedance (Ohm)
8	4000
16	2000
32	1000

Table 3 Sensors Maximum Output Resistor

10.3. Voltage Reference Inputs

The voltage reference is generated from the voltage difference between REFP and REFN: VREF = REFP – REFN. VREF can be selected as 1 or 1/2 through configuring SVREF. In order to increase the reference input impedance, a switching buffer circuit is used. The REFP and REFN value must be considered when buffer is used; REFP cannot lower than 1.2V while REFN must keep under VDDA-1.2V. Input impedance is taken into account when no internal buffer is used to achieve best ADC performance. The input impedance of voltage reference is 500K.



ESD diodes protect the reference inputs. To prevent these diodes from turning on, make sure the voltages of REFP or FEFN do not go below -100mV, and likewise, do not exceed VDDA by 100mV:

VSS – 100mV < REFP or REFN< VDDA + 100mV

10.4. COMB Filter

HY310x adopts 3rd-order digital filter that comprises different output frequency. If a 4.9152MHZ oscillator is used, 2560, 640, 80 and 10Hz output frequency is generated. Figure 12 The frequency response repeats at multiples of the modulator sampling frequency of 100Hz. Notice that signals at multiples of 10Hz are rejected when the data rate =10SPS, and therefore, simultaneous rejection of 50Hz and 60Hz is achieved.

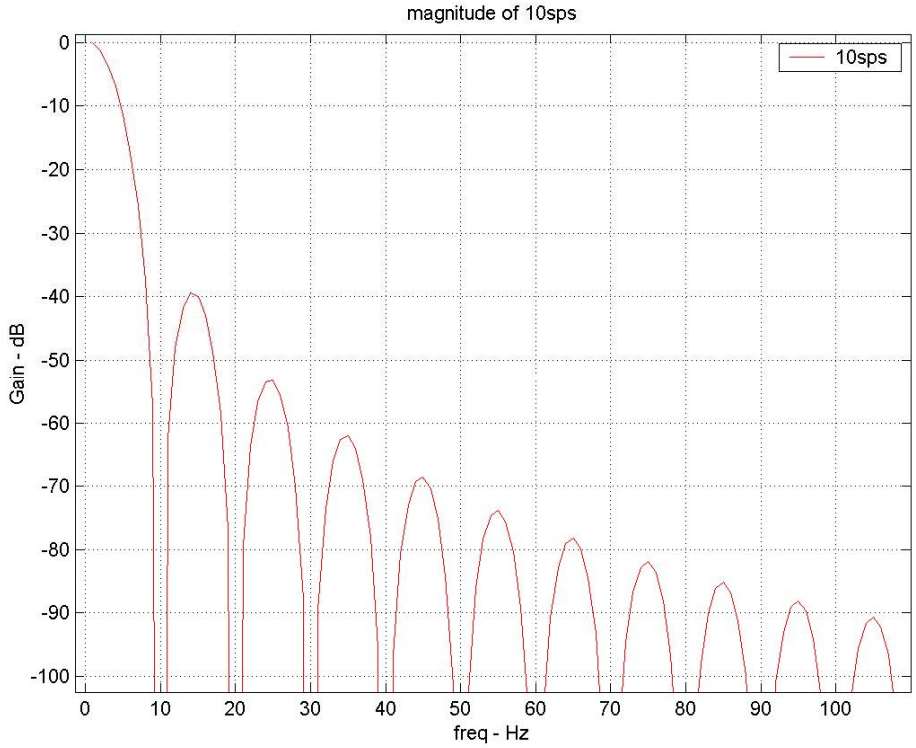


Figure 12

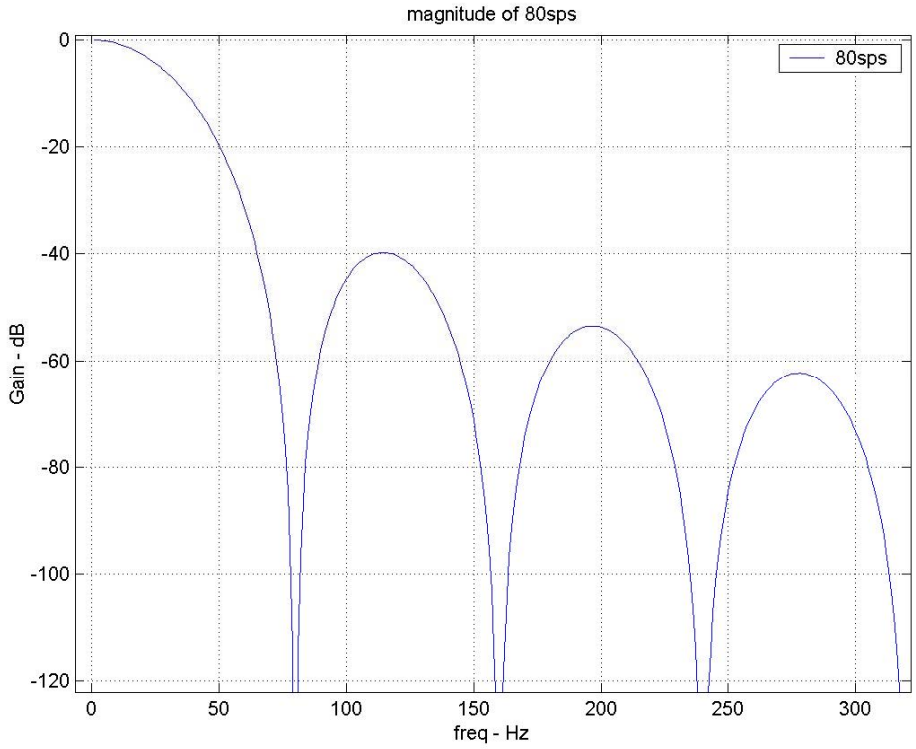


Figure 13

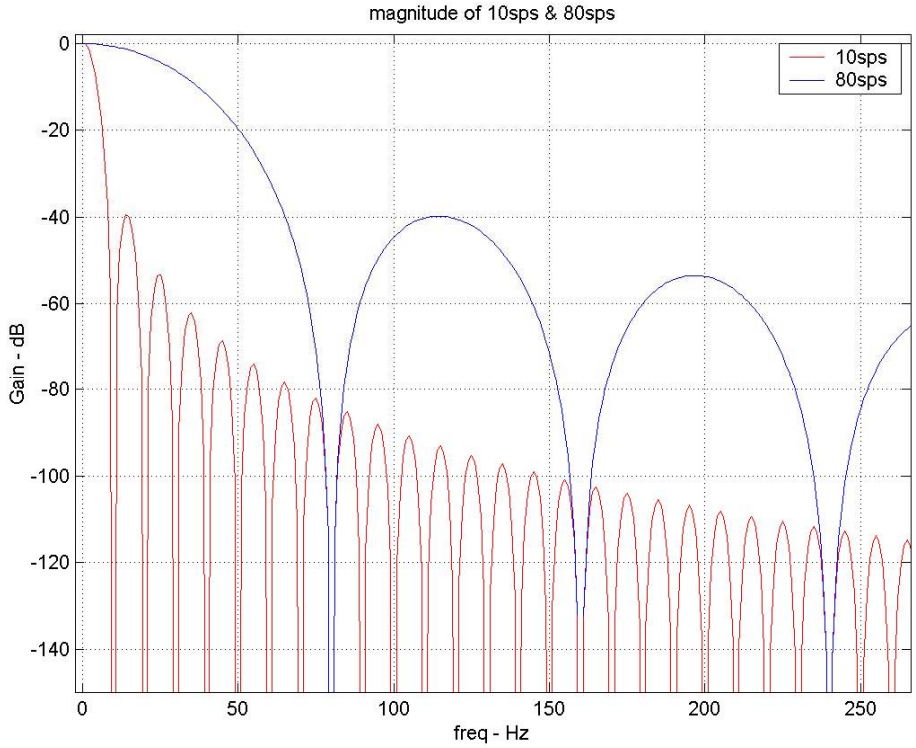


Figure 14

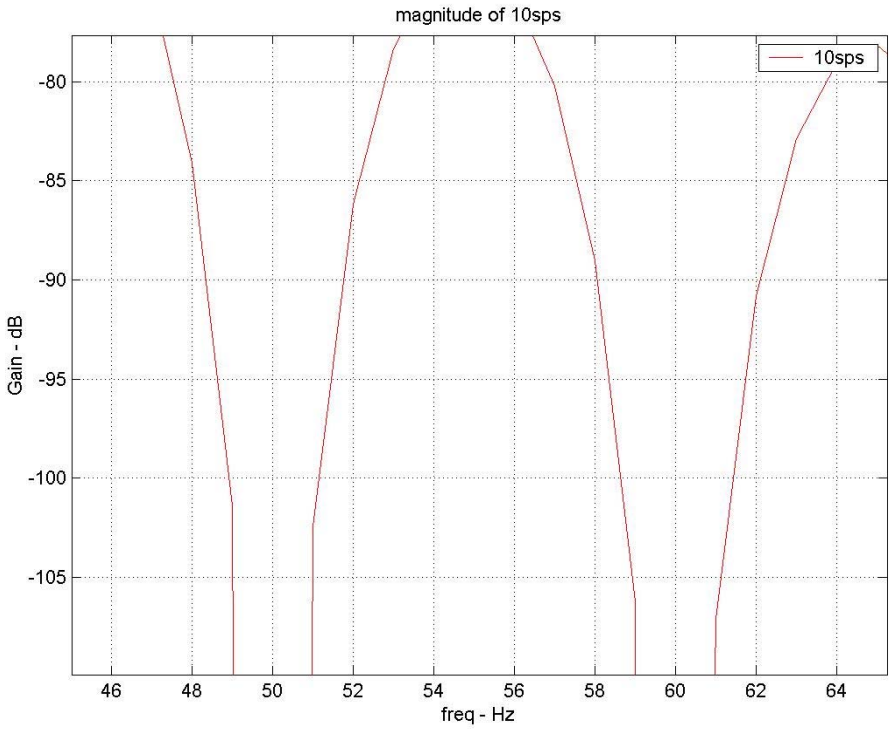


Figure 15

10.5. System Frequency

When ENADC = 0, external and internal clock is inactivated. System power consumption is under 1uA at this moment. When ENADC = 1 and ADCCK = 0, internal RC oscillation frequency output is selected. However with 5% error range, it is recommended not to use internal RC oscillation frequency as to reject 50Hz/60Hz interference. The error range is reduced when crystal is used.

When ENADC = 1 and ADCCK = 1, selects external clock input or connects to crystal. If it needs to reject 50Hz/60Hz interference, clock or crystal of 4.9152 MHz must be chosen.

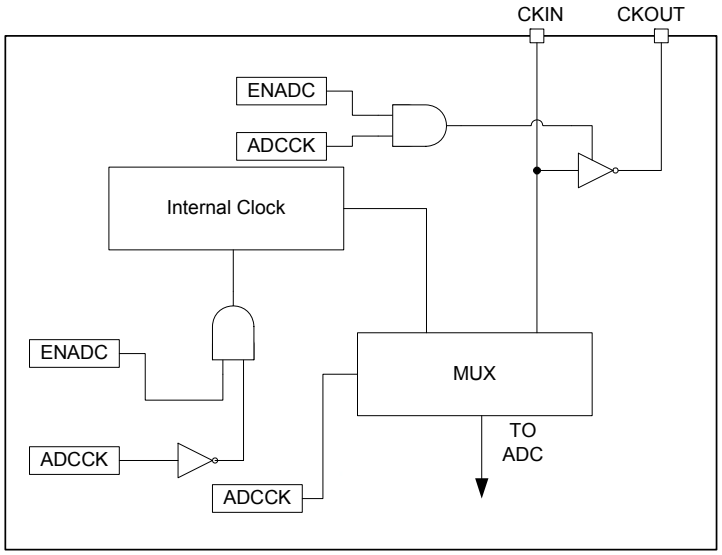


Figure 16

As Figure 17 illustrated, when the external crystal oscillator is connected, R1 has to be varied according to different frequency of external crystal oscillators or resonators so that the circuit of oscillator can be started. Therefore, when external oscillator is 4.9152Mhz, suggested R1 resistance value is 1MΩ. The capacitance value will have a slight difference as the change of PCB layout even the oscillator is the same。Without any particular consideration, C1 and C2 capacitance can be saved. When connected to 4.9152Mhz external oscillator and R1=1MΩ, the ideal start-up time of oscillation is 30ms.

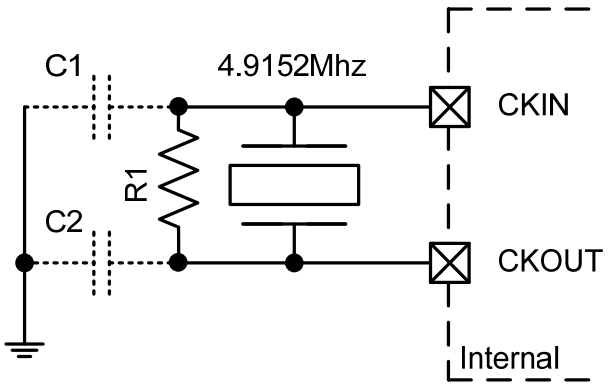


Figure 17 External Oscillator Block Diagram

10.6. Temperature Sensor

Internal temperature sensor can be used to measure temperature when ENADC = 1. After configuring TS register as 1, the chip will generate an IRQ after 3.2ms (using 4.9512 Mhz Crystal or internal RC OSC). This time, the temperature value is stored in TSO Register and ADC measurement will retrieve to original setup and TS register will be 0. ADOx register continues renewing after ADC stabilized. The temperature deviation of this temperature sensor is ± 2℃ after single point calibration.

Under temperature TA, TPS relative voltage, V_{TPS}@TA is measured. Voltage output of TPS, V_{TPS} to temperature change is a linear curve. Thus, the gain G_{TPS}(or slope) is deduced from:

$$G_{TPS} = \frac{V_{TPS@T_A} - V_{TPS@0°K}}{(273.15 + T_{offset} + T_A) - (0)}$$

$$= \frac{V_{TPS@T_A}}{275 + T_A}$$

10.7. Data Format

ADO0 and ADO1 is analog/digital conversion data register of input channel 1 and 2 respectively. It is constituted by Bit[23:0] and is used to save Comb Filter 24-bit output data. Data format of Comb Filter constitution is shown as follows.

+FSR/-FSR：Positive and Negative Full-scale Range

	Equivalent Signal to Be Measured	ADO[23:0]	
		Hexadecimal	Binary
Bipolar Output Binary Two's Complement Format	ΔVR_I	7FFFFF	0111-1111-1111-1111-1111-1111
	$\Delta VR\_I \times \frac{1}{2^{23}}$	000001	0000-0000-0000-0000-0000-0001
	0	000000	0000-0000 0000-0000 0000-0000
	$-\Delta VR\_I \times \frac{1}{2^{23}}$	FFFFFF	1111-1111-1111-1111-1111-1111
	$-\Delta VR\_I$	800000	1000-0000 0000-0000 0000-0000

Table 18 ADO[23:0] vs. Input Signal

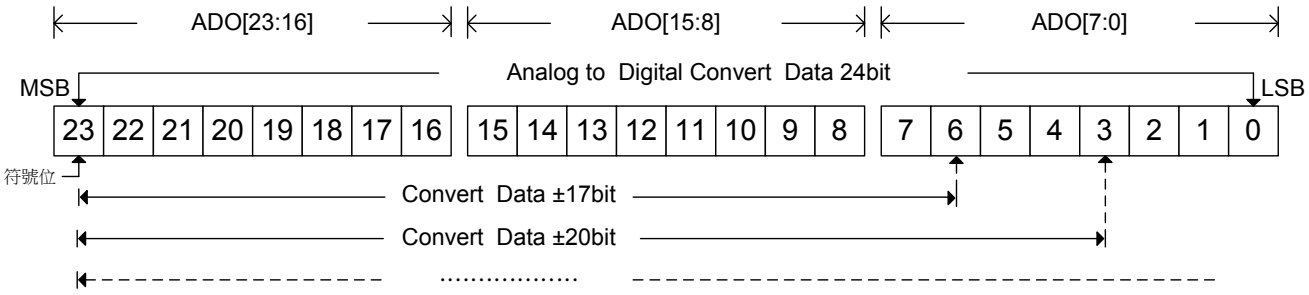


Table 19 Resolution of ADO[23:0

TSO is analog/digital conversion data register of the chip internal temperature sensor. It is constituted by Bit[15:0] and is used to store Comb Filter16-bit output data. Data format of Comb Filter constitution is shown as follows

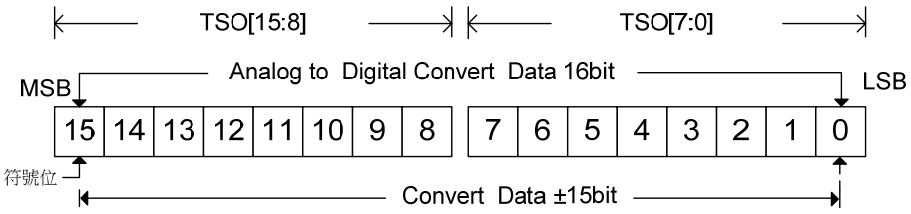


Table 20 Resolution of TSO[15:0]

11. Order Information

Device No.[1]	Package Type	Pins	Package Drawing		Shipment Packing Type	Unit Q'ty	Material Composition	MSL[2]
HY3106-E016	SSOP	16	E	16	Tube	100	Green[3]	MSL-3
HY3106-E016	SSOP	16	E	16	Tape & Reel	2500	Green[3]	MSL-3
HY3104-E016	SSOP	16	E	16	Tube	100	Green[3]	MSL-3
HY3104-E016	SSOP	16	E	16	Tape & Reel	2500	Green[3]	MSL-3
HY3102-E016	SSOP	16	E	16	Tube	100	Green[3]	MSL-3
HY3102-E016	SSOP	16	E	16	Tape & Reel	2500	Green[3]	MSL-3

[1] **Device No.: Model No. – Package Type Description**

Ex: You request HY3106 in SSOP16 package and shipment packing type is Tube.
The device number will be HY3106-E016. And please clearly indicate the shipment packing type (Tube) when placing orders.

Ex: You request HY3102 in SSOP16 package and shipment packing type is Tape & Reel. The device number will be HY3102-E016.
And please clearly indicate the shipment packing type (Tape & Reel) when placing orders.

[2] **MSL:**

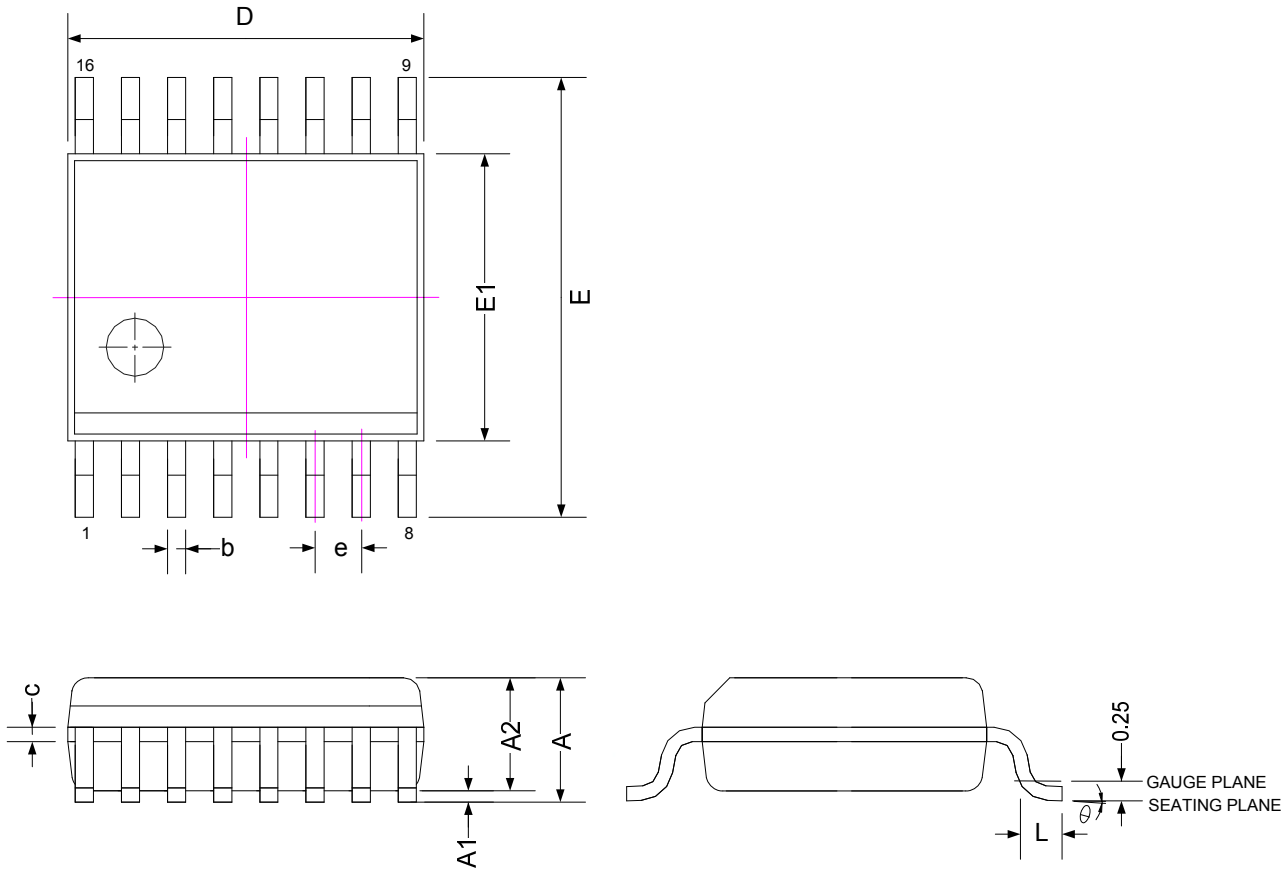
The Moisture Sensitivity Level ranking conforms to IPC/JEDEC J-STD-020 industry standard categorization. The products are processed, packed, transported and used with reference to IPC/JEDEC J-STD-033.

[3] **Green (RoHS & no Cl/Br):**

HYCON products are Green products that compliant with RoHS directive and are Halogen free (Br/Cl<0.1%)

12. Package Information

12.1. SSOP16



SYMBOLS	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	0.15	0.25
A2	-	-	1.50
b	0.20	-	0.30
c	0.18	-	0.25
D	4.80	4.90	5.00
E1	3.81	3.91	3.99
E	5.79	5.99	6.20
L	0.41	-	1.27
e	0.635 BASIC		
θ°	0	-	8

Note:

1. All dimensions refer to JEDEC OUTLINE MO-137.
2. Do not include Mold Flash or Protrusions.
3. Unit : mm

13. Revision Record

Major differences are stated thereinafter:

Version	Page	Revision Summary
V02	All	First Edition
V03	5	Add in Model No. list
	21	Add in SIP description
	32	Revise Order Information
V04	29~30	Add the illustration of System Frequency
V06	23~24	Update SPI Timing diagram
	33	Update Package Information