Solution for I_D:

$$I_{D1} = I_{D2} \cong \frac{1}{8kR_S^2}\left[1 + 4kR_S(V_{CM}+V_{SS}-V_t) \mp \sqrt{1+8kR_S(V_{CM}+V_{SS}-V_t)}\right]$$

(+) physically not possible since $V_{GS} < V_t$

where $k = \frac{1}{2}\frac{W}{L}\mu C_{ox}$

and $$V_{DS1} = V_{DS2} \cong V_{DD} + V_{SS} - I_D(R_D + 2R_S)$$

Numerical Example

$V_{DD} = V_{SS} = 5V$

$R_S = 18k\Omega$

$R_D = 39k\Omega$

$V_t = 0.9V$

$k = 4 \times 10^{-4}\ \frac{A}{V^2}$

$V_{DSsat} \cong (V_{GS} - V_t)$

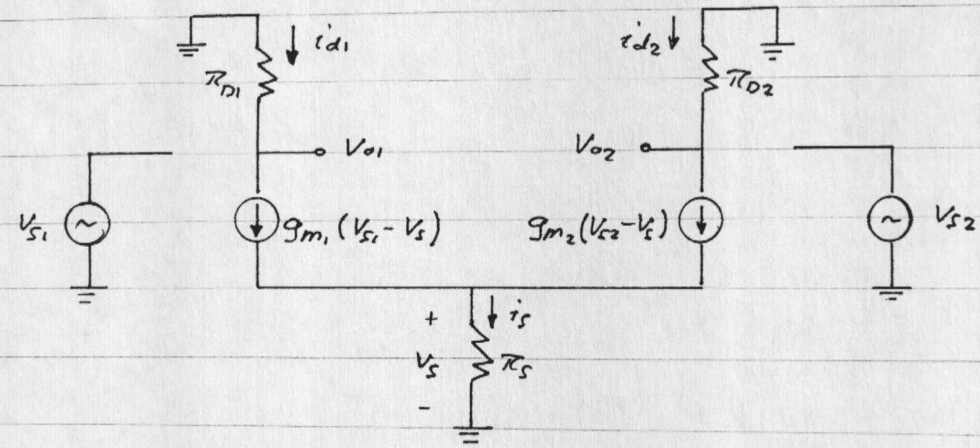
e.g. $\mu_n = 5 \times 10^{-2}\ \frac{m^2}{Vs}$, $C_{ox} = 8 \times 10^{-4}\ \frac{F}{m^2}$, $\frac{W}{L} = \frac{100\mu m}{5\mu m} = 20$

Case A	Case B	Case C
$V_{CM} = 0$	$V_{CM} = -1V$	$V_{CM} = 1V$
$I_D \cong 100\mu A$	$I_D \cong 74\mu A$	$I_D \cong 131\mu A$
$V_{DS} \cong 4.3V$	$V_{DS} \cong 5.8V$	$V_{DS} \cong 2.5V$
$V_{DSsat} \cong 0.50V$	$V_{DSsat} \cong 0.43V$	$V_{DSsat} \cong 0.57V$
$g_m \cong 4 \times 10^{-4}\ \frac{A}{V}$	$g_m \cong 3.4 \times 10^{-4}\ \frac{A}{V}$	$g_m \cong 4.6 \times 10^{-4}\ \frac{A}{V}$

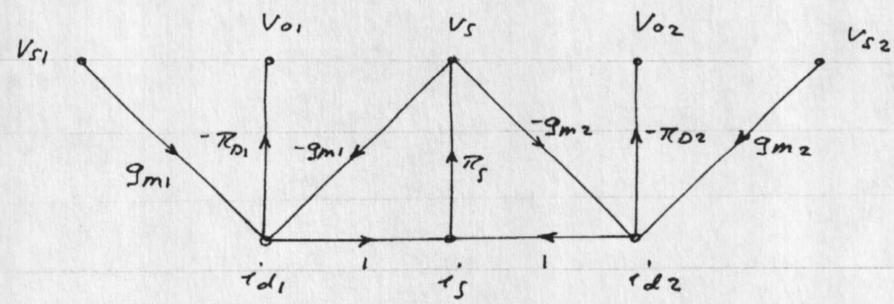
We note again that the common mode input voltage influences the operating point and thus the ac performance (g_m!) of the differential gain stage. To remedy this situation we can again apply a current source biasing scheme!

4.2.2 AC Considerations

linear equivalent circuit (y-parameter model)



SFG



$$\Delta = 1 + g_{m1} r_s + g_{m2} r_s$$

If transistors are perfectly matched we obtain

$$\left| \Delta = 1 + 2 g_m r_s \right|$$

$$\frac{V_{o1}}{V_{s1}} = -g_m R_D \left(\frac{1 + g_m R_S}{1 + 2 g_m R_S} \right)$$

$$V_{o1} = \frac{V_{s1}(-g_m R_D) - V_{s1}(g_m R_S g_m R_D)}{1 + g_m R_S + g_m R_S}$$