

# HD74LS95B ● 4-bit Parallel Access Shift Registers

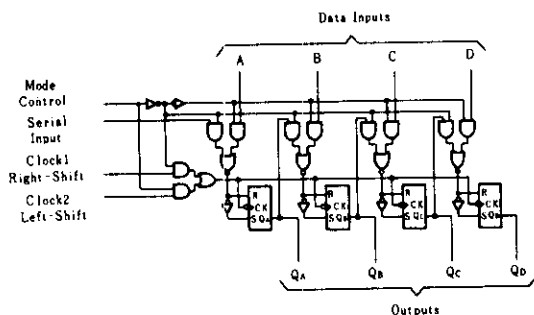
This 4-bit register features parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The register has three mode operation:

- Parallel (broadside) load
- Shift right (the direction  $Q_A$  toward  $Q_D$ )
- Shift left (the direction  $Q_D$  toward  $Q_A$ )

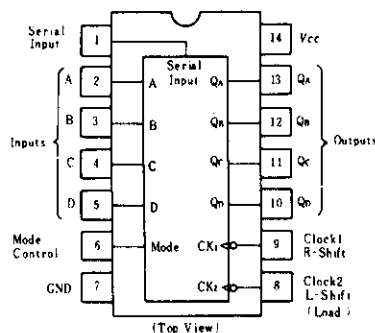
Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited. Shift right is accomplished on the high-to-low transition of clock-1 when the

mode control is low; shift left is accomplished on the high-to-low transition of clock-2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop ( $Q_D$  to input C, etc.) and serial data is entered at input D. The clock input may be applied commonly to clock-1 and clock-2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the function table will also ensure that register contents are protected.

## ■ BLOCK DIAGRAM



## ■ PIN ARRANGEMENT



## ■ FUNCTION TABLE

Mode Control	Inputs							Outputs			
	Clocks		Serial	Parallel				$Q_A$	$Q_B$	$Q_C$	$Q_D$
	2(L)	1(H)		A	B	C	D				
H	H	X	X	X	X	X	X	$Q_{A0}$	$Q_{B0}$	$Q_{C0}$	$Q_{D0}$
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	$Q_B^\dagger$	$Q_C^\dagger$	$Q_D^\dagger$	d	$Q_{Bn}$	$Q_{Cn}$	$Q_{Dn}$	d
L	L	H	X	X	X	X	X	$Q_{A0}$	$Q_{B0}$	$Q_{C0}$	$Q_{D0}$
L	X	↓	H	X	X	X	X	H	$Q_{An}$	$Q_{Bn}$	$Q_{Cn}$
L	X	↓	L	X	X	X	X	L	$Q_{An}$	$Q_{Bn}$	$Q_{Cn}$
↑	L	L	X	X	X	X	X	$Q_{A0}$	$Q_{B0}$	$Q_{C0}$	$Q_{D0}$
↓	L	L	X	X	X	X	X	$Q_{A0}$	$Q_{B0}$	$Q_{C0}$	$Q_{D0}$
↓	L	H	X	X	X	X	X	$Q_{A0}$	$Q_{B0}$	$Q_{C0}$	$Q_{D0}$
↑	H	L	X	X	X	X	X	$Q_{A0}$	$Q_{B0}$	$Q_{C0}$	$Q_{D0}$
↑	H	H	X	X	X	X	X	$Q_{A0}$	$Q_{B0}$	$Q_{C0}$	$Q_{D0}$

Notes) 1. H; high level, L; low level, X; irrelevant

2. †; transition from low to high level

3. ‡; transition from high to low level

4. a~d; the level of steady-state input at inputs A, B, C, or D, respectively

5.  $Q_{A0} \sim Q_{D0}$ ; the level of  $Q_A$ ,  $Q_B$ ,  $Q_C$ , or  $Q_D$ , respectively,

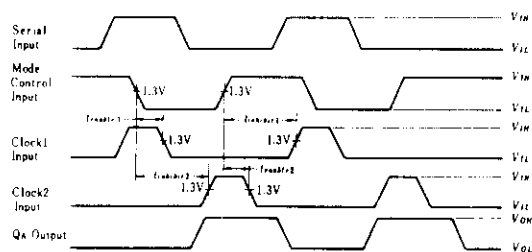
before the indicated steady-state input conditions were established.

6.  $Q_{An} \sim Q_{Dn}$ ; the level of  $Q_A$ ,  $Q_B$ ,  $Q_C$ , or  $Q_D$ , respectively, before the most-recent (†) transition of the clock.

7. ‡; Shifting left requires external connection of  $Q_B$  to A,  $Q_C$  to B, and  $Q_D$  to C. Serial data is entered at input D.

## RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Clock frequency	$f_{clock}$	0	—	25	MHz
Clock pulse width	$t_{w(CK)}$	25	—	—	ns
Setup time	$t_{su}$	20	—	—	ns
Hold time	$t_h$	10	—	—	ns
Enable time 1	$t_{enable\ 1}$	20	—	—	ns
Enable time 2	$t_{enable\ 2}$	20	—	—	ns
Inhibit time 1	$t_{inhibit\ 1}$	20	—	—	ns
Inhibit time 2	$t_{inhibit\ 2}$	20	—	—	ns



Clock Enable/Inhibit Times

## ELECTRICAL CHARACTERISTICS ( $T_a = -20 \sim +75^\circ\text{C}$ )

Item	Symbol	Test Conditions	min	typ*	max	Unit
Input voltage	$V_{IH}$		2.0	—	—	V
	$V_{IL}$		—	—	0.8	
Output voltage	$V_{OH}$	$V_{CC} = 4.75\text{V}, V_{IH} = 2\text{V}, V_{IL} = 0.8\text{V}, I_{OH} = -400\mu\text{A}$	2.7	—	—	V
	$V_{OL}$	$V_{CC} = 4.75\text{V}, V_{IH} = 2\text{V}, I_{OL} = 4\text{mA}$	—	—	0.4	V
		$V_{IL} = 0.8\text{V}, I_{OL} = 8\text{mA}$	—	—	0.5	
Input current	$I_{IH}$	$V_{CC} = 5.25\text{V}, V_i = 2.7\text{V}$	—	—	20	$\mu\text{A}$
	$I_{IL}$	$V_{CC} = 5.25\text{V}, V_i = 0.4\text{V}$	—	—	-0.4	$\text{mA}$
	$I_i$	$V_{CC} = 5.25\text{V}, V_i = 7\text{V}$	—	—	0.1	$\text{mA}$
Short-circuit output current	$I_{os}$	$V_{CC} = 5.25\text{V}$	-20	—	-100	$\text{mA}$
Supply current **	$I_{CC}$	$V_{CC} = 5.25\text{V}$	—	13	21	$\text{mA}$
Input clamp voltage	$V_{IK}$	$V_{CC} = 4.75\text{V}, I_{IN} = -18\text{mA}$	—	—	-1.5	V

\*  $V_{CC} = 5\text{V}, T_a = 25^\circ\text{C}$

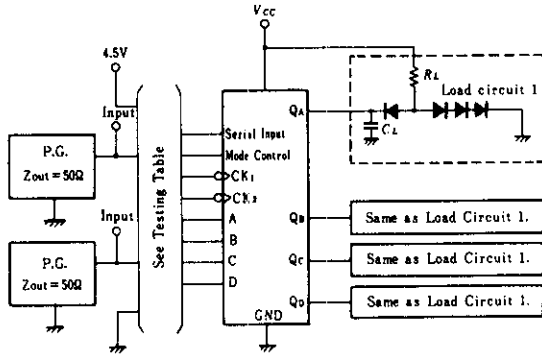
\*\*  $I_{CC}$  is measured with all outputs and serial input open; A, B, C, and D inputs grounded; mode control at 4.5V; and momentary 3V, then ground, applied both clock inputs.

## SWITCHING CHARACTERISTICS ( $V_{CC} = 5\text{V}, T_a = 25^\circ\text{C}$ )

Item	Symbol	Test Conditions	min	typ	max	Unit
Maximum clock frequency	$f_{max}$	$C_L = 15\text{pF}, R_L = 2\text{k}\Omega$	25	36	—	MHz
Propagation delay time	$t_{PLH}$		—	18	27	ns
	$t_{PHL}$		—	21	32	ns

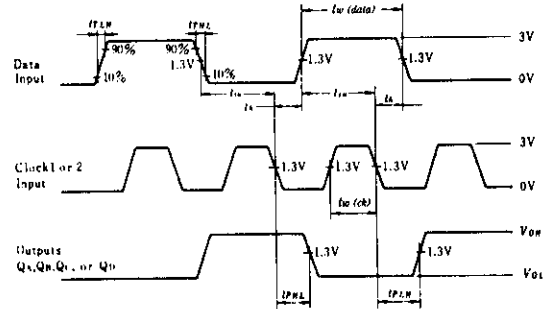
## TESTING METHOD

### 1) Test Circuit



- Notes) 1.  $C_L$  includes probe and jig capacitance.  
2. All diodes are 1S2074  $\text{Ⓢ}$ .

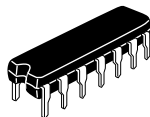
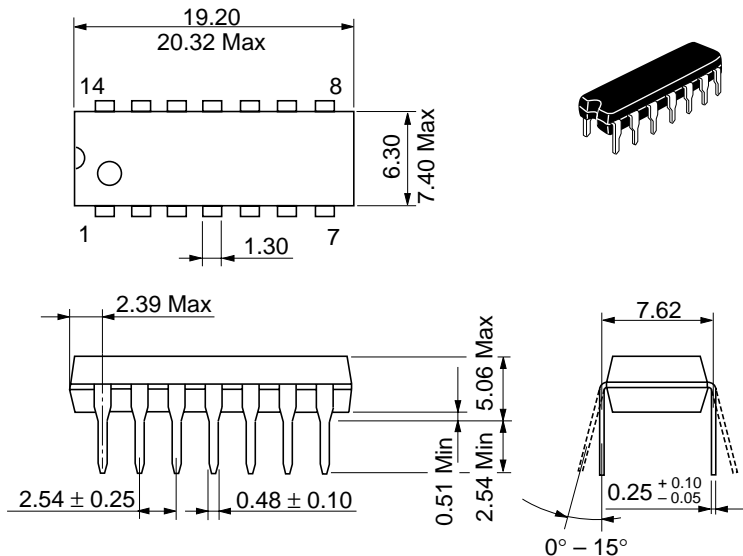
### Waveform



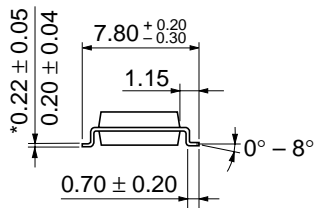
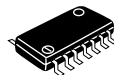
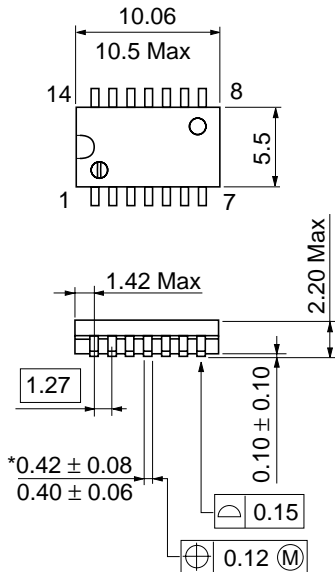
- Note) 1. Input pulse:  $t_{PLH}, t_{THL} \leq 10\text{ns}$ ,  
Data  $PRR = 500\text{kHz}$   
Clock  $PRR = 1\text{MHz}$

### 2) Testing Table

Item	From input to output	Inputs								Outputs			
		CK-1	CK-2	Mode Control	Serial Inputs	A	B	C	D	QA	QB	QC	QD
$f_{max}$	CK-1→Q	IN	4.5V	0V	IN	4.5V	4.5V	4.5V	4.5V	OUT	OUT	OUT	OUT
	CK-2→Q	4.5V	IN	4.5V	4.5V	IN	IN	IN	IN	OUT	OUT	OUT	OUT
$t_{PLH}$	CK-1→Q	IN	4.5V	0V	IN	4.5V	4.5V	4.5V	4.5V	OUT	OUT	OUT	OUT
$t_{PHL}$	CK-2→Q	4.5V	IN	4.5V	4.5V	IN	IN	IN	IN	OUT	OUT	OUT	OUT

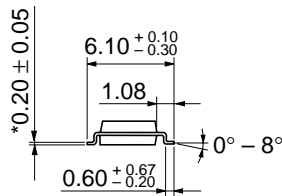
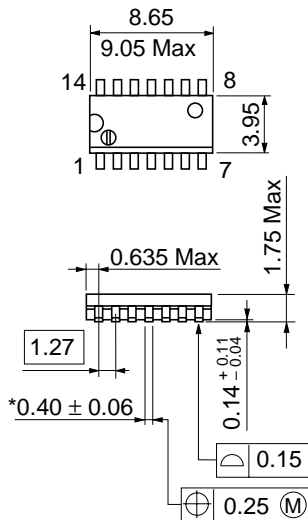


Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g



Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.13 g

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