A Soft Switching Three-phase Current-fed Bidirectional DC-DC Converter With High Efficiency Over a Wide Input Voltage Range

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***Abstract*—In this paper, a three-phase current-fed dual-active-bridge (DAB) bidirectional DC-DC converter is presented. Compared to the voltage source DAB converter, the proposed converter allows low RMS current and maintains zero voltage switching (ZVS) in the whole operating range by keeping the ratio between primary side and secondary side DC-link voltage constant, leading to high efficient energy conversion over a wide input voltage range. In addition, the ZVS conditions can be maintained using small DC inductors and the input current ripple still remains small because of high DC inductor current ripples being alleviated by three-phase interleaving structure. Furthermore, the proposed topology with Y-Y connected transformers is proven to have better current sharing capability compared with other three-phase topologies with different transformer connections. The operation mode analysis, soft switching conditions, and hardware design guidelines are derived in this paper. A 6-kW hardware prototype with input voltage range of 24∼48 V and rated 288 V output voltage is developed and tested in the laboratory. The experimental results verified that the proposed converter could maintain high efficiency over a wide input voltage and power range.**

***Index Terms*—Bidirectional, current-fed, DC-DC converter, dual-active-bridge, three-phase.**

I. Introduction

In RECENT years, dual-active-bridge (DAB) DC-DC converters and their derivatives are catching more attention in industry and academia since they offer many advantages such as galvanic isolation, natural soft-switching, and bidirectional power flow with unified phase shift controller [1]–[9]. For example, it has been used in hybrid electric vehicles (HEVs) as auxiliary an power supply to replace the starter/alternator and to provide galvanic isolation between the low voltage battery and high voltage bus [2], [3]. Another important application is interfacing with energy storage elements [4], [6]. In addition, it has become a key stage in AC–DC–DC–AC solid state transformers (SSTs) [7]–[10].

Most of the research in the literature focuses on the voltage source DAB converters [1]–[11]. In the voltage source DAB converters, the DC-link voltage cannot be regulated by phase shift control. Therefore, the converter will fail to satisfy the soft switching conditions when the ratio of input to output voltage is not close to the transformer turns ratio [1]. Furthermore, the mismatch between the primary side and secondary side DC-link voltages will result in large RMS and peak current in both transformer and switches even in no load conditions [2], thus high efficiency is hard to achieve over wide input or output voltage ranges [11].

In order to improve performance in a wide operating range, many optimized modulation methods are proposed for voltage source DAB converters to maintain soft switching conditions and reduce reactive power loss. In [12], phase shift plus duty cycle control is used to maintain ZVS conditions, but the maximum phase shift is constrained and the power flow is therefore limited. A novel dual-phase-shift control is proposed in [13] to eliminate reactive power and increase system efficiency when input and output voltages do not match. In this case, converter control becomes complicated due to the output power being related to two-phase shift variables, and that the circulating current still exists in this mode even though the reactive power is eliminated totally. A hybrid modulation method is applied to extend power range for ultracapacitor application in [14], in which a proposed triangular modulation and common phase shift modulation are applied together to increase the power transfer range with wide input voltage.

Current-fed topology provides another solution to improve performance for the wide operating range. In [15], an isolated boost full-bridge DC-DC converter is addressed to fulfill the requirements of wide voltage range, bidirectional power flow and high-efficiency. Another current-fed dual-half-bridge (DHB) converter is proposed for fuel cell application [16], in which the DC-link voltage of low voltage side can be controlled by adjusting the duty cycle. In these two current-fed converters, auxiliary clamp circuit or comparable large DC inductors are required to avoid voltage spikes and high input current ripples.

Although current-fed topologies improve performance for the wide operating range compared to their voltage-fed counterparts, a large DC inductor is usually required to lower the input current ripple. In addition, the DC inductor current will affect and complicate the soft switching condition analysis. In this study, a three-phase current-fed dual-active-bridge (DAB) DC-DC converter with isolated Y-Y connected transformers is proposed to solve the above issues. The major features of the proposed converter are as follows:

1) Increased converter power rating by paralleling phases.

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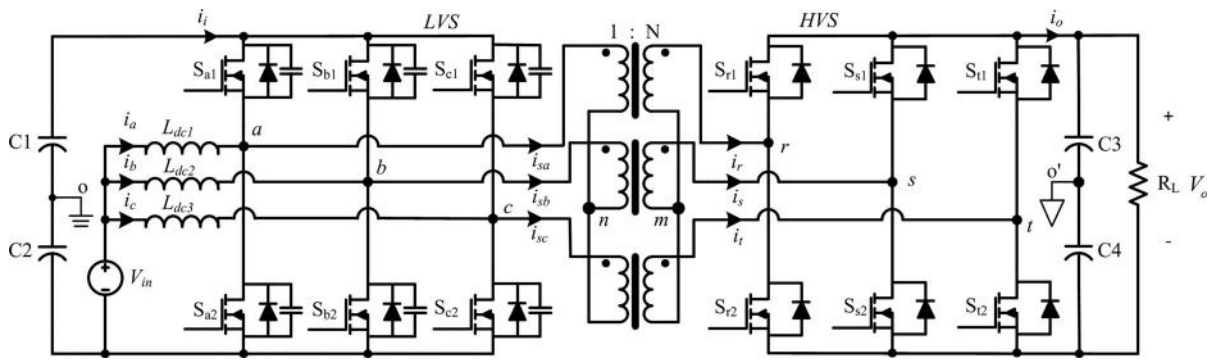

Fig. 1. Proposed three-phase current-fed dual-active-bridge bidirectional DC-DC converter.

2) Reduced size of input DC inductors and DC-link capacitor with interleaving structure.
3) Maintained soft switching conditions and high efficiency over a wide load range and wide input voltage range without auxiliary circuitry.
4) Easily-implemented power flow management because of decoupled duty cycle and phase shift control.

The operation principle of the proposed topology is described in detail in Section II. In order to demonstrate the advantages of the proposed topology, a three-phase voltage source DAB converter and a three single-phase interleaved DHB converter have also been discussed and compared. The results show that three-phase topology is superior to single-phase topology not only due to the reduction of current and voltage ripples leading to smaller size of passive components, but also due to the lower reactive power loss and higher maximum power capability. Moreover, among three-phase topologies, the current-fed topology can maintain the DC-link voltage constant to flatten the current waveform, therefore, the peak value and RMS value of current in switches and transformer will be lower under varied input voltage compared with voltage type topology. The analysis of ZVS conditions of the converter is given in Section III. Furthermore, the current unbalance analysis is presented in section IV. The analysis is also extended to other types of three-phase converters with different transformers connection. The analysis indicates that the proposed converter with Y-Y connected transformers has better current sharing capability compared with other types of topologies, especially when integrated leakage inductance is applied. Based on the analysis in these sections, the hardware design guideline and experimental results is given in Sections V and VI.

II. The Proposed Topology and Comparison

A. Topology Description

The topology of the proposed converter is shown in Fig. 1, which consists of three DC inductors and a three-phase DAB bidirectional DC-DC converter. A low voltage energy storage element such as battery or ultracapacitor can be connected in the current-fed port and the high voltage side can be connected to the high voltage DC bus to provide power to inverter for specific applications. The converter can be operated in boost mode when the power flows from low voltage side (LVS) to high voltage side (HVS) or in buck mode when the energy source absorbs power from HVS. In the boost mode, the boost function is achieved by DC inductors and three half bridges on LVS, to keep DC bus voltage constant so as to allow high efficiency conversion for widely varied input voltage sources. Comparatively, in buck mode, three small DC inductors $L_{\rm dc1}$ – $L_{\rm dc3}$ are used as filters to smooth the charging current. In order to achieve soft switching and reduce the turn-off switching loss, small snubber capacitors are paralleled with the MOSFETs on LVS and HVS. Three single-phase high frequency transformers are connected in Y-Y type to reduce circulating current and alleviate current unbalance issues. The leakage inductance is implemented in each transformer as an energy transfer element.

Benefitting from interleaving structure, the three-phase current-fed DAB converter has much smaller passive components compared with the single-phase DHB converter. Similar to the three-phase DAB converter, the gate signals for upper and bottom switches on each phase are complementary, with the phase angle $2\pi/3$ between phase legs on one side. The power flow is bidirectional by controlling the phase shift angle between the active switches on LVS and HVS. Unlike the fixed duty cycle control in voltage source DAB converter, the duty cycle is controllable to keep the DC-link voltage constant on LVS in wide input voltage range or to keep the DC-link voltages on both sides to be matched. Due to the two control variables, duty cycle D and phase shift angle φ, the operation will be more complicated than voltage source three-phase DAB (DAB3) converter. Detailed analysis will be given in the following sections.

B. Operating Mode Analysis

1) 50% Fixed Duty Cycle: Considering that the duty cycle is 50% fixed, the operation principle is similar to the three-phase voltage source DAB converter. The power equation can be derived by the integration of the instantaneous power $p(t)$ over one switching period

$$P_o = \frac{3}{2\pi}\int_0^{2\pi} v_{\rm an}(\omega t) i_a(\omega t) d\omega t \tag{1}$$

where $v_{\rm an}(\omega t)$ is the voltage on the primary side of transformer and $i_a(\omega t)$ is the primary side transformer current. Fig. 2 shows the voltage and current waveforms on transformer in different cases. Taking phase a in 2 (a) as an example, ignore the capacitor resonance during the dead time zone which is discussed in [16], and the interval t_1 to t_9 of Fig. 2(a) can illustrate

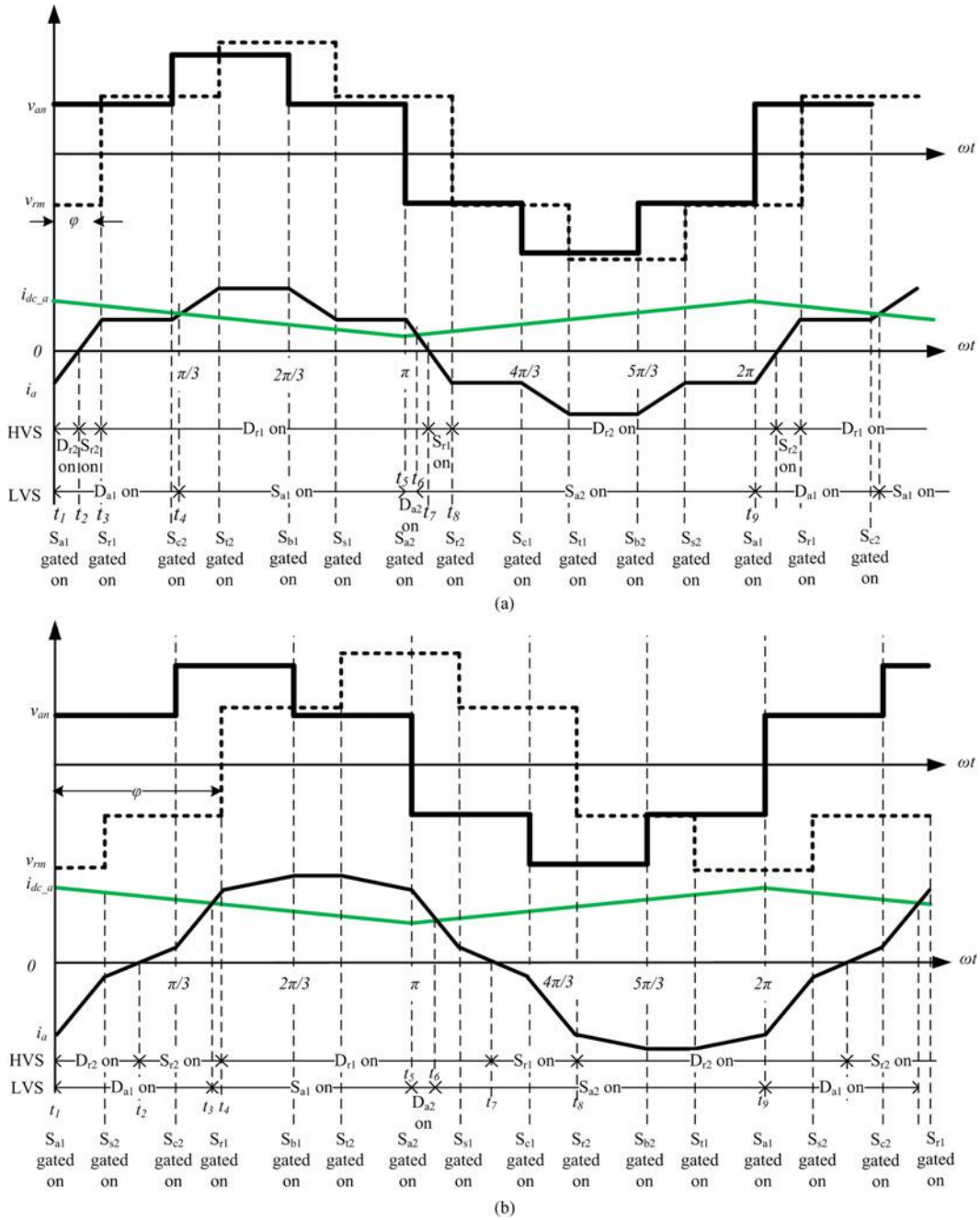

Fig. 2. Voltage and current waveforms in transformer and DC input inductor: (a) $\varphi \leq \pi/3$. (b) $\pi/3 < \varphi < 2\pi/3$.

the stages of operation during one switching period. The situation of switches on LVS is determined by the sum of dc inductor current i_{dc_a} and transformer current i_a, and stage of switches on HVS is depends on the transformer current. The brief description of each stage is given as follows:

Stage 1 (t_1–t_2): At t_1, S_{a1} is gated on. i_a is increasing but negative, so D_{r2} is conducting. i_{dc_a} is decreasing but higher than i_a, thus D_{a1} is conducting in accordance with Kirchoff's Current Law (KCL).

Stage 2 (t_2–t_3): At t_2, i_a increases to be positive and S_{r2} begins to conduct. But it is lower than i_{dc_a}, so D_{a1} continues conducting.

Stage 3 (t_3–t_4): At t_3, S_{r1} is gated on. i_a is positive and D_{r1} is conducting. i_{dc_a} continues decreasing but i_a is still lower than i_{dc_a}, therefore D_{a1} is conducting.

Stage 4 (t_4–t_5): At t_4, i_{dc_a} decreases and is lower than i_a, so S_{a1} begins to conduct.

Stage 5 (t_5–t_6): At t_5, S_{a2} is gated on. Since i_a is higher than i_{dc_a}, D_{r2} conducts first until t_6 when i_{dc_a} surpasses i_a.

Stage 6 (t_6–t_7): At t_6, S_{a2} begins to conduct. i_a is positive, so D_{r1} continues conducting.

Stage 7 (t_7–t_8): At t_7, i_a decreases to be negative and S_{r1} begins to conduct.

Stage 8 (t_8–t_9): At t_8, S_{r2} is gated on. i_a is negative, so D_{r2} is conducting. At t_9, one switching period is completed and the converter operation will repeat.

The stage of operation of 2(b) can be derived in the same way.

The exact value of $v_{\rm an}(\omega t)$ can be expressed as

$$v_{\rm an}(\omega t) = \begin{cases} \dfrac{V_d}{3}, 0 < \omega t < \pi/3 \\ \dfrac{2V_d}{3}, \pi/3 < \omega t < 2\pi/3 \\ \dfrac{V_d}{3}, 2\pi/3 < \omega t < \pi. \end{cases} \tag{2}$$

There is a phase delay φ between $v_{\rm an}$ and $v_{\rm rm}$

$$v_{\rm rm}(\omega t) = v_{\rm an}(\omega t - \varphi). \tag{3}$$

The voltage on the leakage inductance is the difference between $v_{\rm an}$ and $v_{\rm rm}$. For each time interval, $v_{\rm an}$ and $v_{\rm rm}$ are constants, so the current on leakage inductance can be calculated as

$$i_a(\omega t) = i_a(\omega t_0) + \frac{V_{an} - V_{\rm rm}}{\omega L_s}(\omega t - \omega t_0) \tag{4}$$

where $i_a(\omega t_0)$ is the initial current of corresponding time interval. $i_a(\omega t)$ can be expressed by $i_a(0)$ using iterative method. As D was given 1/2, the current waveform is symmetrical in one switching period, i.e., $i_a(0) = -i_a(\pi)$. Solve for $i_a(0)$

$$i_a(0) = \begin{cases} \dfrac{-V_d\left[2(1-d)\pi + 3d\varphi\right]}{9\omega L_s}, & 0 < \varphi \le \dfrac{\pi}{3} \\ \dfrac{-2V_d\left[3d\left(\varphi - \dfrac{\pi}{2}\right) + \pi\right]}{9\omega L_s}, & \dfrac{\pi}{3} < \varphi \le \dfrac{2\pi}{3} \end{cases} \tag{5}$$

where $d = V_o/N{\cdot}V_d$, and N is the transformer turns ratio.

According to (3)–(5), the current in each time interval can be obtained and the power equation can be calculated as

$$P_{o\_\rm DAB3} = \begin{cases} \dfrac{dV_d^2\varphi(4\pi - 3|\varphi|)}{6\pi\omega L_s}, & |\varphi| \le \pi/3 \\ \dfrac{dV_d^2(-18\varphi|\varphi| + 18\pi\varphi - \pi^2\cdot\varphi/|\varphi|)}{18\pi\omega L_s}, & \pi/3 < |\varphi| \le 2\pi/3. \end{cases} \tag{6}$$

In order to minimize the peak current and RMS current, the voltages on LVS and HVS should be matched, i.e., $d = 1$. The base power is defined as $1\,\text{p.u.} = V_d^2/\omega L_s$, and the power equation could be rewritten as

$$P_{o\_\rm DAB3}(\text{p.u.}) = \begin{cases} \dfrac{\varphi(4\pi - 3\varphi)}{6\pi}, & \varphi \le \pi/3 \\ \dfrac{-18\varphi^2 + 18\pi\varphi - \pi^2}{18\pi}, & \pi/3 < \varphi \le 2\pi/3. \end{cases} \tag{7}$$

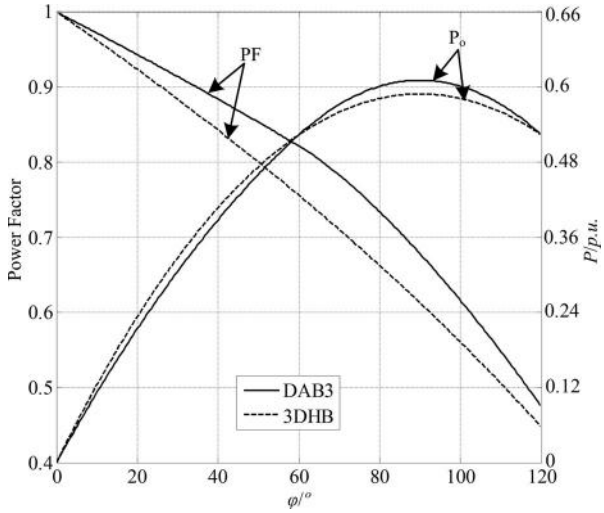

Fig. 3. Comparison of power and power factor for DAB3 and 3DHB converters.

If the neutral points of transformer n and m are connected to the corresponding middle points (o and o') of DC-link capacitors, the converter turns to be three interleaving single-phase DHB (3DHB) converter [17] and the power equation will be

$$P_{o\_3\rm DHB}(\text{p.u.}) = \frac{3\varphi(\pi - \varphi)}{4\pi},\ 0 < \varphi < \pi. \tag{8}$$

Fig. 3 shows the power curves of DAB3 and 3DHB converters. Under the same conditions, 3DHB converter has higher output power than DAB3 before 60° phase shift angle. The maximum output power of two converters are both at $\pi/2$

$$P_{o\_\max} = \begin{cases} \dfrac{7}{36}\pi = 0.611\,\text{p.u.}, & \text{DAB3} \\ \dfrac{3}{16}\pi = 0.589\,\text{p.u.}, & \text{3DHB.} \end{cases} \tag{9}$$

On the other hand, the transformer size and reactive power loss are determined by apparent power rating, which can be calculated by

$$S = 3V_{\rm an\_rms}\cdot I_{a\_\rm rms} \tag{10}$$

where the RMS value of current for different converter is

$$I_{a\_\rm rms} = \begin{cases} \begin{cases} \dfrac{V_d\varphi}{3\omega L_s}\sqrt{\dfrac{2\pi - \varphi}{\pi}}, & 0 < \varphi < \pi/3 \\ \dfrac{V_d\varphi}{6\omega L_s}\sqrt{\dfrac{2(4\pi - 3\varphi)}{\pi}}, & \pi/3 < \varphi < 2\pi/3 \end{cases} & \text{DAB3} \\ \dfrac{V_d\varphi}{\omega L_s}\sqrt{\dfrac{(3\pi - 2\varphi)}{6\pi}} & \text{3DHB.} \end{cases} \tag{11}$$

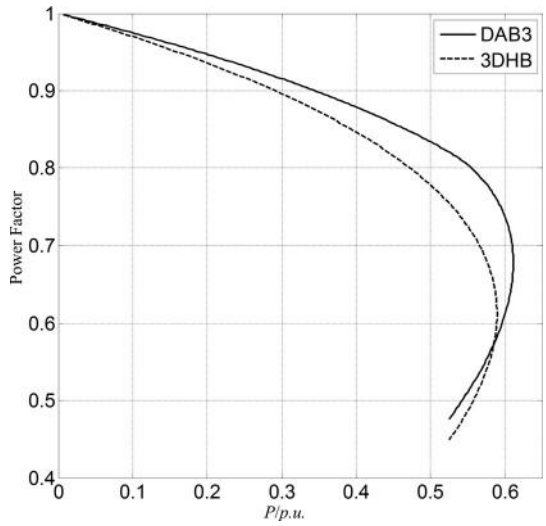

Fig. 4. Comparison of power and power factor for DAB3 and 3DHB converters.

Define the ratio of P_o/S as power factor (PF) of the transformer, and PF on these two converters can be derived as

$$\mathrm{PF}=\begin{cases}\begin{cases}\dfrac{(4\pi-3\varphi)}{2\sqrt{2\pi(2\pi-\varphi)}}, & 0<\varphi\le\dfrac{\pi}{3}\\[2ex] \dfrac{3(18\pi\varphi-\pi^2-18\varphi^2)}{2\sqrt{6\pi(9\pi^2\varphi-81\pi\varphi^2-\pi^3+54\varphi^3)}}, & \dfrac{\pi}{3}<\varphi\le\dfrac{2\pi}{3}\end{cases} & \text{DAB3}\\[2ex] \dfrac{3(\pi-\varphi)}{\sqrt{3\pi(3\pi-2\varphi)}}, & \text{3DHB}.\end{cases} \tag{12}$$

The power factor curves are also plotted in Fig. 3. As shown, the PF of 3DHB decreases faster than DAB3 with the phase shift angle increasing. Furthermore, the curves of PF versus output power are also plotted in Fig. 4. It shows that the power factor of DAB3 converter is always higher when generating the same real power, therefore less reactive power loss and higher efficiency is expected in DAB3 converter.

2) Varied Duty Cycle: Another feature of the current-fed DAB3 converter comes from its ability to interface with voltage varied energy source. With changes of the input voltage, duty cycle D is controlled to keep the DC-link voltage constant. For different duty cycle D and phase shift angle φ, the operating range can be divided into six areas, which are shown in Fig. 5. The corresponding current waveforms in different operating areas are also given in Fig. 5, and according to different current waveforms and voltage, the corresponding power equations can be derived. The calculation process of power flow is similar to the fixed duty cycle, which is described in (13):

$$P_{o\_\mathrm{DAB3}}=\begin{cases}\dfrac{K|\varphi|(4D\pi-\varphi)}{2\pi}, & I\\[2ex] \dfrac{-K[4\pi^2(3D-1)^2\mathrm{sgn}(\varphi)+3\varphi(9|\varphi|-4\pi-12D\pi)]}{36\pi}, & II\\[2ex] \dfrac{K|\varphi|(4\pi-3\varphi)}{6\pi}, & III\\[2ex] \dfrac{K[-[18(D-(1/2))^2+\pi^2]\mathrm{sgn}(\varphi)-18\varphi(|\varphi|-\pi)]}{9\pi}, & IV\\[2ex] \dfrac{-K[4\pi^2(2-3D)^2\mathrm{sgn}(\varphi)+3\varphi(9|\varphi|-16\pi+12D\pi)]}{36\pi}, & V\\[2ex] \dfrac{K[|\varphi|(4(1-D)\pi-\varphi)]}{2\pi}, & VI\end{cases} \tag{13}$$

where $K=V_d^2/\omega L_s$. The 3-D power flow is plotted in Fig. 6, and the global maximum power is still located at (1/2, π/2).

In practical use, duty cycle D is limited in [1/3, 2/3] considering the efficiency of converter and the variation range of input voltage, so that the DC-link voltage of LVS can keep constant with 100% variation of input voltage, i.e., V_{in} [V_d/3, 2V_d/3], which includes area II, III, IV, and V. Therefore, we focus on this operating range in this study. The power of current-fed 3DHB converter can be derived similarly

$$P_{o\_\mathrm{3DHB}}(\mathrm{p.u.})=\frac{3\varphi(4D\pi-4D^2\pi-|\varphi|)}{4\pi},\quad |\varphi|<2\pi/3,\ 1/3\le D\le 2/3. \tag{14}$$

In Fig. 7, the power flow curves of DAB3 and 3DHB in 3-D plot were drawn. The gray and black areas are the power of 3DHB and DAB3 converter, respectively. As shown, the power of 3DHB is higher than that of DAB3 converter with $\varphi<60^\circ$, which has the same conclusion as the case of 50% fixed duty cycle.

The reactive power on transformer and PF values of two converters can be calculated piecewise. Fig. 8 shows the PF curves versus phase shift angle φ in different D. The PF achieves the highest value at $D=1/2$ which will decrease when D is moving away from 1/2. Furthermore, the PF in DAB3 is always higher than 3DHB until D comes to 1/3 or 2/3, where they are squared. Fig. 9 also gives a comparison of PF between DAB3 and 3DHB – the ratio of $\mathrm{PF}_{\mathrm{DAB3}}$ to $\mathrm{PF}_{\mathrm{3DHB}}$ is always higher than 1. The analysis above indicates clearly that the reactive power loss increases with the increasing of phase shift angle, and the reactive power loss in $D=1/2$ is the smallest value so that the power efficiency is the highest. In practice, the magnetic flux swing and RMS current rating in transformer should be considered separately. For example, the power density can be higher at $D=1/3$ [18], as the maximum flux swing is smaller than $D=1/2$, which means smaller core or winding turns are needed. Thus, in application level, different D is chosen in voltage type converter based on different criteria.

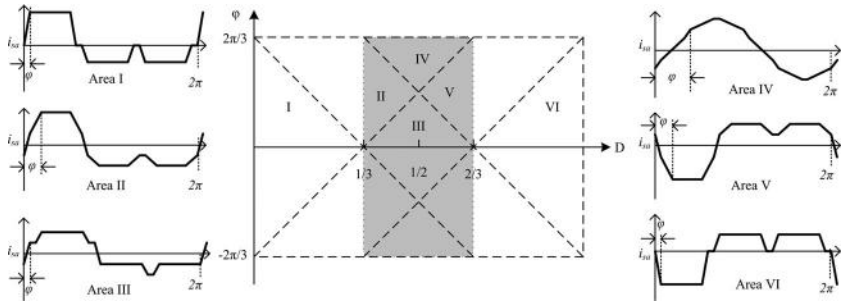

Fig. 5. Six operating areas with different (D, φ) and corresponding transformer current waveforms.

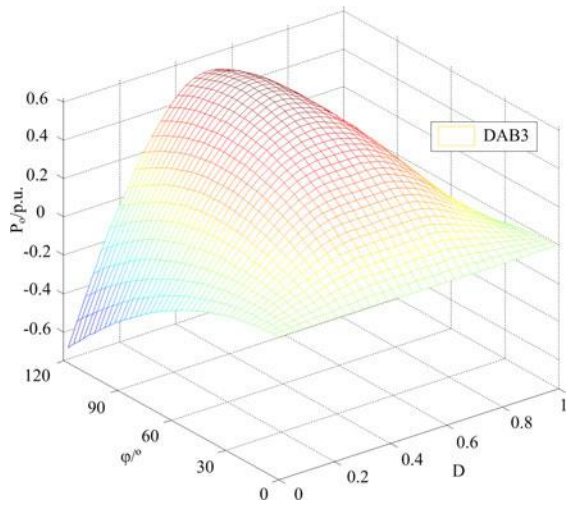

Fig. 6. Power flow versus duty cycle D and phase shift angle φ.

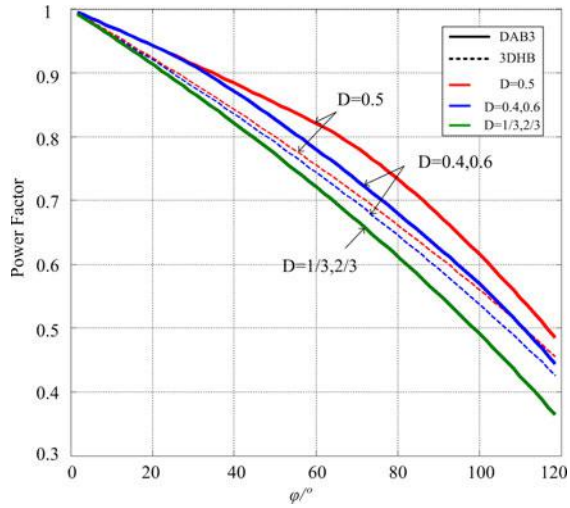

Fig. 8. *PF* of DAB3 and 3DHB converter with different (D, φ).

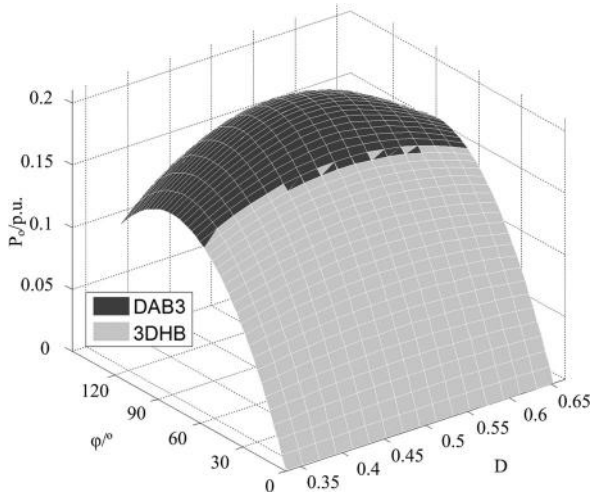

Fig. 7. Power flow of DAB3 and 3DHB converter with different (D, φ).

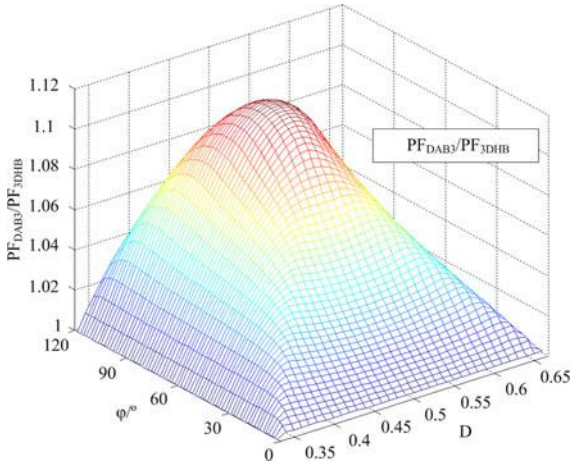

Fig. 9. Comparison of PF of DAB3 and 3DHB converter with different (D, φ).

When the input voltage changes, current-fed DAB3 (CF-DAB3) converter has smaller RMS current on the MOSFETs compared with the voltage type DAB3 converter. Define the base input voltage $V_{\text{in\_DAB3}}(1\text{ p.u.}) = V_o/N$, $V_{\text{in\_CF-DAB3}}(1\text{ p.u.}) = V_o/2\ N$, and RMS current on MOSFETs can be calculated and plotted in Fig. 10. As shown, when $V_{\text{in}} = 1$ p.u., voltage source DAB3 converter has smaller RMS current value compared with CF-DAB3. But when V_{in} changes, the RMS current on current-fed type will be lower than voltage type since it is able to maintain "$d = 1$" by controlling the duty cycle D. In summary, CF-DAB3 converter is a suitable topology for renewable energy source applications.

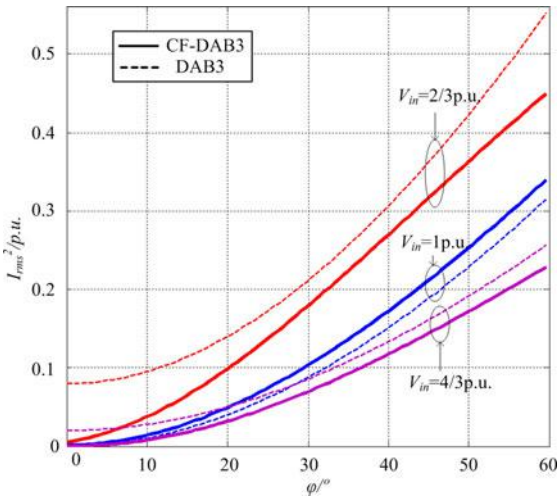

Fig. 10. RMS current curves on LVS MOSFETs.

III. Analysis of ZVS Conditions

In Section II, we showed that the reactive power in DAB3 is lower than in 3DHB converter, which also indicates the difficulty in maintaining soft switching conditions compared to DHB converter, as DAB3 converter has less reactive current. However, the ZVS condition is more critical in the current-fed type due to the effect of DC inductor current. This section will focus on the analysis of the ZVS conditions for DAB3 under different duty cycles and also find the relationship between the soft switching conditions and DC inductor.

A. ZVS Conditions for Voltage Source DAB3 Converter

In [1], the ZVS conditions are analyzed at $D = 1/2$. However, the ZVS conditions will also vary when D changes. The ZVS conditions of voltage type DAB3 converter turn to be

$$\begin{cases} i_{\mathrm{Ls}}(0) < 0, & \text{for LVS upper switches} \\ i_{\mathrm{Ls}}(2D\pi) > 0, & \text{for LVS lowerer switches} \\ i_{\mathrm{Ls}}(\varphi) > 0, & \text{for HVS upper switches} \\ i_{\mathrm{Ls}}(2D\pi+\varphi) < 0, & \text{for HVS lower switches.} \end{cases} \tag{15}$$

According to the calculation in Section II, the current values can be obtained, as well as ZVS conditions, in different operating area. The ZVS conditions of each switch in operation Area III can be further simplified to

$$\begin{cases} d < \dfrac{2\pi}{2\pi-3\varphi}, & \text{for LVS upper switches} \\ d > \dfrac{2\pi-3\varphi}{2\pi}, & \text{for HVS upper switches} \\ d < \dfrac{2\pi}{2\pi-3\varphi}, & \text{for LVS lower switches} \\ d > \dfrac{2\pi-3\varphi}{2\pi}, & \text{for HVS lower switches} \end{cases}, \quad \text{Area III.} \tag{16}$$

Similarly, ZVS conditions in other operation areas can also be described by d and φ. Fig. 11 plots the ZVS boundaries when D varies from 1/3 to 2/3. As shown, the ZVS boundaries will vary with various duty cycles, but ZVS is very well maintained on all switches when the DC-link voltages on LVS and HVS match each other. Therefore, $d = 1$ is the key to keeping ZVS conditions and lower switching loss.

B. ZVS Conditions for Current-fed DAB3 Converter

For the current-fed topology, the ZVS conditions are more complicated than voltage source type, since the DC input current changes the current waveforms on the switches of LVS. However, the transformer current is not affected by DC input current, thus the ZVS conditions on HVS switches are the same as voltage source DAB3 converter. ZVS conditions in boost mode and buck mode are symmetrical [16], so only boost mode is considered in this study.

Fig. 12 shows the circuits of one leg on LVS and HVS, as well as the denotation of current in each branch. Write the ZVS conditions on LVS as

$$\begin{cases} i_{\mathrm{ls}}(0) - i_{\mathrm{dc}}(0) < 0, & \text{for LVS upper switches} \\ i_{\mathrm{dc}}(2D\pi) - i_{\mathrm{ls}}(2D\pi) < 0, & \text{for LVS lower switches.} \end{cases} \tag{17}$$

The DC input current is related to the input power and DC inductor, which is shown in Fig. 13. Three operating areas ($D \in [1/3, 2/3]$, $\varphi \in [0, \pi/3]$) are under consideration here. By calculation, if $d = 1$, the ZVS conditions are always satisfied when $d = 1$, except in Area III. The ZVS conditions in Area III are described in (18)

$$\begin{cases} \dfrac{1}{9}\dfrac{V_d}{\omega L_s}(2\pi - 2d\pi + 3d\varphi) + \dfrac{P_{o\_III}}{3V_{\mathrm{in}}} \\ \quad + \dfrac{(1-D)V_{\mathrm{in}}\pi}{\omega L_{\mathrm{dc}}} > 0, & \text{for LVS upper switches} \\ \dfrac{P_{o\_III}}{3V_{\mathrm{in}}} - \dfrac{1}{9}\dfrac{V_d}{\omega L_s}(2\pi - 2d\pi + 3d\varphi) \\ \quad - \dfrac{(1-D)V_{\mathrm{in}}\pi}{\omega L_{\mathrm{dc}}} < 0, & \text{for LVS lower switches} \end{cases}, \quad \text{Area III.} \tag{18}$$

In (18), the upper switches on LVS can be soft switched, but the ZVS condition on lower switches is related to the DC inductor. Define $m = L_{\mathrm{dc}}/L_s$, and the in-equation in (18) can be simplified to

$$\frac{\varphi(4\pi - 3\varphi)}{18\pi D} - \frac{D(1-D)\pi}{m} - \frac{\varphi}{3} > 0. \tag{19}$$

Fig. 14 plots the ZVS region under different m, and it is clear that the soft switching region will increase when m decreases. Small DC inductor will result in large input current ripple, but the current ripples on each phase can be cancelled each other using interleaving strategy so the total current ripple can be alleviated significantly [19].

IV. Analysis of Unbalance Issue

Compared to the single-phase converters, multiphase converters have many advantages, but phase current unbalance is an important issue that should be solved. It is necessary to find

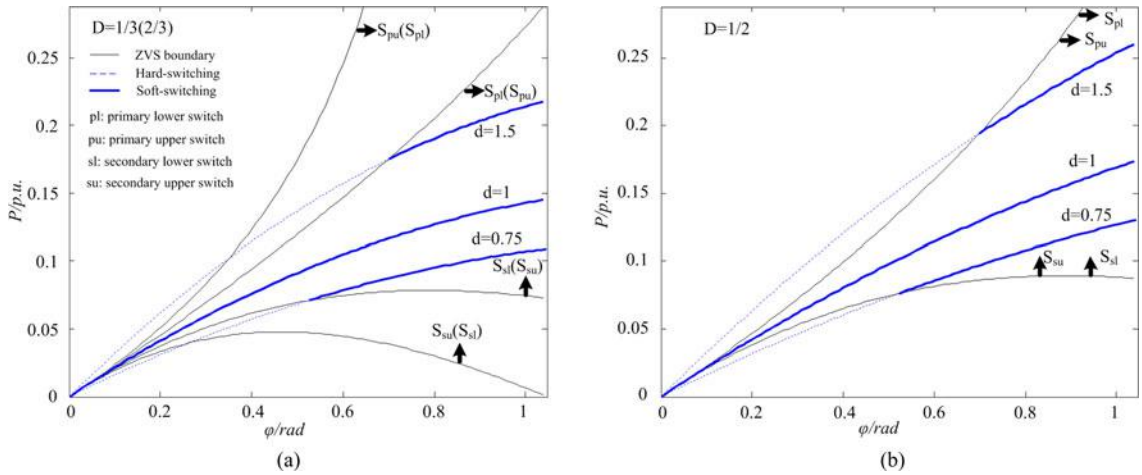

Fig. 11. ZVS boundaries and power curves at different D: (a) $D = 1/3, 2/3$. (b) $D = 1/2$.

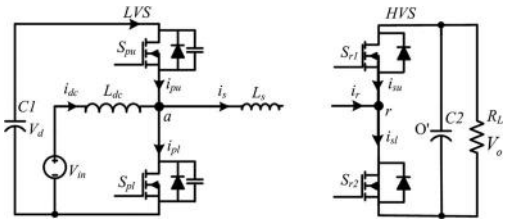

Fig. 12. Middle points of one leg on LVS and HVS.

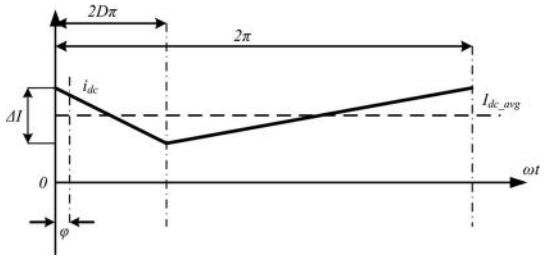

Fig. 13. DC inductor current in one switching period.

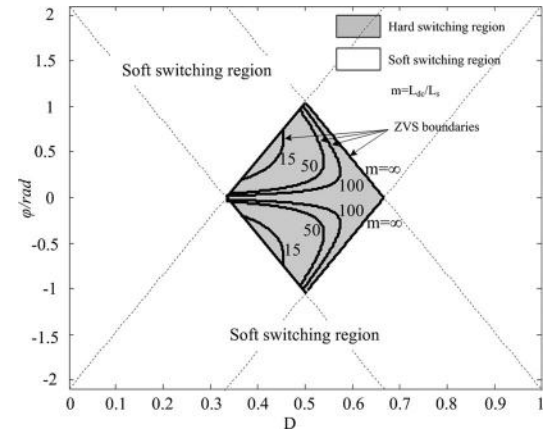

Fig. 14. ZVS boundaries under different m.

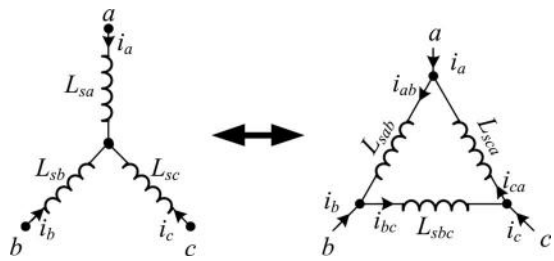

Fig. 15. Transformation between Y-model to Δ-model.

the reason for unbalance current and determine solution to alleviate its impact.

A. Analysis of Current Unbalance

According to the power equation, since the phase current is inversely proportional to the leakage inductance, the unbalanced leakage inductance will lead to unbalanced phase current. In [20], the relationship between phase current unbalance ratio ($\Delta I_\varphi\%$) and leakage inductance unbalance ratio ($\Delta L_s\%$) was analyzed. Different transformer connection types have different impacts on phase current. There are several sub types in DAB3 converter based on different transformer connections. Y-Y connection and Δ-Δ connection model can be transferred to each other, as shown in Fig. 15, so they have the same operation modes. Due to the features of phase shift method, the voltage waveforms on both sides of the transformer should have the same shape to avoid high reactive current, thus Δ-Y (or Y-Δ) connection type is not recommended. Fig. 16 shows the different transformer connection type of DAB3 and 3DHB converters. In Fig. 16, two different Δ-Δ types are distinguished by the position of leakage inductance. For Δ-Δ type DAB3 converter, the unbalanced leakage inductance will result in unbalanced transformer current, as well as unbalanced phase current.

Consider Fig. 16 (c) as an example, and define $K_{\mathrm{xy(xy=ab,bc,ca)}}$ as the coefficient to describe how far away the leakage inductance of each transformer is from the normal value $L_{\varphi 0}$, then

$$L_{\mathrm{xy}} = K_{\mathrm{xy}} L_{\varphi 0} = (1 + \Delta K_{\mathrm{xy}}) L_{\varphi 0},\ xy = \mathrm{ab,bc\ or\ ca} \quad (20)$$

where $\Delta K_{\mathrm{ab}} + \Delta K_{\mathrm{bc}} + \Delta K_{\mathrm{ca}} = 0$.

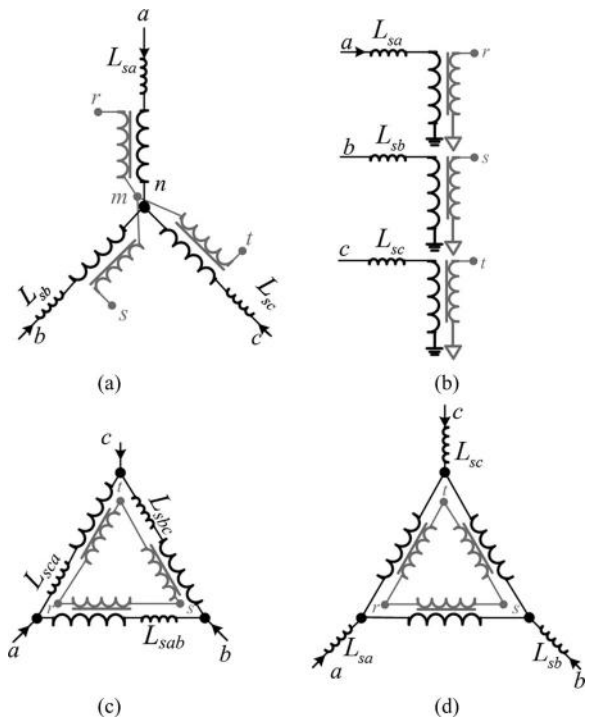

Fig. 16. Four transformer connection types DC-DC converter: (a) Y-Y DAB3. (b) 3DHB. (c) Δ-Δ DAB3 with integrated L_s. (d) Δ-Δ DAB3 with external L_s.

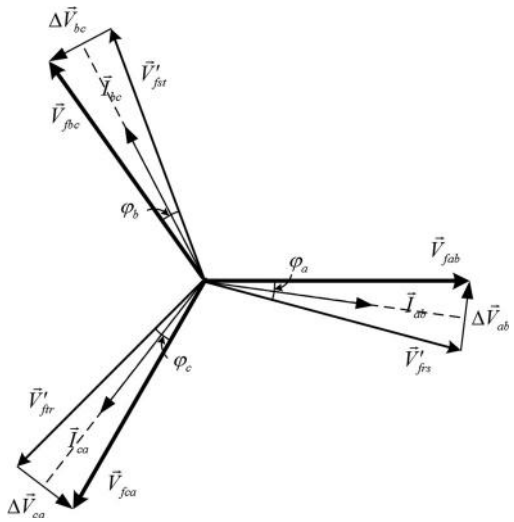

Fig. 17. Phasor diagram of phase voltage and current.

The fundamental model [1], [21] is applied in this study, and the current and voltage phasors are shown in Fig. 17. The phase voltage on HVS lags corresponding phase voltage on LVS φ_0. The transformer current $i_{\rm ab}$ is calculated as

$$\vec{I}_{\rm ab}=\frac{\Delta\vec{V}_{\rm ab}}{j\omega L_{\rm ab}}=\frac{\Delta\vec{V}_{\rm ab}}{j\omega L_{\varphi 0}K_{\rm ab}}=\frac{|\Delta V_0|}{\omega L_{\varphi 0}}(1-\Delta K_{\rm ab})\angle-\frac{\pi}{2} \tag{21}$$

where $|\Delta V_0|=V_d\varphi_0\sin(D\pi)/\pi$. So the amplitude of $i_{\rm ab}$ is

$$|\vec{I}_{\rm ab}|=\frac{|\Delta V_0|}{\omega L_{\varphi 0}}(1-\Delta K_{\rm ab})=(1-\Delta K_{\rm ab})I_{\phi 0}. \tag{22}$$

The phase current i_a can be obtained by

$$\vec{I}_a=\vec{I}_{\rm ab}-\vec{I}_{\rm ca}=\frac{\Delta\vec{V}_{\rm ab}}{j\omega L_{\varphi 0}K_{\rm ab}}-\frac{\Delta\vec{V}_{\rm ca}}{j\omega L_{\varphi 0}K_{\rm ca}}$$
$$=\frac{|\Delta V_0|}{\omega L_{\varphi 0}}\frac{\sqrt{K_{\rm ab}^2+K_{\rm ca}^2+K_{\rm ab}K_{\rm ca}}}{K_{\rm ab}K_{\rm ca}}\angle\left(\Delta\vec{V}_{\rm ab}-\frac{\pi}{3}\right). \tag{23}$$

By simplifying (23), we can get

$$|\vec{I}_a|\approx I_0\frac{1}{1+(\Delta K_{\rm ab}+\Delta K_{\rm ca})/2}=\left(1+\frac{\Delta K_{\rm bc}}{2}\right)I_0. \tag{24}$$

From (22) and (24), it can be seen that the transformer current unbalance ratio is the same as that of leakage inductance, i.e., $\Delta i_{\rm ab}\sim-\Delta K_{\rm ab}$, and the phase current unbalance ratio is just half of it, i.e., $\Delta i_a\sim\Delta K_{\rm bc}/2$. Using the same method, the relationship of current unbalance ratio and leakage inductance for other types of converters can be found and listed in Table I.

In Table I, "A" and "D" have the same performance that $\Delta I/I_0$ is halved comparing with $\Delta I/I_0$, so they have inherent current sharing capability. The $\Delta I/I_0$ in topology "B" is equal to ΔK of its own phase. In "C" the $\Delta I/I_0$ of phase current and that of transformer current are not consistent, which also implies that phase current and transformer current cannot be controlled to balance at the same time. In part B, the current sharing control analysis will be given in detail.

B. Current Sharing Control

Though topology A and D have inherent current sharing capability, the phase current are still asymmetrical when leakage inductances are not equivalent. The current sharing controller should be developed to make the current balance. We still use topology C as the objective, but transfer Δ-model to Y-model for simplicity. Define phase shift angles on each phase

$$\begin{cases}\varphi_a=\sigma_a\varphi_0\\ \varphi_b=\sigma_b\varphi_0\\ \varphi_c=\sigma_c\varphi_0\end{cases} \tag{25}$$

where $\sigma_{x(x=a,b\,\text{or}\,c)}=1+\Delta\sigma_x$ is the coefficient to describe how far away the phase shift angle of each phase is from the normal value φ_0 and $\Delta\sigma_a+\Delta\sigma_b+\Delta\sigma_c=0$.

The phase current i_a can be expressed as

$$\vec{I}_a=\frac{\Delta\vec{V}_{\rm an}}{j\omega L_{\rm sa}}=\frac{|\Delta V_0|\,(1+\Delta\sigma_a)}{\omega L_0(1+\Delta K_a)}\angle\left(\Delta\vec{V}_{\rm an}-\frac{\pi}{2}\right)$$
$$=|I_0|\,\frac{(1+\Delta\sigma_a)}{(1+\Delta K_a)}\angle\left(\Delta\vec{V}_{\rm an}-\frac{\pi}{2}\right). \tag{26}$$

In order to let $|I_a|$ equal to the average value $|I_0|$

$$\frac{1+\Delta\sigma_a}{1+\Delta K_a}=1. \tag{27}$$

So we have

$$\Delta\sigma_x=\Delta K_x,\quad x=a,b\,\text{or}\,c. \tag{28}$$

TABLE I
$\Delta I/I_{\rm avg}$ RESULTING FROM UNBALANCED LEAKAGE INDUCTANCE

Index	Connection type	Phase current	Transformer current
A	Y-Y connection	$\Delta I_a/I_0 = -\Delta K_a/2$ $\Delta I_b/I_0 = -\Delta K_b/2$ $\Delta I_c/I_0 = -\Delta K_c/2$	
B	3DHB	$\Delta I_a/I_0 = -\Delta K_a$ $\Delta I_b/I_0 = -\Delta K_b$ $\Delta I_c/I_0 = -\Delta K_c$	
C	Δ-Δ connection with integrated L_s	$\Delta I_a/I_0 = \Delta K_{bc}/2$ $\Delta I_b/I_0 = \Delta K_{ca}/2$ $\Delta I_c/I_0 = \Delta K_{ab}/2$	$\Delta I_{ab}/I_{\varphi 0} = -\Delta K_{ab}$ $\Delta I_{bc}/I_{\varphi 0} = -\Delta K_{bc}$ $\Delta I_{ca}/I_{\varphi 0} = -\Delta K_{ca}$
D	Δ-Δ connection with external L_s	$\Delta I_a/I_0 = -\Delta K_b/2$ $\Delta I_b/I_0 = -\Delta K_c/2$ $\Delta I_c/I_0 = -\Delta K_a/2$	$\Delta I_{ab}/I_{\varphi 0} = -\Delta K_c/2$ $\Delta I_{bc}/I_{\varphi 0} = -\Delta K_a/2$ $\Delta I_{ca}/I_{\varphi 0} = -\Delta K_b/2$

*: the subscript of K depends on the position of the L_s

TABLE II
RELATIONSHIP BETWEEN REGULATION OF φ AND $\Delta I/I_{\rm avg}$

Index	Connection type	Phase current	Transformer current
A	Y-Y connection	$\Delta I_a/I_0 = \Delta\sigma_a/2$ $\Delta I_b/I_0 = \Delta\sigma_b/2$ $\Delta I_c/I_0 = \Delta\sigma_c/2$	
B	3DHB	$\Delta I_a/I_0 = \Delta\sigma_a$ $\Delta I_b/I_0 = \Delta\sigma_b$ $\Delta I_c/I_0 = \Delta\sigma_c$	
C	Δ-Δ connection with integrated L_s	$\Delta I_a/I_0 = \Delta\sigma_c/2$ $\Delta I_b/I_0 = \Delta\sigma_b/2$ $\Delta I_c/I_0 = \Delta\sigma_a/2$	$\Delta I_{ab}/I_{\varphi 0} = \Delta\sigma_c$ $\Delta I_{bc}/I_{\varphi 0} = \Delta\sigma_a$ $\Delta I_{ca}/I_{\varphi 0} = \Delta\sigma_b$
D	Δ-Δ connection with external L_s	$\Delta I_a/I_0 = \Delta\sigma_a/2$ $\Delta I_b/I_0 = \Delta\sigma_b/2$ $\Delta I_c/I_0 = \Delta\sigma_c/2$	$\Delta I_{ab}/I_{\varphi 0} = \Delta\sigma_c/2$ $\Delta I_{bc}/I_{\varphi 0} = \Delta\sigma_a/2$ $\Delta I_{ca}/I_{\varphi 0} = \Delta\sigma_b/2$

Consider the transformer current $I_{\rm ab}$ in Δ-model.

$$\vec{I}_{\rm ab} = \frac{\Delta\vec{V}_{\rm ab}}{j\omega L_{\rm sab}} = \frac{|\Delta V_{\varphi 0}|\,(1+\Delta\sigma_{\rm ab})}{\omega 3L_0(1-\Delta K_c)}\angle\left(\Delta\vec{V}_{\rm ab}-\frac{\pi}{2}\right)$$
$$= |I_{\varphi 0}|\,\frac{(1-(\Delta\sigma_c/2))}{(1-\Delta K_c)}\angle\left(\Delta\vec{V}_{\rm ab}-\frac{\pi}{2}\right). \quad (29)$$

To make the transformer current $i_{\rm ab}$ balance, the regulation of phase shift angle is

$$\frac{(1-(\Delta\sigma_c/2))}{(1-\Delta K_c)} = 1. \quad (30)$$

So for three-phase system, the regulation of phase shift angle is

$$\Delta\sigma_x = 2\Delta K_x, \quad x = a, b \text{ or } c. \quad (31)$$

Equations (28) and (31) cannot be satisfied at the same time, so for topology C there is no current sharing controller which can make the phase current and transformer current to be balanced. Using the same method, the regulation of phase shift angle in other topology can be calculated and listed in Table II. In Table II, only topology C cannot realize current sharing control, so Δ-Δ type should be avoided if using integrated leakage inductance as the main power transfer element.

Based on the relationship between phase shift angle and unbalanced current ratio, the ratio of each phase shift angle σ_x can be set and applied to phase shift controller. Fig. 18 shows the flow chart of ratio presetting current sharing control, where N_i is the times of tuning ($1 \sim \infty$). Using this method, the ratio of phase shift angle can be tuned faster than a PI controller.

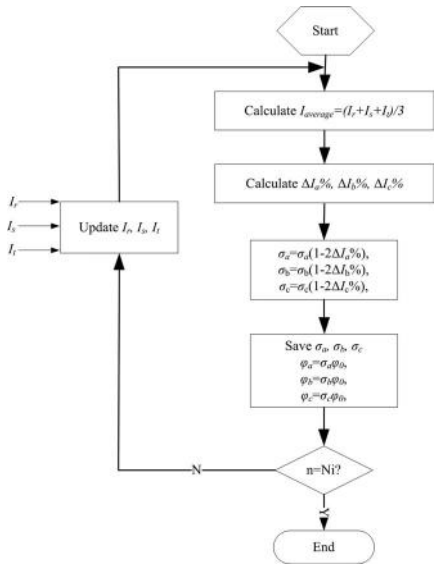

Fig. 18. Flow chart of ratio presetting current sharing control.

The simulation in Psim is to verify the analysis. In the simulation, the leakage inductances were selected as: $L_{\rm sa} = 520$ nH, $L_{\rm sb} = 444$ nH, $L_{\rm sc} = 370$ nH, which demonstrated 17% inductance unbalance. Figs. 19 and 20 show the simulation results for split capacitor and Y-Y type converters when output power is 4 kW and input voltage is 24 V. For split capacitor type converter, without current sharing control, the phase shift angle is 0.043π and the phase current are $I_{\rm sa} = 34.9$ A, $I_{\rm sb} = 40.9$ A and $I_{\rm sc} =$

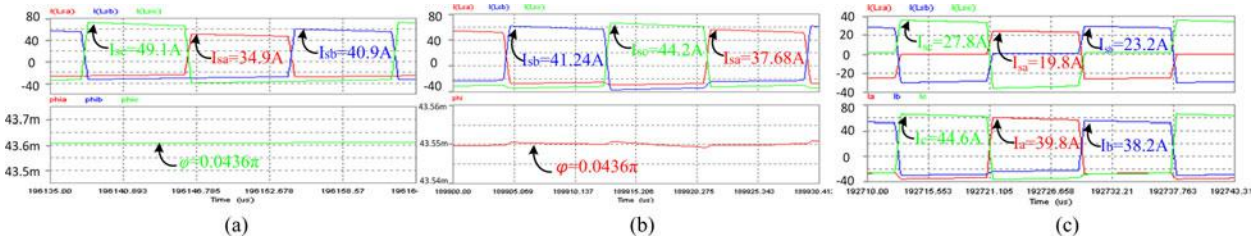

Fig. 19. Phase current and transformer current waveforms without unbalance controller: (a) Split-cap type. (b) Y-Y type. (c) Δ- Δ type.

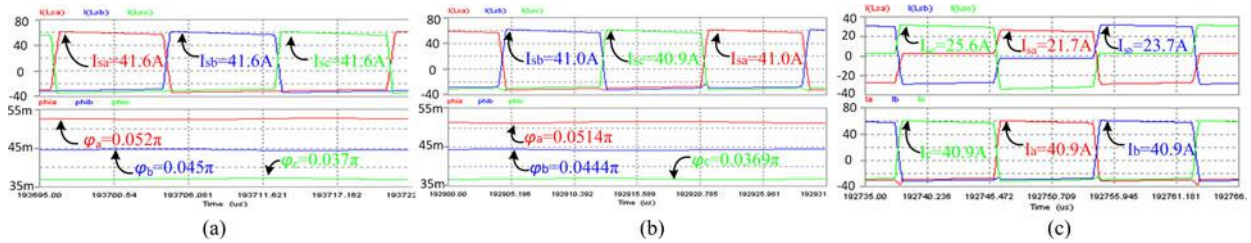

Fig. 20. Phase current and transformer current waveforms with unbalance controller: (a) Split-cap type. (b) Y-Y type. (c) Δ- Δ type.

49.1 A, respectively, which are shown in Fig. 19(a) and have 16% unbalance ratio. With current sharing control, the phase shift angles are different and the phase current are balanced with the value 41.6 A. With current sharing control, square of RMS current value decreases from 5302 A^2 to 5217 A^2, so it will help to decrease the conducting loss and improve the efficiency. For Y-Y type converter, without current sharing control, as shown in Fig. 20(a), the phase shift angle is 0.043π and $I_{\rm sa} = 37.7$ A, $I_{\rm sb} = 41.2$ A and $I_{\rm sc} = 44.2$ A, which have only 8.7% difference. With current sharing control, the phase current is balanced and $I_{\rm sa} = I_{\rm sb} = I_{\rm sc} = 41.0$ A. The square of RMS current value decreases from 5115 A^2 to 5018 A^2. Comparing Y-Y type with split capacitor type, former has smaller RMS current and higher efficiency.

V. Converter Design Guideline

A. Transformer Design

A 6 kW converter is designed with varied low input voltage (24 V – 48 V) and rated high output voltage 288 V. The DC-link voltage on LVS $V_d = V_{\rm in}/D$ is constant, therefore the transformer turns ratio is determined by $N = V_o/V_d = DV_o/V_{\rm in} = 4$. The leakage inductance is integrated into the transformer. Compared to traditional transformers, PCB planar transformers provide better consistency and flexibility. Each transformer consists of 2 E64-3C92 planar cores with separate primary and secondary PCBs. The primary and secondary windings have 4 turns and 16 turns, respectively. Each turn on LVS and HVS is made up of two paralleled 4 oz copper windings, therefore satisfying the requirement of current density and helping to reduce AC resistance. Though the interleaving transformer windings structure can reduce the AC resistance significantly, it is very hard to provide enough leakage inductance as energy transfer element, thus additional leakage inductance is needed. By using

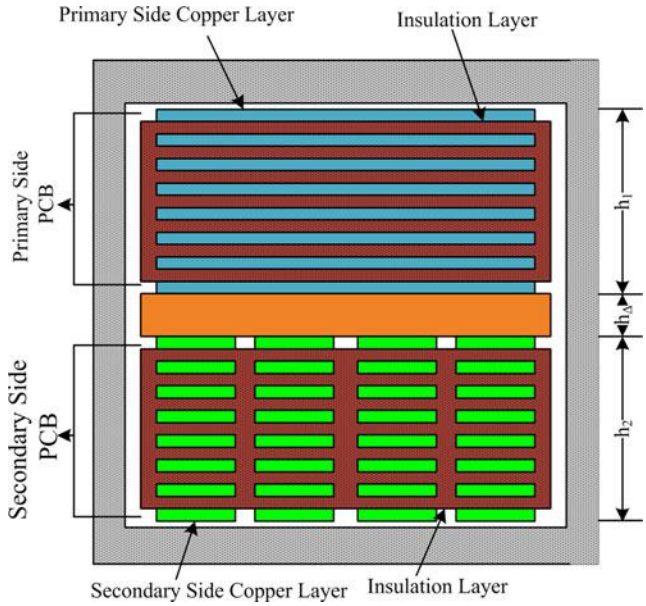

Fig. 21. Sectional view of transformer.

two separate PCB windings as primary and secondary winding, the desired leakage inductance can be controlled by adjusting the distance between the two PCBs. The single-phase transformer prototype is shown in Fig. 21. The primary and secondary PCBs are separated by a thickness h_Δ and the leakage inductance for the non-interleaved structure is given in (32) [22]:

$$L_s = \mu_0 N^2 \frac{l_w}{b_w}\left(\frac{h_1 + h_2}{3} + h_\Delta\right) \tag{32}$$

where μ_0 is the permeability of air (H/m), N is turns ratio, l_w is the mean length of traces (m), and b_w is the width of primary trace (m). h_1 and h_2 are the thickness of primary and secondary

TABLE III
LEAKAGE INDUCTANCE OF EACH PHASE (REFER TO LVS)

	Leakage inductance
Designed L_s	510nH
Measured L_{sa}	511.8nH
Measured L_{sb}	517.5nH
Measured L_{sc}	505nH

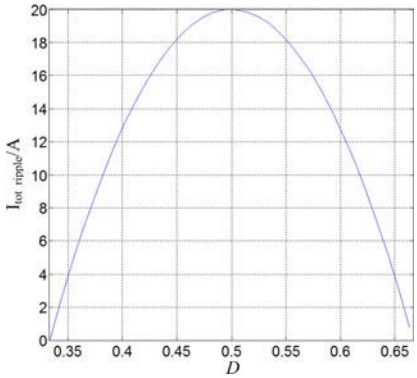

Fig. 22. Input current ripple versus duty cycle.

side, and h_Δ is the distance between them. Table III gives the designed and measured leakage inductance of each transformer.

B. DC Inductor Design

The main goals of DC inductor design are to maintain the ZVS and achieve small size. The DC inductance should meet the in-equation (21), i.e., $L_{\rm dc} < 11L_s$. In the experiment, the DC inductor is designed as $L_{\rm dc} = 12L_s = 6\ \mu$H, so the phase current ripple $\Delta I_{\rm dc}$ is as large as $2I_{\rm dc}$ at rated power, and at the same time ZVS can be guaranteed in a majority of operation area. For three-phase interleaving structure, the total input current ripple is given as

$$I_{\rm tot\_ripple} = \left| \frac{3V_d(D-1/3)(D-2/3)}{f_s L_{\rm dc}} \right|. \tag{33}$$

Fig. 22 shows the total input current ripple will reach zero at $D = 1/3$ and 2/3 but maximum value is 20 A at $D = 1/2$.

C. Power Loss Analysis

The power loss of converter is the key factor for component selection and design. For DC-DC converters, the losses are mainly switching loss and conduction loss. For the switching loss, the converter is operating in ZVS situation, so there is no turn-on loss, only turn-off loss is considered, which can be approximately calculated by [23]

$$P_{\rm sw\_off} = \frac{I_{\rm off}^2 t_f^2 f_s}{24C} \tag{34}$$

where $I_{\rm off}$ is the turn off current, t_f is the falling time of MOSFET, and C is the snubber capacitance. Larger snubber capacitance will get smaller turn-off loss, but it will cause turn-on loss especially at light load since there is not enough current

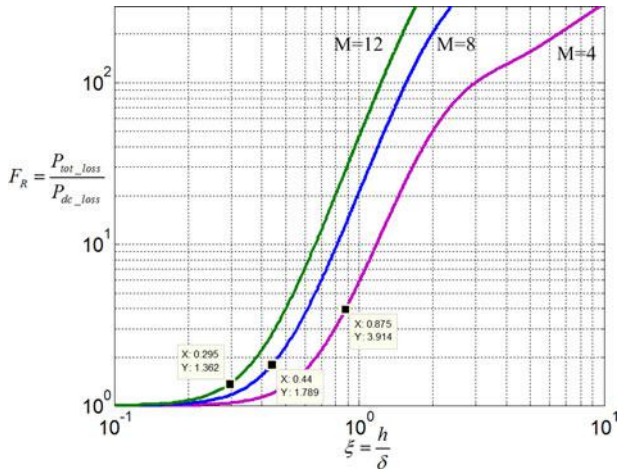

Fig. 23. Total winding copper loss ratio versus ξ and number of layers M.

to release the energy stored in the snubber capacitors and the ZVS condition will be unsatisfied. So choosing proper snubber capacitor is important. In the experiment, 0.2 μF and 0.03 μF capacitors are selected as snubber capacitors on LVS and HVS MOSFETs, respectively.

The conduction losses include the losses in DC inductor windings, MOSFETs and transformer windings. The current ripple I_Δ on DC inductor is not related to the output power, which can be written as

$$I_\Delta = \frac{V_d D(1-D)}{L_{\rm dc} f_s}. \tag{35}$$

And the AC flux density of inductor can be calculated by

$$B_{\rm AC} = \frac{L_{\rm dc} \cdot I_\Delta}{A_c N_L} \tag{36}$$

where A_c is the sectional area of magnetic core, and N_L is the turns number. $B_{\rm AC}$ always exists even at no load thus AC core loss dominates the major power loss at the light load. When there is power drawn from the energy source, the RMS current value on each inductor is derived by

$$\begin{aligned} I_{\rm Ldc\_rms} &= \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_{\rm Ldc}^2(\theta)d\theta} \\ &= \sqrt{\frac{1}{\pi}\int_0^1 \left(I_\Delta x + \frac{P_o}{3V_{\rm in}\eta} - \frac{1}{2}I_\Delta\right)^2 dx} \end{aligned} \tag{37}$$

where P_o is the output power and η is the efficiency. In order to find the transformer conduction loss, the transformer RMS current value can also be calculated as

$$\begin{aligned} I_{\rm Ls\_rms} &= \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_{Ls}^2(\omega t)d\omega t} \\ &= \begin{cases} \dfrac{V_d\varphi}{3\omega L_s}\sqrt{\dfrac{2\pi-\varphi}{\pi}}, & D = 1/2 \\ \dfrac{V_d\varphi}{6\omega L_s}\sqrt{\dfrac{2(4\pi-3\varphi)}{\pi}}, & D = 1/3, 2/3. \end{cases} \end{aligned} \tag{38}$$

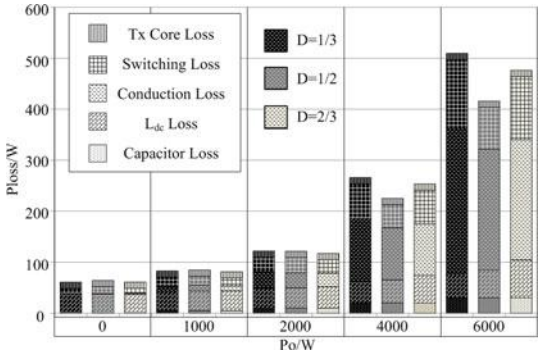

Fig. 24. $P_{\rm loss}$ distribution in different output power in different D.

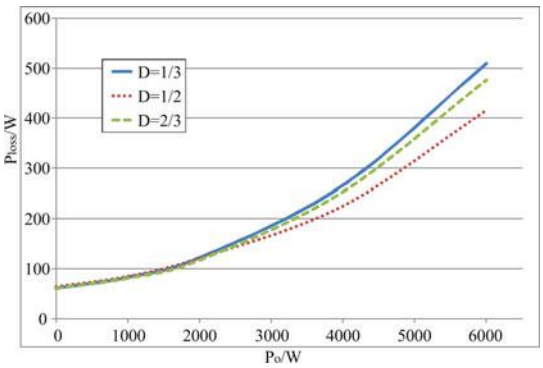

Fig. 25. Total $P_{\rm loss}$ curves in different D.

TABLE IV
SPECIFICATIONS AND PARAMETERS OF CONVERTER

Input voltage V_{in} (V)	24~48
Output voltage V_o (V)	288
Rated power P_o (W)	6000
Switching frequency f_s (kHz)	40
LVS MOSFETs	SK 260MB10
LVS Snubber	0.2 μF
HVS MOSFETs	ST W45NM50FD
HVS Snubber	30 nF
LVS Capacitor	5600μF + 10 μF*25 (MLCC)
HVS Capacitor	390 μF + 10 μF*5 (Film)
HF Transformer	E64-3C92*6
DC Inductor	E64-3C92*6

From (36) to (38), the DC inductor core loss can be obtained by the following empirical formula

$$P_{\rm Ldc\_core} = V_e C_m f^x B_{\rm AC}^y \tag{39}$$

where V_e is effective core volume of transformer, C_m, x, and y are coefficient related to core material. The DC inductor conduction loss is

$$P_{\rm Ldc\_con} = I_{\rm Ldc\_rms}^2 R_{\rm Ldc}. \tag{40}$$

The transformer core loss has the same form as equation (39), and the conduction loss can be written by

$$P_{\rm Tx\_con} = I_{\rm Ls\_rms}^2 \left(R_{\rm dc} + R_{\rm ac}\right). \tag{41}$$

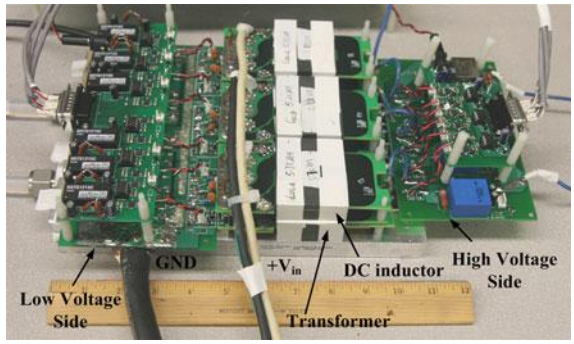

Fig. 26. Photo of 6 kW experimental prototype.

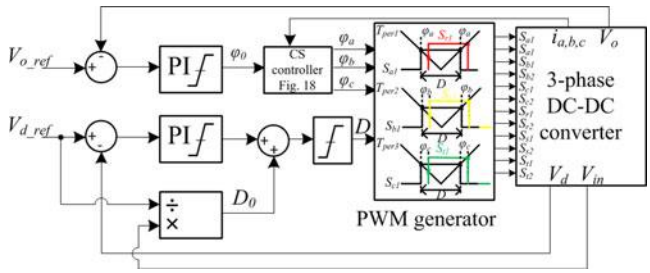

Fig. 27. System control system including current sharing controller.

The total conduction loss of MOSFETs on HVS can be calculated as

$$P_{\rm HVS\_con} = 6\left(\frac{I_{\rm Ls\_rms}^2 R_{\rm ds\_on}}{2}\right) = 3I_{\rm Ls\_rms}^2 R_{\rm ds\_on} \tag{42}$$

where $R_{\rm ds\_on}$ is the turn on resistance of MOSFET.

The conduction loss on one MOSFET of LVS is different from that of HVS since the dc inductor current will affect the current waveform in MOSFET. In addition, the current flowing through the upper switches and lower switches are asymmetrical, the RMS values of current in different D can be calculated as follows, (43) and (44) at the bottom of the next page.

So the conduction loss of MOSFET on LVS can be expressed as

$$P_{\rm LVS\_con} = 3(I_{\rm upper\_rms}^2 + I_{\rm lower\_rms}^2) R_{\rm ds\_on}. \tag{45}$$

For the transformer design, using 2 paralleled 4 oz PCB windings to replace 8 oz PCB winding, the AC resistance of transformer winding $R_{\rm ac}$ is reduced from $2.9R_{\rm dc}$ to $0.79\ R_{\rm dc}$ [24]. Define the ratio of total copper loss to DC copper loss $F_R = P_{\rm tot\_loss}/P_{\rm dc\_loss}$, and the ratio of the conductor thickness h to the skin depth δ, i.e., $\xi = h/\delta$. Fig. 23 shows F_R versus ξ in different number of layers. It is clear that the total copper loss is reduced from $3.914P_{\rm dc\_loss}$ to $1.789P_{\rm dc\_loss}$. In Fig. 23, when the number of copper layers M increases to 12, the total copper loss just decreases by $0.43P_{\rm dc\_loss}$, but more counts of copper layers will increase the cost.

Fig. 24 gives the power loss distribution in different power rating at different duty cycle. It can be seen that the DC inductors' loss always exists because of the ripple current and it is dominant at the light load, and the conduction loss and switching loss will be dominant at the heavy load. Fig. 25 shows

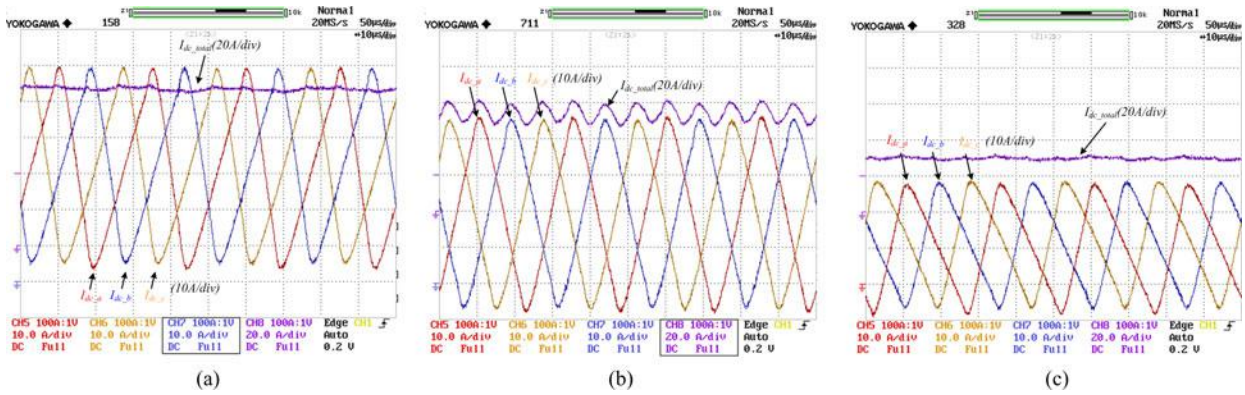

Fig. 28. Three-phase inductor current and total input current: (a) $I_{\rm dc}$ at $D = 1/3$. (b) $I_{\rm dc}$ at $D = 1/2$. (c) $I_{\rm dc}$ at $D = 2/3$.

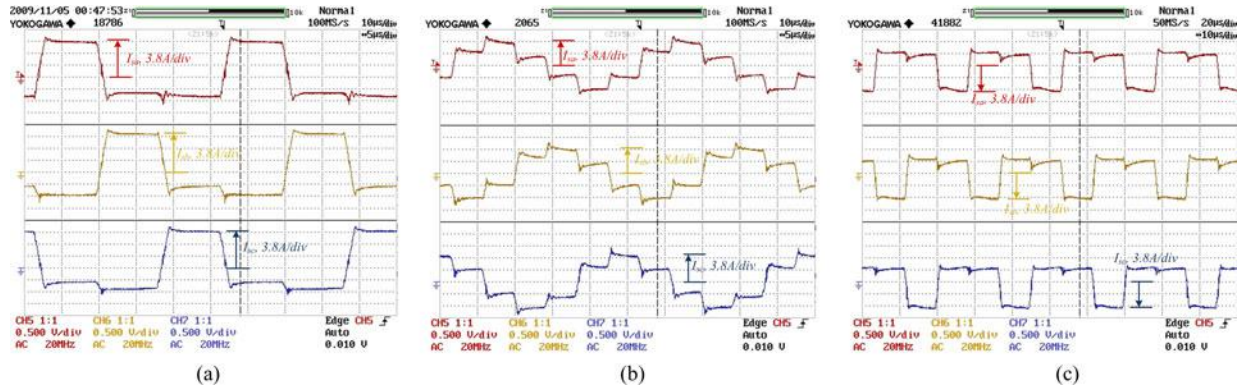

Fig. 29. Transformer current waveforms on secondary side in different D: (a) $D = 1/3$. (b) $D = 1/2$. (c) $D = 2/3$.

the total power loss curve in different duty cycle. Lower power loss in $D = 1/2$ can be obtained due to the smaller transformer and switches' current, which is also consistent with the analysis in Section II.

VI. Experimental Results

A 6 kW experimental prototype is built in the lab, and the specifications and parameters of the converter are listed in Table IV. The input voltage varies from 24 V to 48 V, and output voltage is 288 V. Fig. 26 shows a photo of the 6-kW prototype with a liquid-cooled heat sink. The size of this converter is 13.7″ by 7.8″. The DC inductors and transformers are implemented with PCBs and 6 E64-3C92 planar cores. Fig. 27 is the control diagram including current sharing controller. The duty cycle D is just controlled to keep LVS DC-link voltage constant, and phase shift angle is used to control the output voltage. The duty cycle D and phase shift angle is used to control the output voltage.

Fig. 28 shows the transformer current with different duty cycle. The current become 2 level waveforms in $D = 1/3$, 2/3, which are the same as 3DHB converter. Fig. 29 shows the DC

$$I_{\rm upper\_rms} = \begin{cases} \dfrac{V_d}{324\pi\omega L_s}\sqrt{972\varphi^2\pi^2 + 16524\varphi^3\pi - 19683\varphi^4 + 4\pi^4}, & D = 1/3 \\ \dfrac{V_d}{144\pi\omega L_s}\sqrt{2(320\varphi^2\pi^2 + 864\varphi^3\pi - 576\varphi^4 + 3\pi^4)}, & D = 1/2 \\ \dfrac{V_d}{648\pi\omega L_s}\sqrt{2(1944\varphi^2\pi^2 + 34020\varphi^3\pi - 19683\varphi^4 + 16\pi^4)}, & D = 2/3 \end{cases} \tag{43}$$

$$I_{\rm lower\_rms} = \begin{cases} \dfrac{V_d}{162\pi\omega L_s}\sqrt{17253\varphi^2\pi^2 + 35235\varphi^3\pi + 19683\varphi^4 + 648\varphi\pi^3 + 14\pi^4}, & D = 1/3 \\ \dfrac{V_d}{144\pi\omega L_s}\sqrt{6(1472\varphi^2\pi^2 - 1760\varphi^3\pi + 576\varphi^4 + \pi^4)}, & D = 1/2 \\ \dfrac{V_d}{648\pi\omega L_s}\sqrt{144828\varphi^2\pi^2 - 246888\varphi^3\pi - 98415\varphi^4 - 2592\varphi\pi^3 + 98415\pi^4}, & D = 2/3. \end{cases} \tag{44}$$

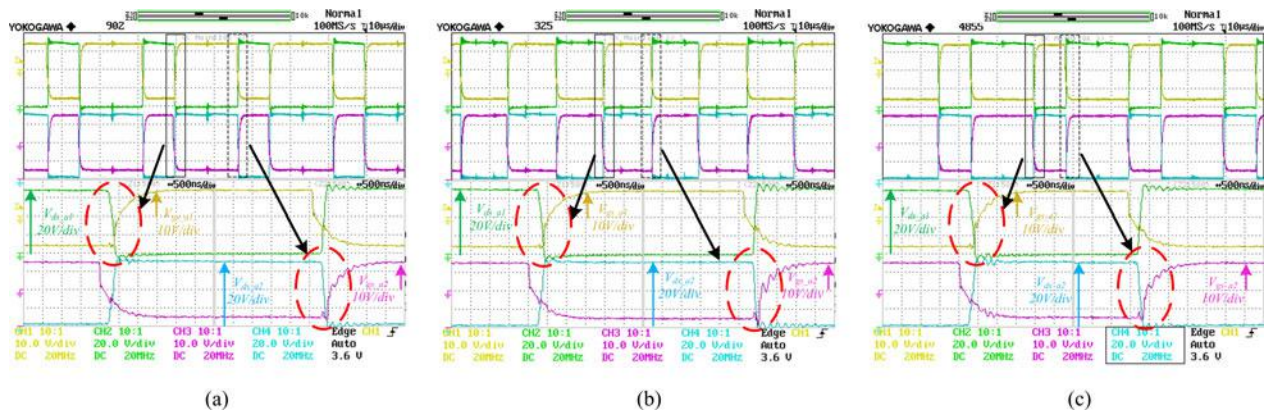

Fig. 30. ZVS waveforms for S_{a1} and S_{a2} at $P_o = 1200$ W in (a) $V_{\rm in} = 24$ V. (b) $V_{\rm in} = 36$ V. (c) $V_{\rm in} = 48$ V.

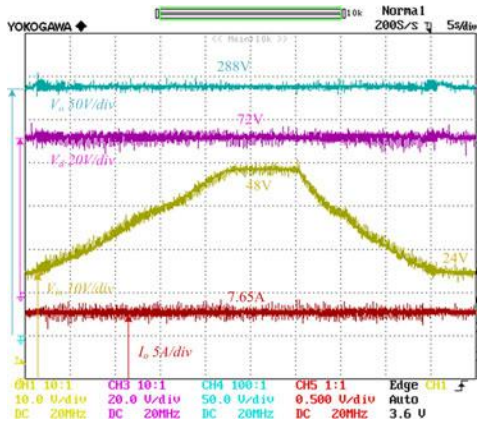

Fig. 31. Voltage and current waveforms when $V_{\rm in}$ varies between 24 V and 48 V.

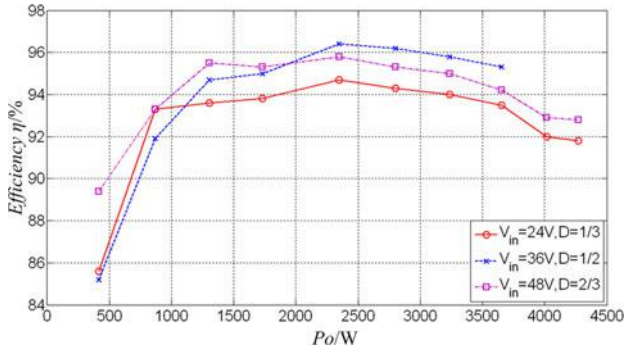

Fig. 32. Measured efficiency of proposed converter at $V_{\rm in} = 24$ V, 36 V and 48 V.

inductor current and total input current with $D = 1/3$, 1/2 and 2/3, respectively. The large DC inductor current ripple of each phase is beneficial for device ZVS operation and lower inductor volume size but a total small current ripple can be achieved by interleaving three-phase current. It can be seen that when $D = 1/3$ and 2/3, the input current ripple is minimum, and when $D = 1/2$, the current ripple reaches maximum value. As shown in Fig. 30, the ZVS is always guaranteed in the switches of LVS in the light load under varied input voltage. Fig. 31 shows that when the input voltage changes from 24 V to 48 V, duty cycle is changed with the input voltage $V_{\rm in}$ and satisfies $D = V_d/V_{\rm in}$. The measured efficiency from 450 W to 4.5 kW with different input voltage is shown in Fig. 32. The efficiencies in different input voltage keep stable, and the highest efficiency is 96.4% at $V_{\rm in} = 36$ V and $P_o = 2.3$ kW.

VII. Conclusion

This paper proposes a three-phase current-fed bidirectional isolated DC-DC converter to achieve high efficiency over a wide input voltage range. By using the proposed technology, the reactive power loss is always maintained to be low and ZVS conditions can be maintained when input voltage changes, so high efficiency can be guaranteed over a wide operation range. Another feature of the proposed topology is to allow the small passive components while the current and voltage ripples can still remain small due to three-phase interleaving structure. The maximum input current ripple is no more than 20% of total input current. With respect to the leakage inductance unbalance ratio, the proposed topology with Y-Y connected transformers decreases the current unbalance ratio by half. Although Δ-Δ type topology achieves a similar performance, the phase current and transformer current cannot be regulated to balance at the same time. In addition, PCB planar transformers are applied to achieve the lower profile and better consistency compared with conventional transformers. Finally, both the power loss calculation and the experimental results based on a 6-kW optimal designed prototype validate the effectiveness of the proposed topology.

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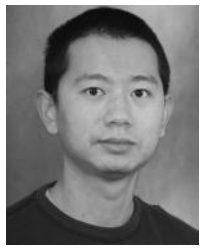

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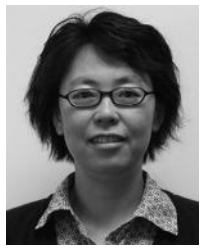

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